

FEATURES

- 4 ADCs integrated into 1 package
- 98 mW ADC power per channel at 50 MSPS
- SNR = 73 dB (to Nyquist)
- ENOB = 12 bits
- SFDR = 84 dBc (to Nyquist)
- Excellent linearity
 - DNL = ± 0.5 LSB (typical)
 - INL = ± 1.5 LSB (typical)
- Serial LVDS (ANSI-644, default)
 - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 315 MHz full-power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation
- Serial port control
 - Full-chip and individual-channel power-down modes
 - Flexible bit orientation
 - Built-in and custom digital test pattern generation
 - Programmable clock and data alignment
 - Programmable output resolution
 - Standby mode

APPLICATIONS

- Medical imaging and nondestructive ultrasound
- Portable ultrasound and digital beam-forming systems
- Quadrature radio receivers
- Diversity radio receivers
- Tape drives
- Optical networking
- Test equipment

GENERAL DESCRIPTION

The AD9259 is a quad, 14-bit, 50 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 50 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

Rev. D

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FUNCTIONAL BLOCK DIAGRAM

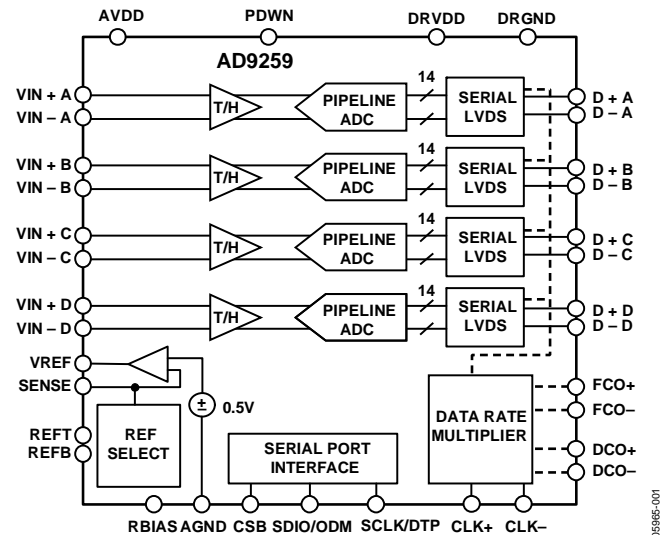


Figure 1.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual-channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9259 is available in a RoHS compliant, 48-lead LFCSP. It is specified over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

PRODUCT HIGHLIGHTS

1. Small Footprint. Four ADCs are contained in a small, space-saving package.
2. Low power of 98 mW/channel at 50 MSPS.
3. Ease of Use. A data clock output (DCO) operates at frequencies of up to 350 MHz and supports double data rate (DDR) operation.
4. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.
5. Pin-Compatible Family. This includes the AD9287 (8-bit), AD9219 (10-bit), and AD9228 (12-bit).

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6/06—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 1.

| Parameter ¹ | Temperature | Min | Typ | Max | Unit |
|---|-------------|-----|------------|-------|--------|
| RESOLUTION | | 14 | | | Bits |
| ACCURACY | | | Guaranteed | | |
| No Missing Codes | Full | | | | |
| Offset Error | Full | | ±1 | ±8 | mV |
| Offset Matching | Full | | ±2 | ±8 | mV |
| Gain Error | Full | | ±0.5 | ±2 | % FS |
| Gain Matching | Full | | ±0.3 | ±0.7 | % FS |
| Differential Nonlinearity (DNL) | Full | | ±0.5 | ±1.0 | LSB |
| Integral Nonlinearity (INL) | Full | | ±1.5 | ±3.5 | LSB |
| TEMPERATURE DRIFT | | | | | |
| Offset Error | Full | | ±2 | | ppm/°C |
| Gain Error | Full | | ±17 | | ppm/°C |
| Reference Voltage (1 V Mode) | Full | | ±21 | | ppm/°C |
| REFERENCE | | | | | |
| Output Voltage Error (V _{REF} = 1 V) | Full | | ±5 | ±30 | mV |
| Load Regulation at 1.0 mA (V _{REF} = 1 V) | Full | | 3 | | mV |
| Input Resistance | Full | | 6 | | kΩ |
| ANALOG INPUTS | | | | | |
| Differential Input Voltage (V _{REF} = 1 V) | Full | | 2 | | V p-p |
| Common-Mode Voltage | Full | | AVDD/2 | | V |
| Differential Input Capacitance | Full | | 7 | | pF |
| Analog Bandwidth, Full Power | Full | | 315 | | MHz |
| POWER SUPPLY | | | | | |
| AVDD | Full | 1.7 | 1.8 | 1.9 | V |
| DRVDD | Full | 1.7 | 1.8 | 1.9 | V |
| I _{AVDD} | Full | | 185 | 192.5 | mA |
| I _{DRVDD} | Full | | 32.5 | 34.7 | mA |
| Total Power Dissipation (Including Output Drivers) | Full | | 392 | 409 | mW |
| Power-Down Dissipation | Full | | 2 | 4 | mW |
| Standby Dissipation ² | Full | | 72 | | mW |
| CROSSTALK | Full | | -100 | | dB |
| CROSSTALK (Overrange Condition) ³ | Full | | -100 | | dB |

¹ See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, at www.analog.com for definitions and for details on how these tests were completed.

² Can be controlled via the SPI.

³ Overage condition is specific with 6 dB of the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 2.

| Parameter ¹ | Temperature | Min | Typ | Max | Unit |
|--|-------------|------|-------|-----|------|
| SIGNAL-TO-NOISE RATIO (SNR) | | | | | |
| $f_{IN} = 2.4$ MHz | Full | | 73.5 | | dB |
| $f_{IN} = 19.7$ MHz | Full | 71.0 | 73.0 | | dB |
| $f_{IN} = 70$ MHz | Full | | 72.8 | | dB |
| SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD) | | | | | |
| $f_{IN} = 2.4$ MHz | Full | | 72.7 | | dB |
| $f_{IN} = 19.7$ MHz | Full | 70.2 | 72.2 | | dB |
| $f_{IN} = 70$ MHz | Full | | 72.0 | | dB |
| EFFECTIVE NUMBER OF BITS (ENOB) | | | | | |
| $f_{IN} = 2.4$ MHz | Full | | 11.92 | | Bits |
| $f_{IN} = 19.7$ MHz | Full | 11.5 | 11.85 | | Bits |
| $f_{IN} = 70$ MHz | Full | | 11.8 | | Bits |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) | | | | | |
| $f_{IN} = 2.4$ MHz | Full | | 84 | | dBc |
| $f_{IN} = 19.7$ MHz | Full | 73 | 84 | | dBc |
| $f_{IN} = 70$ MHz | Full | | 78 | | dBc |
| WORST HARMONIC (Second or Third) | | | | | |
| $f_{IN} = 2.4$ MHz | Full | | -88 | | dBc |
| $f_{IN} = 19.7$ MHz | Full | | -84 | -73 | dBc |
| $f_{IN} = 70$ MHz | Full | | -78 | | dBc |
| WORST OTHER (Excluding Second or Third) | | | | | |
| $f_{IN} = 2.4$ MHz | Full | | -90 | | dBc |
| $f_{IN} = 19.7$ MHz | Full | | -90 | -80 | dBc |
| $f_{IN} = 70$ MHz | Full | | -88 | | dBc |
| TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = -7.0 dBFS | | | | | |
| $f_{IN1} = 15$ MHz, $f_{IN2} = 16$ MHz | 25°C | | 80.0 | | dBc |
| $f_{IN1} = 70$ MHz, $f_{IN2} = 71$ MHz | 25°C | | 80.0 | | dBc |

¹ See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, at www.analog.com for definitions and for details on how these tests were completed.

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DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 3.

| Parameter ¹ | Temperature | Min | Typ | Max | Unit |
|---|-------------|-------|------------------|-------------|--------|
| CLOCK INPUTS (CLK+, CLK-) | | | | | |
| Logic Compliance | | | CMOS/LVDS/LVPECL | | |
| Differential Input Voltage ² | Full | 250 | | | mV p-p |
| Input Common-Mode Voltage | Full | | 1.2 | | V |
| Input Resistance (Differential) | 25°C | | 20 | | kΩ |
| Input Capacitance | 25°C | | 1.5 | | pF |
| LOGIC INPUTS (PDWN, SCLK/DTP) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | 3.6 | V |
| Logic 0 Voltage | Full | | | 0.3 | V |
| Input Resistance | 25°C | | 30 | | kΩ |
| Input Capacitance | 25°C | | 0.5 | | pF |
| LOGIC INPUT (CSB) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | 3.6 | V |
| Logic 0 Voltage | Full | | | 0.3 | V |
| Input Resistance | 25°C | | 70 | | kΩ |
| Input Capacitance | 25°C | | 0.5 | | pF |
| LOGIC INPUT (SDIO/ODM) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | DRVDD + 0.3 | V |
| Logic 0 Voltage | Full | 0 | | 0.3 | V |
| Input Resistance | 25°C | | 30 | | kΩ |
| Input Capacitance | 25°C | | 2 | | pF |
| LOGIC OUTPUT (SDIO/ODM) ³ | | | | | |
| Logic 1 Voltage (I _{OH} = 800 μA) | Full | | 1.79 | | V |
| Logic 0 Voltage (I _{OL} = 50 μA) | Full | | | 0.05 | V |
| DIGITAL OUTPUTS (D + x, D - x), (ANSI-644) | | | | | |
| Logic Compliance | | | LVDS | | |
| Differential Output Voltage (V _{OD}) | Full | 247 | | 454 | mV |
| Output Offset Voltage (V _{OS}) | Full | 1.125 | | 1.375 | V |
| Output Coding (Default) | | | Offset binary | | |
| DIGITAL OUTPUTS (D + x, D - x), (Low Power, Reduced Signal Option) | | | | | |
| Logic Compliance | | | LVDS | | |
| Differential Output Voltage (V _{OD}) | Full | 150 | | 250 | mV |
| Output Offset Voltage (V _{OS}) | Full | 1.10 | | 1.30 | V |
| Output Coding (Default) | | | Offset binary | | |

¹ See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, at www.analog.com for definitions and for details on how these tests were completed.

² This is specified for LVDS and LVPECL only.

³ This is specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 4.

| Parameter ^{1, 2} | Temp | Min | Typ | Max | Unit |
|--|------|-------------------------|-----------------------------|-------------------------|------------|
| CLOCK³ | | | | | |
| Maximum Clock Rate | Full | 50 | | | MSPS |
| Minimum Clock Rate | Full | | | 10 | MSPS |
| Clock Pulse Width High (t_{EH}) | Full | | 10 | | ns |
| Clock Pulse Width Low (t_{EL}) | Full | | 10 | | ns |
| OUTPUT PARAMETERS³ | | | | | |
| Propagation Delay (t_{PD}) | Full | 2.0 | 2.7 | 3.5 | ns |
| Rise Time (t_R) (20% to 80%) | Full | | 300 | | ps |
| Fall Time (t_F) (20% to 80%) | Full | | 300 | | ps |
| FCO Propagation Delay (t_{FCO}) | Full | 2.0 | 2.7 | 3.5 | ns |
| DCO Propagation Delay (t_{CPD}) ⁴ | Full | | $t_{FCO} + (t_{SAMPLE}/28)$ | | ns |
| DCO to Data Delay (t_{DATA}) ⁴ | Full | $(t_{SAMPLE}/28) - 300$ | $(t_{SAMPLE}/28)$ | $(t_{SAMPLE}/28) + 300$ | ps |
| DCO to FCO Delay (t_{FRAME}) ⁴ | Full | $(t_{SAMPLE}/28) - 300$ | $(t_{SAMPLE}/28)$ | $(t_{SAMPLE}/28) + 300$ | ps |
| Data to Data Skew ($t_{DATA-MAX} - t_{DATA-MIN}$) | Full | | ± 50 | ± 150 | ps |
| Wake-Up Time (Standby) | 25°C | | 600 | | ns |
| Wake-Up Time (Power-Down) | 25°C | | 375 | | μ s |
| Pipeline Latency | Full | | 8 | | CLK cycles |
| APERTURE | | | | | |
| Aperture Delay (t_A) | 25°C | | 500 | | ps |
| Aperture Uncertainty (Jitter) | 25°C | | <1 | | ps rms |
| Out-of-Range Recovery Time | 25°C | | 2 | | CLK cycles |

¹ See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, at www.analog.com for definitions and for details on how these tests were completed.

² Measured on standard FR-4 material.

³ Can be adjusted via the SPI.

⁴ $t_{SAMPLE}/28$ is based on the number of bits multiplied by 2; delays are based on half duty cycles.

TIMING DIAGRAMS

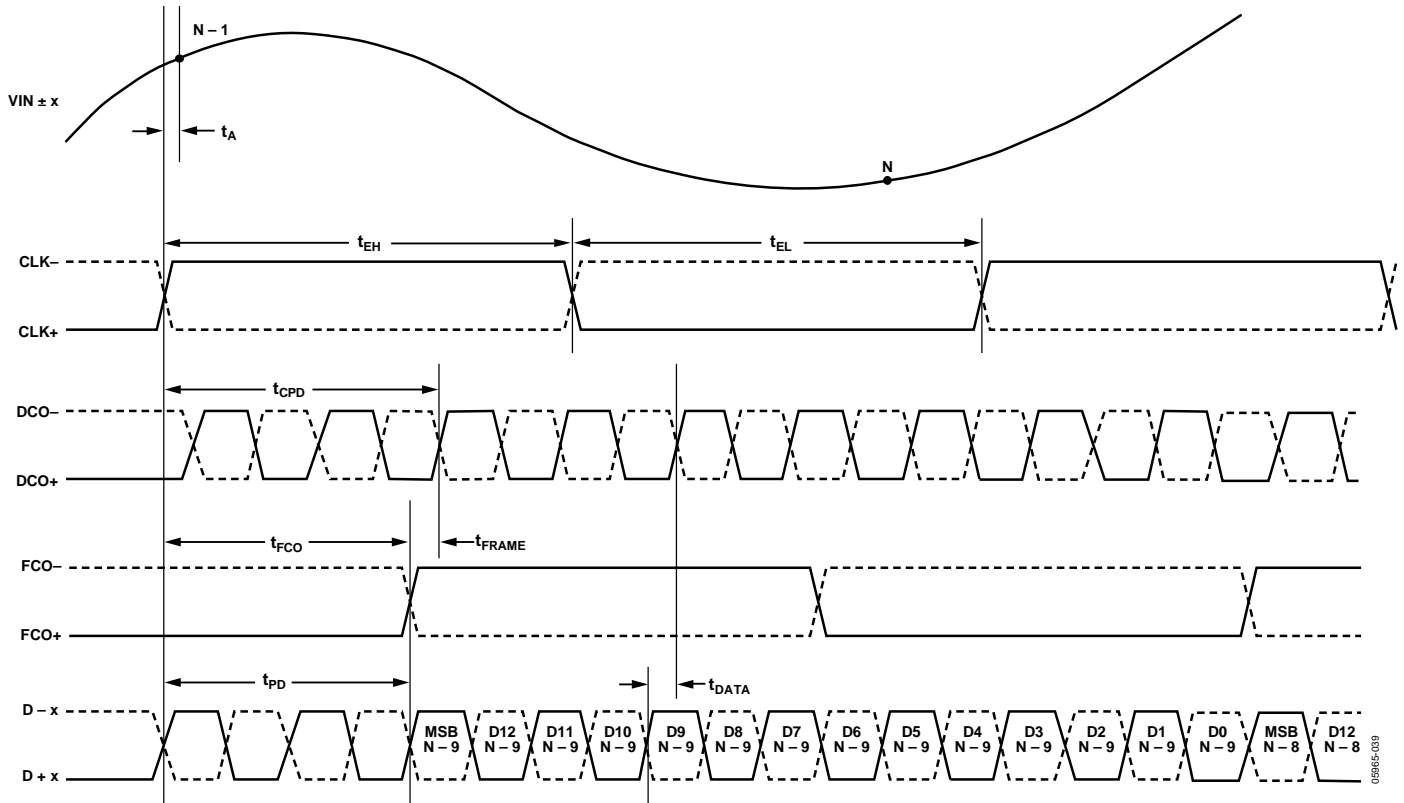


Figure 2. 14-Bit Data Serial Stream, MSB First (Default)

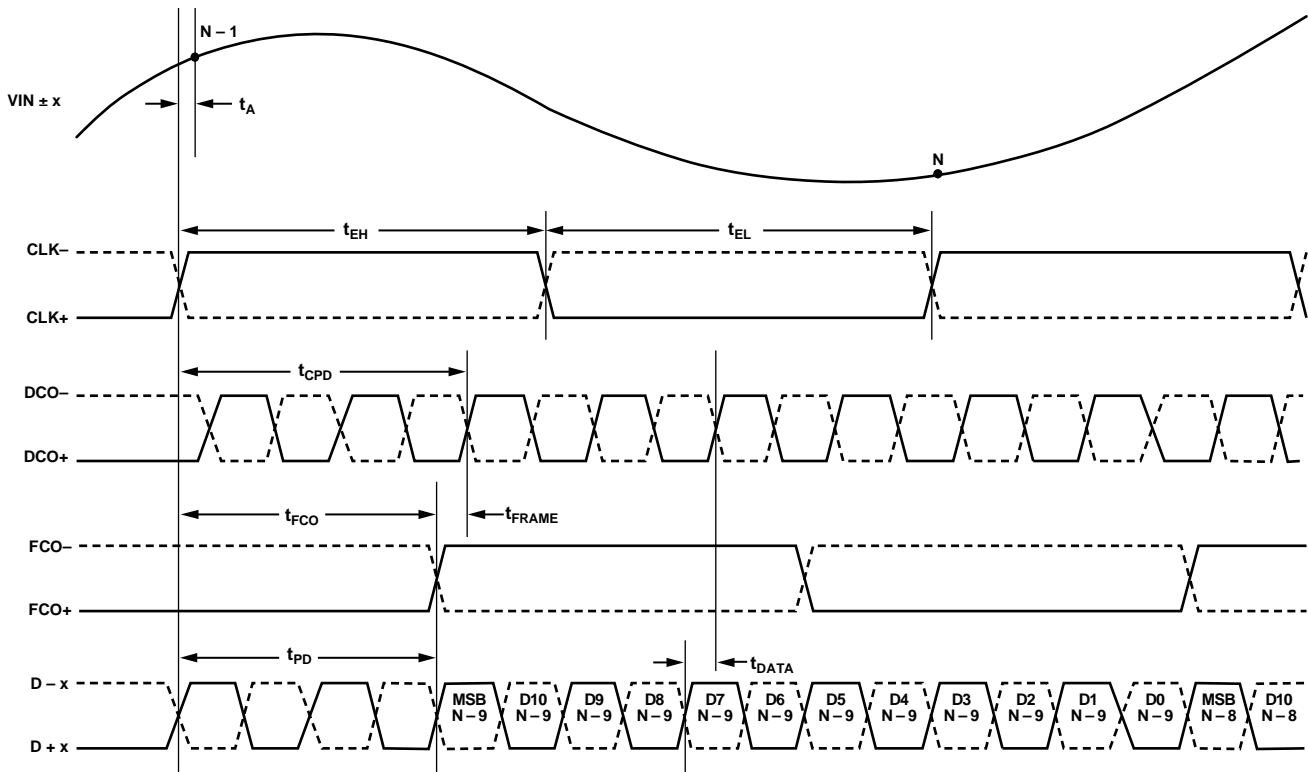


Figure 3. 12-Bit Data Serial Stream, MSB First

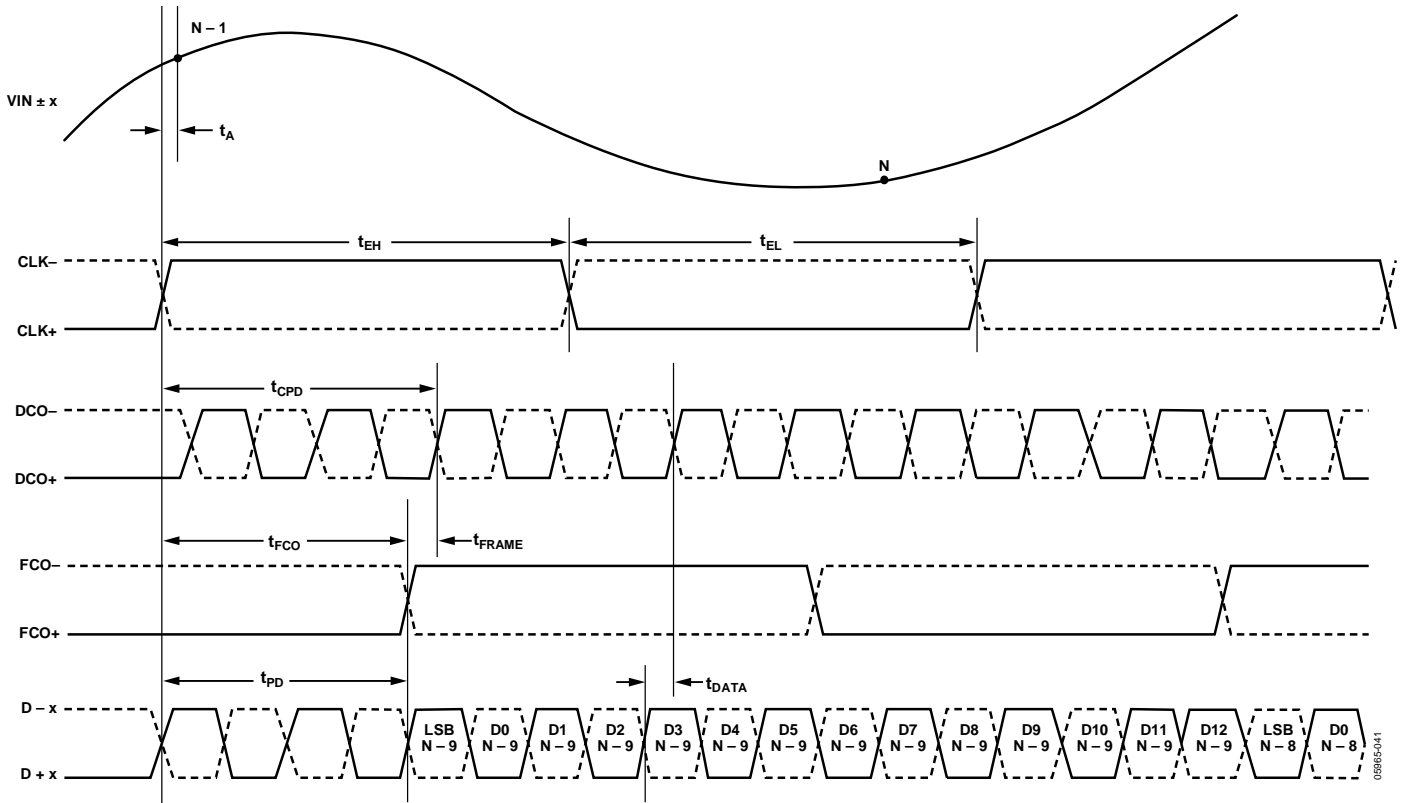


Figure 4. 14-Bit Data Serial Stream, LSB First

05985-0-11

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|---------------------------------------|------------------|
| ELECTRICAL | |
| AVDD to AGND | −0.3 V to +2.0 V |
| DRVDD to DRGND | −0.3 V to +2.0 V |
| AGND to DRGND | −0.3 V to +0.3 V |
| AVDD to DRVDD | −2.0 V to +2.0 V |
| Digital Outputs ¹ to DRGND | −0.3 V to +2.0 V |
| CLK+, CLK− to AGND | −0.3 V to +3.9 V |
| VIN + x, VIN − x to AGND | −0.3 V to +2.0 V |
| SDIO/ODM to AGND | −0.3 V to +2.0 V |
| PDWN, SCLK/DTP, CSB to AGND | −0.3 V to +3.9 V |
| REFT, REFB, RBIAS to AGND | −0.3 V to +2.0 V |
| VREF, SENSE to AGND | −0.3 V to +2.0 V |
| ENVIRONMENTAL | |
| Operating Temperature Range (Ambient) | −40°C to +85°C |
| Maximum Junction Temperature | 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Storage Temperature Range (Ambient) | −65°C to +150°C |

¹ Digital outputs include D + x, D − x, DCO+, DCO−, FCO+, FCO−.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 6.

| Air Flow Velocity (m/sec) | θ_{JA} ¹ | θ_{JB} | θ_{JC} | Unit |
|---------------------------|----------------------------|---------------|---------------|------|
| 0.0 | 24 | | | °C/W |
| 1.0 | 21 | 12.6 | 1.2 | °C/W |
| 2.5 | 19 | | | °C/W |

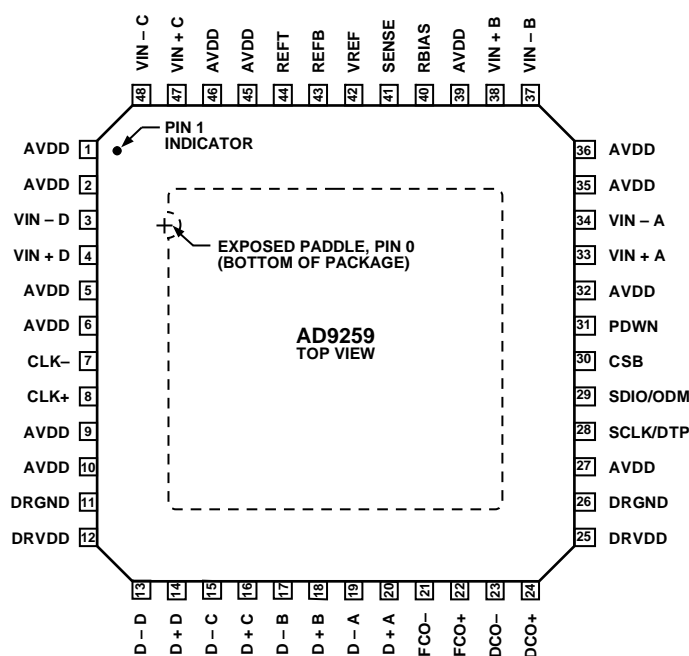
¹ θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATIONAL.

Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---|----------|------------------------------------|
| 0 | AGND | Analog Ground (Exposed Paddle) |
| 1, 2, 5, 6, 9, 10, 27, 32, 35, 36, 39, 45, 46 | AVDD | 1.8 V Analog Supply |
| 11, 26 | DRGND | Digital Output Driver Ground |
| 12, 25 | DRVDD | 1.8 V Digital Output Driver Supply |
| 3 | VIN - D | ADC D Analog Input Complement |
| 4 | VIN + D | ADC D Analog Input True |
| 7 | CLK- | Input Clock Complement |
| 8 | CLK+ | Input Clock True |
| 13 | D - D | ADC D Digital Output Complement |
| 14 | D + D | ADC D Digital Output True |
| 15 | D - C | ADC C Digital Output Complement |
| 16 | D + C | ADC C Digital Output True |
| 17 | D - B | ADC B Digital Output Complement |
| 18 | D + B | ADC B Digital Output True |
| 19 | D - A | ADC A Digital Output Complement |
| 20 | D + A | ADC A Digital Output True |
| 21 | FCO- | Frame Clock Output Complement |
| 22 | FCO+ | Frame Clock Output True |
| 23 | DCO- | Data Clock Output Complement |
| 24 | DCO+ | Data Clock Output True |
| 28 | SCLK/DTP | Serial Clock/Digital Test Pattern |
| 29 | SDIO/ODM | Serial Data I/O/Output Driver Mode |

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| Pin No. | Mnemonic | Description |
|---------|----------|---|
| 30 | CSB | Chip Select Bar |
| 31 | PDWN | Power-Down |
| 33 | VIN + A | ADC A Analog Input True |
| 34 | VIN – A | ADC A Analog Input Complement |
| 37 | VIN – B | ADC B Analog Input Complement |
| 38 | VIN + B | ADC B Analog Input True |
| 40 | RBIAS | External resistor sets the internal ADC core bias current |
| 41 | SENSE | Reference Mode Selection |
| 42 | VREF | Voltage Reference Input/Output |
| 43 | REFB | Differential Reference (Negative) |
| 44 | REFT | Differential Reference (Positive) |
| 47 | VIN + C | ADC C Analog Input True |
| 48 | VIN – C | ADC C Analog Input Complement |

EQUIVALENT CIRCUITS

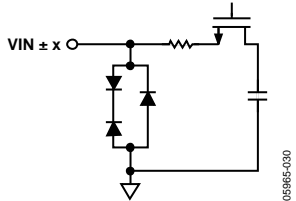


Figure 6. Equivalent Analog Input Circuit

059865-030

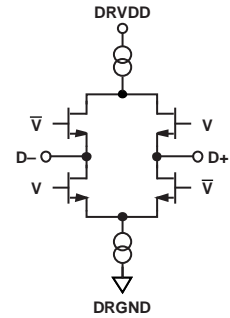


Figure 9. Equivalent Digital Output Circuit

059865-005

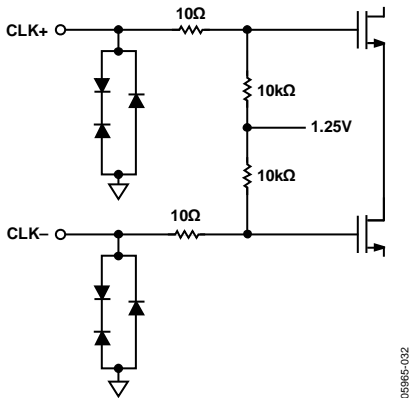


Figure 7. Equivalent Clock Input Circuit

059865-032

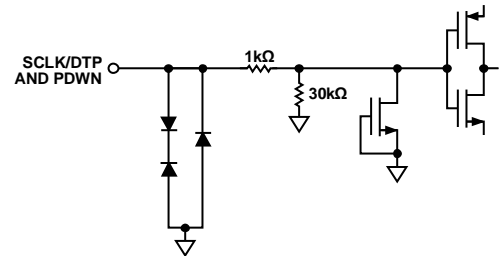


Figure 10. Equivalent SCLK/DTP and PDWN Input Circuit

059865-033

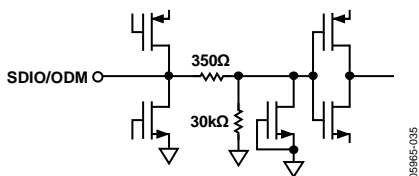


Figure 8. Equivalent SDIO/ODM Input Circuit

059865-035

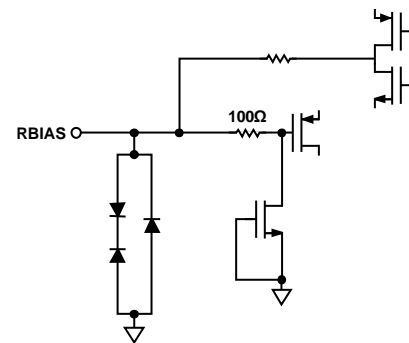


Figure 11. Equivalent RBIAS Circuit

059865-031

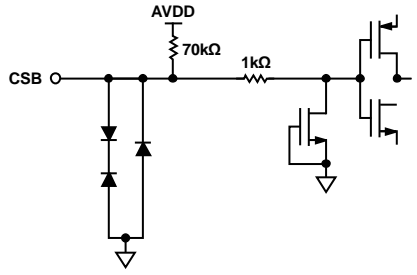


Figure 12. Equivalent CSB Input Circuit

05985-034

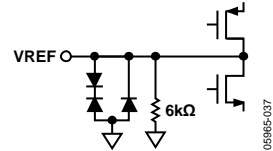


Figure 14. Equivalent VREF Circuit

05985-037

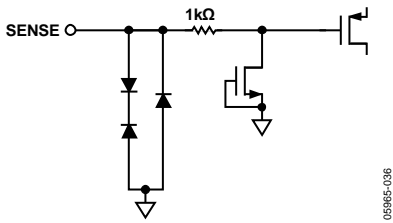


Figure 13. Equivalent SENSE Circuit

05985-036

TYPICAL PERFORMANCE CHARACTERISTICS

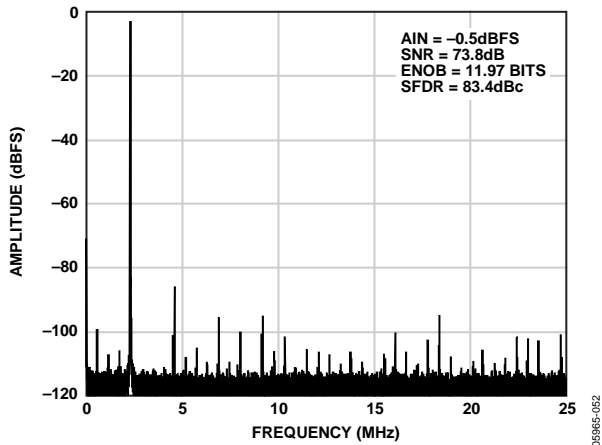


Figure 15. Single-Tone 32k FFT with $f_{IN} = 2.4$ MHz, $f_{SAMPLE} = 50$ MSPS

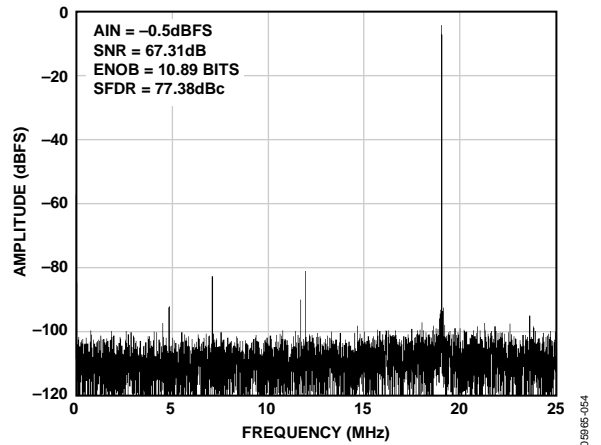


Figure 18. Single-Tone 32k FFT with $f_{IN} = 170$ MHz, $f_{SAMPLE} = 50$ MSPS

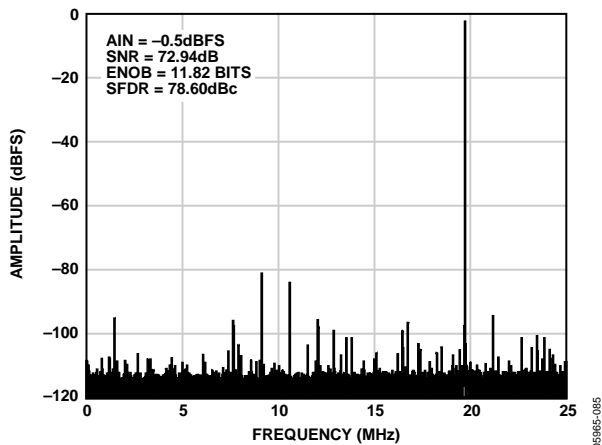


Figure 16. Single-Tone 32k FFT with $f_{IN} = 70$ MHz, $f_{SAMPLE} = 50$ MSPS

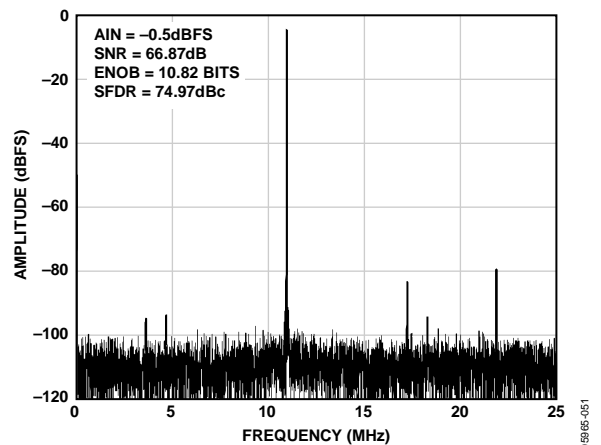


Figure 19. Single-Tone 32k FFT with $f_{IN} = 190$ MHz, $f_{SAMPLE} = 50$ MSPS

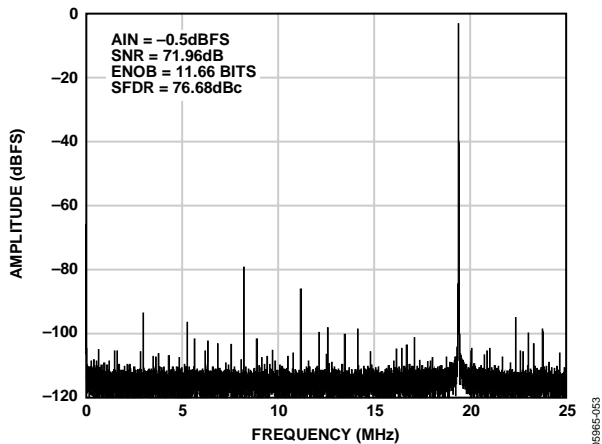


Figure 17. Single-Tone 32k FFT with $f_{IN} = 120$ MHz, $f_{SAMPLE} = 50$ MSPS

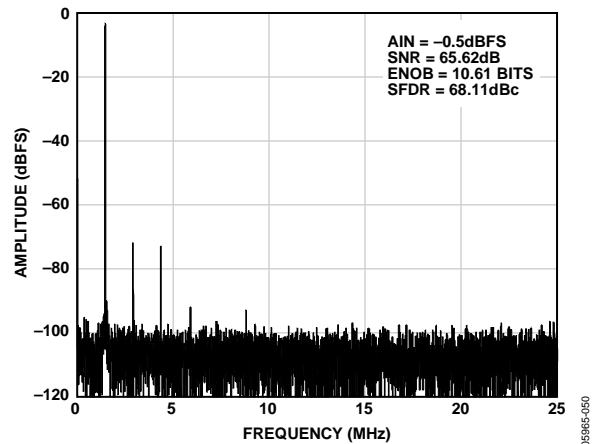


Figure 20. Single-Tone 32k FFT with $f_{IN} = 250$ MHz, $f_{SAMPLE} = 50$ MSPS

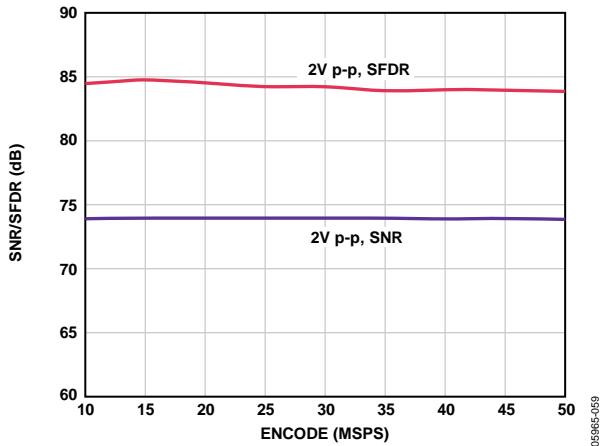


Figure 21. SNR/SFDR vs. Encode, $f_{IN} = 10.3 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

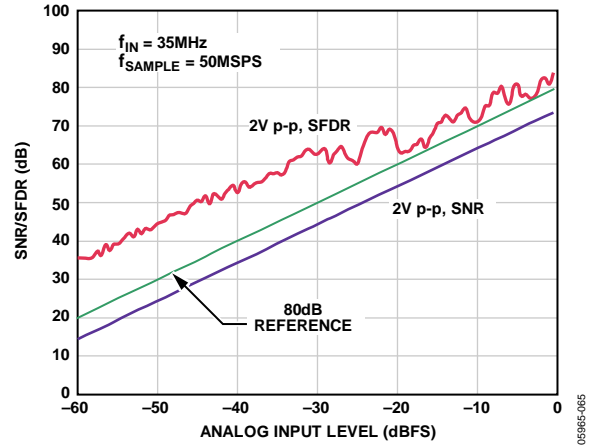


Figure 24. SNR/SFDR vs. Analog Input Level, $f_{IN} = 35 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

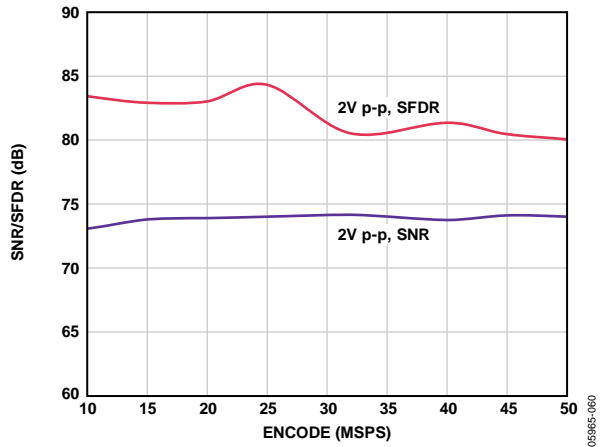


Figure 22. SNR/SFDR vs. Encode, $f_{IN} = 35 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

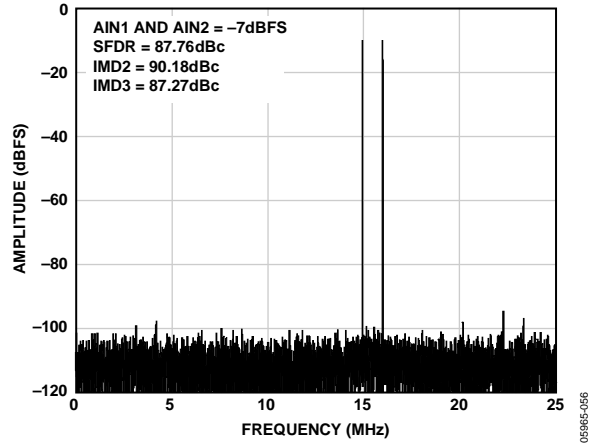


Figure 25. Two-Tone 32k FFT with $f_{IN1} = 15 \text{ MHz}$ and $f_{IN2} = 16 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

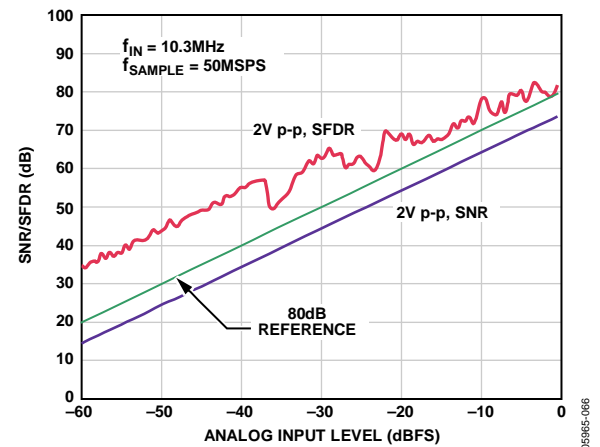


Figure 23. SNR/SFDR vs. Analog Input Level, $f_{IN} = 10.3 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

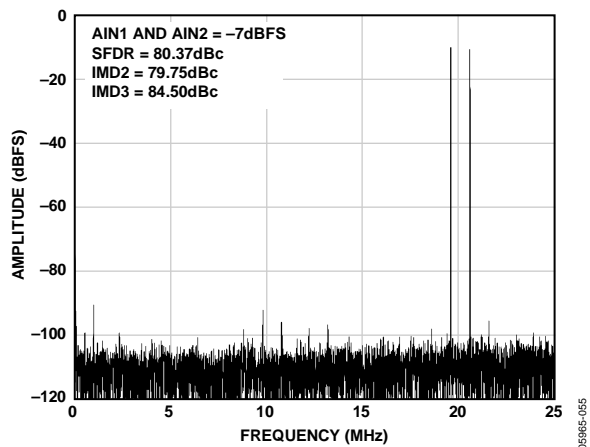


Figure 26. Two-Tone 32k FFT with $f_{IN1} = 70 \text{ MHz}$ and $f_{IN2} = 71 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

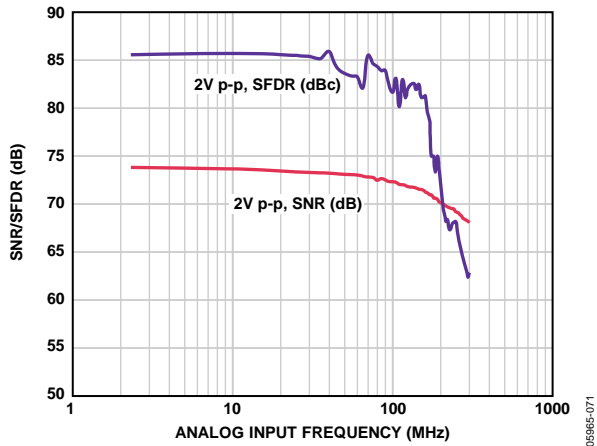


Figure 27. SNR/SFDR vs. Analog Input Frequency, $f_{SAMPLE} = 50$ MSPS

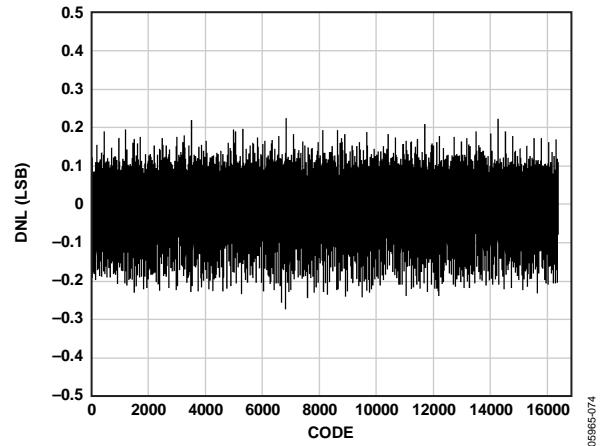


Figure 30. DNL, $f_{IN} = 2.4$ MHz, $f_{SAMPLE} = 50$ MSPS

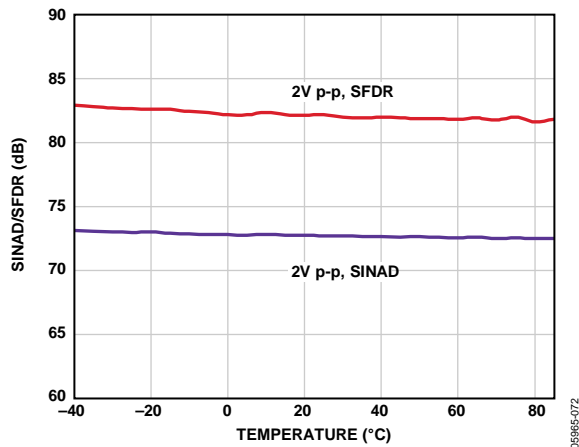


Figure 28. SINAD/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, $f_{SAMPLE} = 50$ MSPS

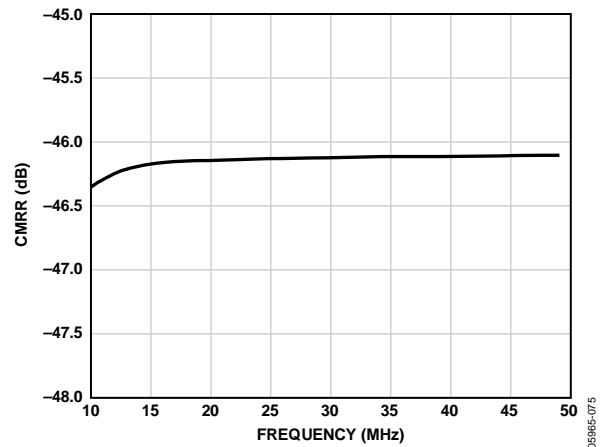


Figure 31. CMRR vs. Frequency, $f_{SAMPLE} = 50$ MSPS

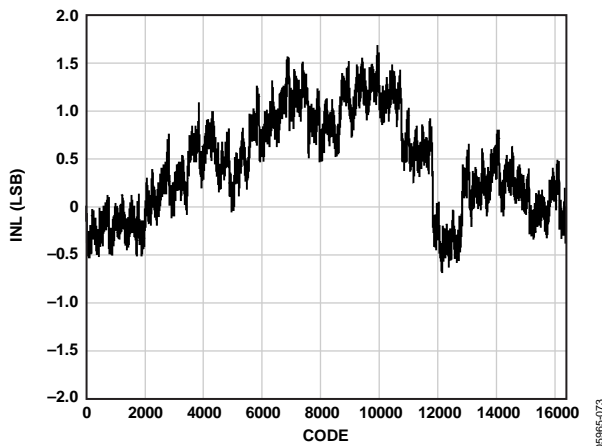


Figure 29. INL, $f_{IN} = 2.4$ MHz, $f_{SAMPLE} = 50$ MSPS

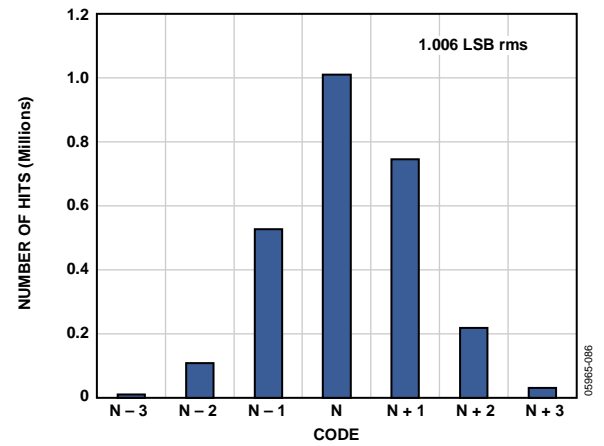


Figure 32. Input-Referred Noise Histogram, $f_{SAMPLE} = 50$ MSPS

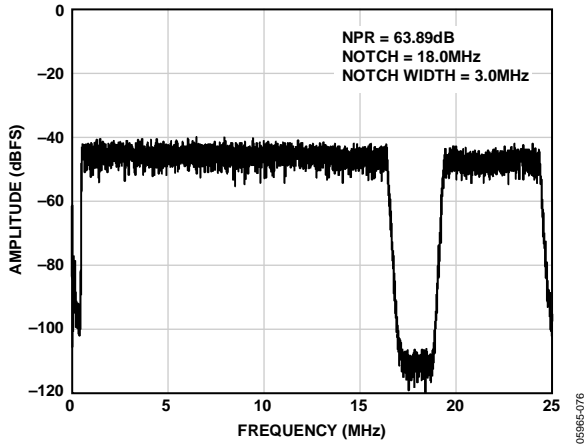


Figure 33. Noise Power Ratio (NPR), $f_{\text{SAMPLE}} = 50 \text{ MSPS}$

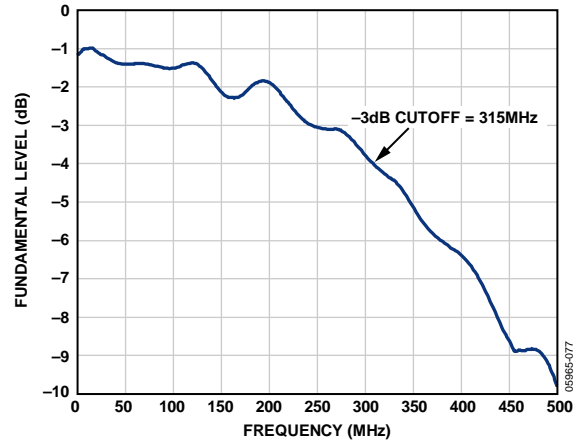


Figure 34. Full-Power Bandwidth vs. Frequency, $f_{\text{SAMPLE}} = 50 \text{ MSPS}$

THEORY OF OPERATION

The AD9259 architecture consists of a pipelined ADC divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9259 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

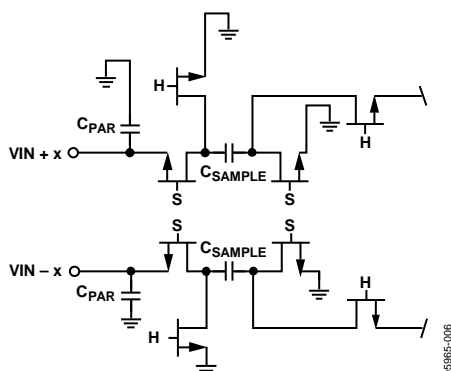


Figure 35. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 35). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low-Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of

low-Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article “Transformer-Coupled Front-End for Wideband A/D Converters” (Volume 39, April 2005) for more information at www.analog.com. In general, the precise values depend on the application.

The analog inputs of the AD9259 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 36 and Figure 37.

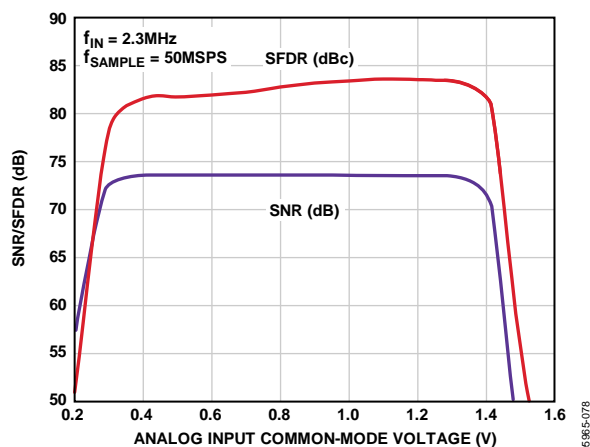


Figure 36. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 2.3 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

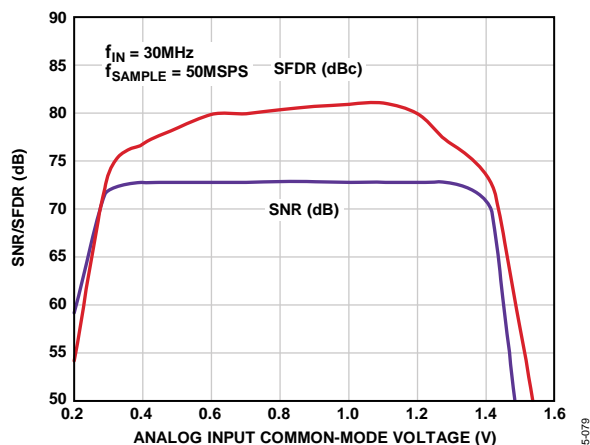


Figure 37. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 30 \text{ MHz}$, $f_{SAMPLE} = 50 \text{ MSPS}$

AD9259

For best dynamic performance, the source impedances driving $VIN + x$ and $VIN - x$ should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2 (AVDD + VREF)$$

$$REFB = 1/2 (AVDD - VREF)$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from these equations that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

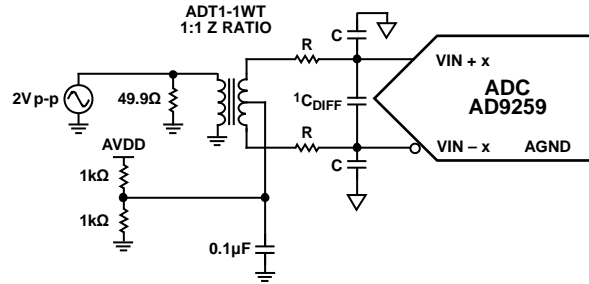
Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9259, the largest input span available is 2 V p-p.

Differential Input Configurations

There are several ways to drive the AD9259 either actively or passively; however, optimum performance is achieved by driving the analog input differentially. For example, using the AD8332 differential driver to drive the AD9259 provides excellent performance and a flexible interface to the ADC (see Figure 41) for baseband applications. This configuration is commonly used for medical ultrasound systems.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 38 and Figure 39), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9259.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.



¹C_{DIFF} IS OPTIONAL.

Figure 38. Differential Transformer-Coupled Configuration for Baseband Applications

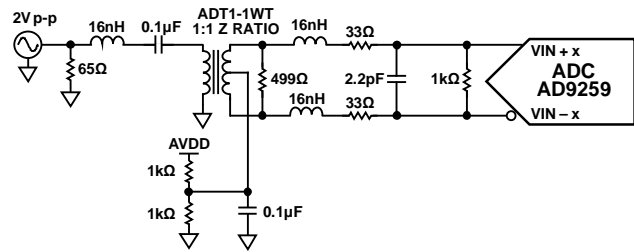
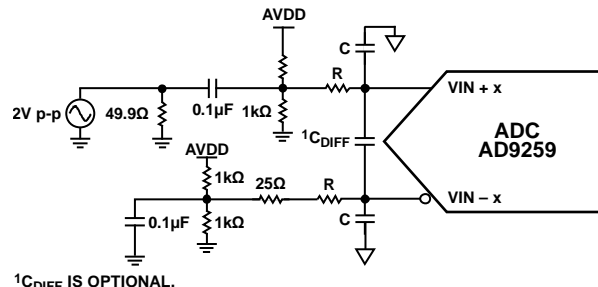


Figure 39. Differential Transformer-Coupled Configuration for IF Applications

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the application requires a single-ended input configuration, ensure that the source impedances on each input are well matched in order to achieve the best possible performance. A full-scale input of 2 V p-p can be applied to the ADC's $VIN + x$ pin while the $VIN - x$ pin is terminated. Figure 40 details a typical single-ended input configuration.



¹C_{DIFF} IS OPTIONAL.

Figure 40. Single-Ended Input Configuration

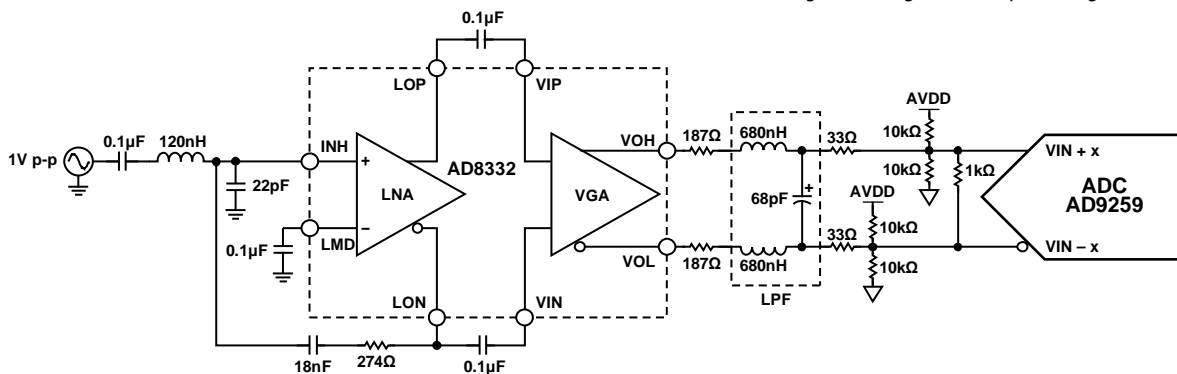


Figure 41. Differential Input Configuration Using the AD8332 with Two-Pole, 16 MHz Low-Pass Filter

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9259 sample clock inputs (CLK+ and CLK-) should be clocked with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally and require no additional biasing.

Figure 42 shows a preferred method for clocking the AD9259. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9259 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9259, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

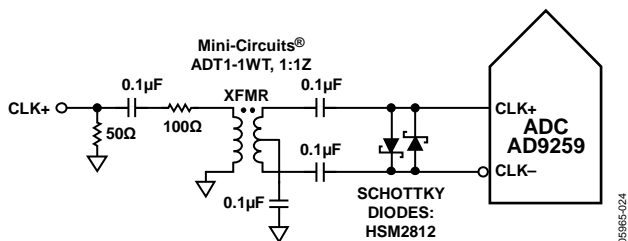


Figure 42. Transformer-Coupled Differential Clock

Another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 43. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 of clock drivers offers excellent jitter performance.

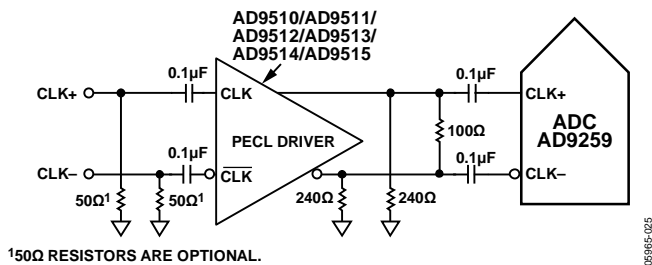


Figure 43. Differential PECL Sample Clock

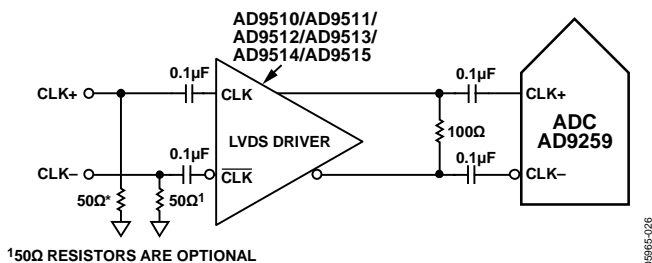


Figure 44. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK- pin should be bypassed to ground with a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 45). Although the

CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.3 V and therefore offers several selections for the drive logic voltage.

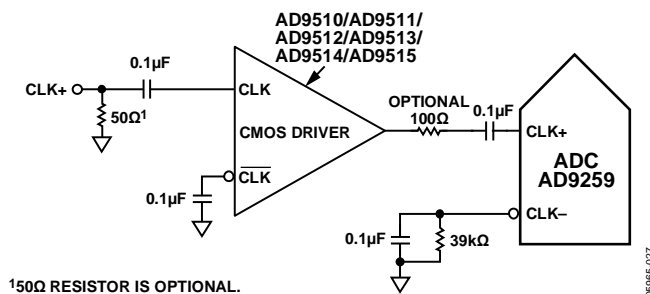


Figure 45. Single-Ended 1.8 V CMOS Sample Clock

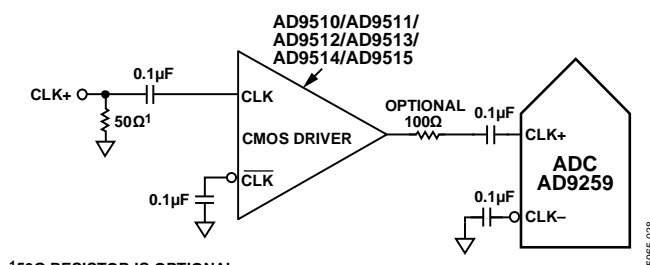


Figure 46. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9259 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9259. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the Memory Map section for more details on using this feature.

Jitter in the rising edge of the input is an important concern, and it is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz nominal. The loop has a time constant associated with it that must be considered in applications where the clock rate can change dynamically. This requires a wait time of 1.5 μs to 5 μs after a dynamic clock frequency increase (or decrease) before the DCS loop is relocked to the input signal. During the period that the loop is not locked, the DCS loop is bypassed and the internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_j) can be calculated by

$$\text{SNR Degradation} = 20 \times \log_{10}(1/2 \times \pi \times f_A \times t_j)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 47).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9259. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note and to the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs at www.analog.com.

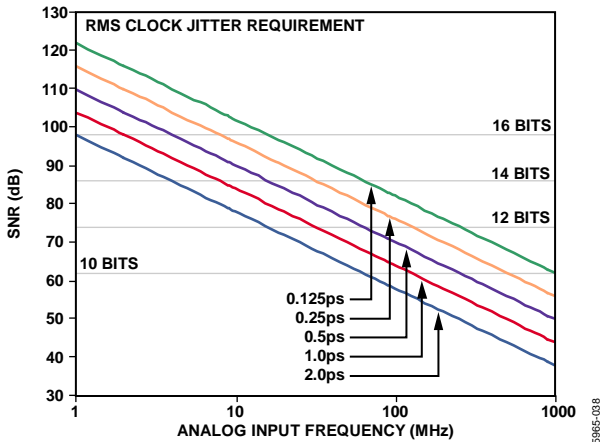


Figure 47. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 48, the power dissipated by the AD9259 is proportional to its sample rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

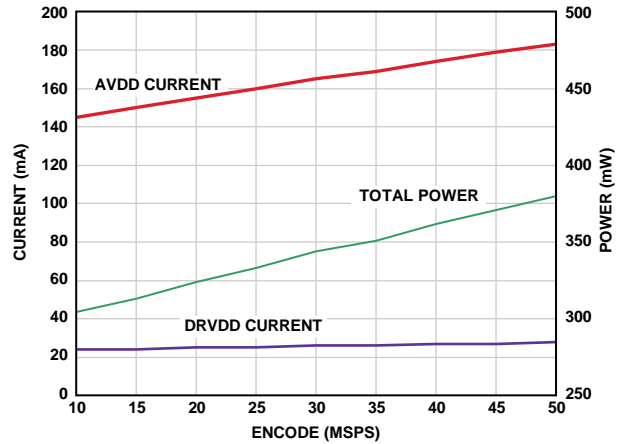


Figure 48. Supply Current vs. f_{SAMPLE} for $f_{\text{IN}} = 10.3 \text{ MHz}$, $f_{\text{SAMPLE}} = 50 \text{ MSPS}$

By asserting the PDWN pin high, the AD9259 is placed into power-down mode. In this state, the ADC typically dissipates 3 mW. During power-down, the LVDS output drivers are placed into a high impedance state. If any of the SPI features are changed before the power-down feature is enabled, the chip continues to function after PDWN is pulled low without requiring a reset. The AD9259 returns to normal operating mode when the PDWN pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode: shorter cycles result in proportionally shorter wake-up times. With the recommended 0.1 μ F and 2.2 μ F decoupling capacitors on REFT and REFB, approximately 1 sec is required to fully discharge the reference buffer decoupling capacitors and approximately 375 μ s is required to restore full operation.

There are several other power-down options available when using the SPI. The user can individually power down each channel or put the entire device into standby mode. The latter option allows the user to keep the internal PLL powered when fast wake-up times (~600 ns) are required. See the Memory Map section for more details on using these features.

Digital Outputs and Timing

The AD9259 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SDIO/ODM pin or SPI. The LVDS standard can further reduce the overall power dissipation of the device by approximately 17 mW. See the SDIO/ODM Pin section or Table 16 in the Memory Map section for more information. The LVDS driver current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9259 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor

placed as close to the receiver as possible. If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 24 inches and that the differential output traces be close together and at equal lengths. An example of the FCO and data stream with proper trace length and position is shown in Figure 49.

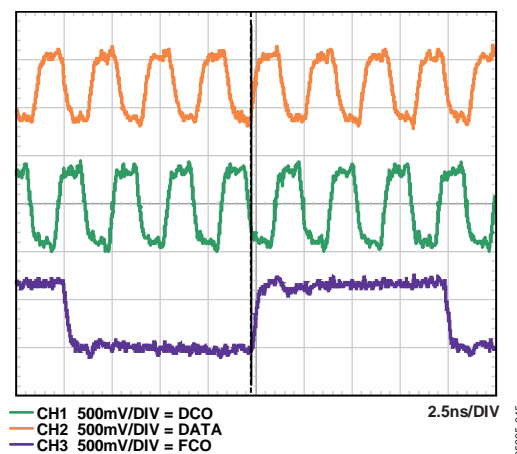


Figure 49. LVDS Output Timing Example in ANSI-644 Mode (Default)

An example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 24 inches on standard FR-4 material is shown in Figure 50. Figure 51 shows an example of trace lengths exceeding 24 inches on standard FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is the user's responsibility to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all four outputs to drive longer trace lengths (see Figure 52). Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used. In addition, notice in Figure 52 that the histogram is improved compared with that shown in Figure 51. See the Memory Map section for more details.

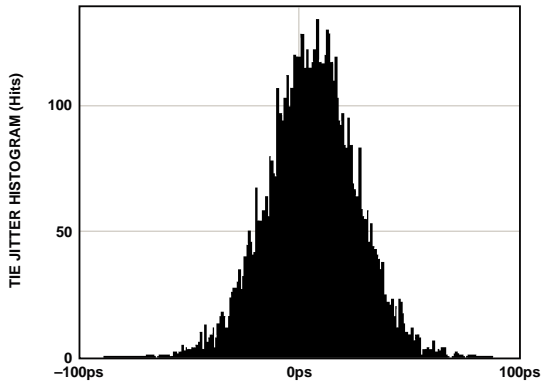
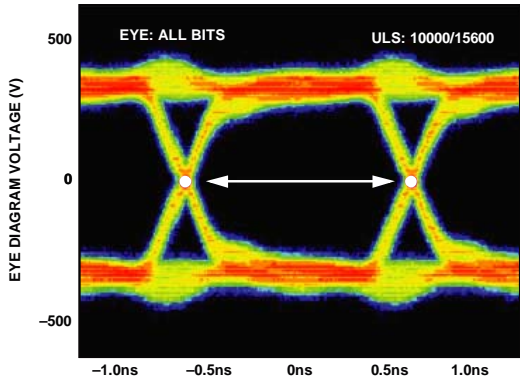


Figure 50. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Less than 24 Inches on Standard FR-4, External 100 Ω Far Termination Only

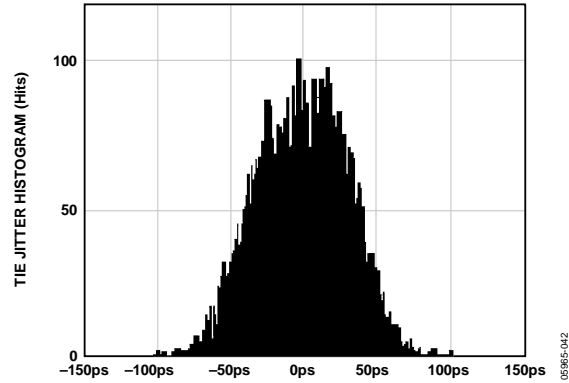
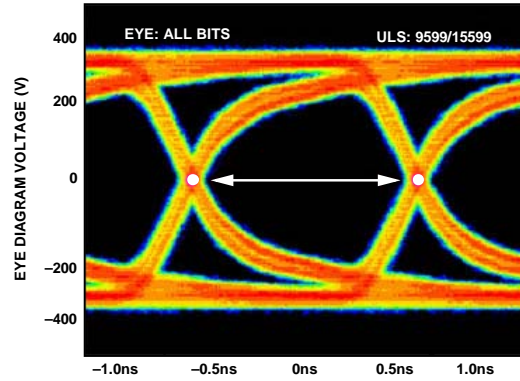


Figure 52. Data Eye for LVDS Outputs in ANSI-644 Mode with 100 Ω Internal Termination on and Trace Lengths Greater than 24 Inches on Standard FR-4, External 100 Ω Far Termination Only

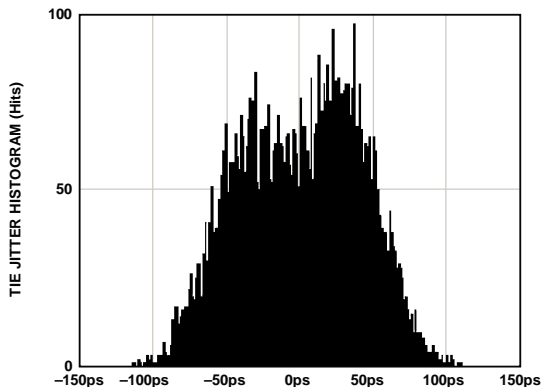
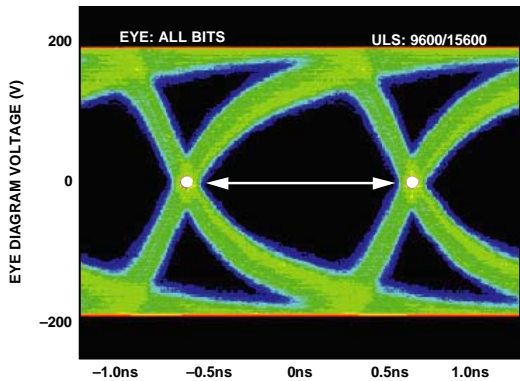


Figure 51. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater than 24 Inches on Standard FR-4, External 100 Ω Far Termination Only

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 8. To change the output data format to twos complement, see the Memory Map section.

Table 8. Digital Output Coding

| Code | $(VIN + x) - (VIN - x)$, Input Span = 2 V p-p (V) | Digital Output Offset Binary (D13 ... D0) |
|-------|---|--|
| 16383 | +1.00 | 11 1111 1111 1111 |
| 8192 | 0.00 | 10 0000 0000 0000 |
| 8191 | -0.000122 | 01 1111 1111 1111 |
| 0 | -1.00 | 00 0000 0000 0000 |

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 14 bits times the sample clock rate, with a maximum of 700 Mbps (14 bits \times 50 MSPS = 700 Mbps). The lowest typical conversion rate is 10 MSPS. However, if lower sample rates are required for a specific application, the PLL can be set up via the SPI to allow encode rates as low as 5 MSPS. See the Memory Map section for details on enabling this feature.

Two output clocks are provided to assist in capturing data from the AD9259. The DCO is used to clock the output data and is equal to seven times the sample clock (CLK) rate. Data is clocked out of the AD9259 and must be captured on the rising and falling edges of the DCO that supports double data rate

(DDR) capturing. The FCO is used to signal the start of a new output byte and is equal to the sample clock rate. See the timing diagram shown in Figure 2 for more information.

Table 9. Flexible Output Test Modes

| Output Test Mode Bit Sequence | Pattern Name | Digital Output Word 1 | Digital Output Word 2 | Subject to Data Format Select |
|-------------------------------|--------------------------------|---|---|-------------------------------|
| 0000 | Off (default) | N/A | N/A | N/A |
| 0001 | Midscale short | 1000 0000 (8-bit) 10 0000 0000 (10-bit) 1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit) | Same | Yes |
| 0010 | +Full-scale short | 1111 1111 (8-bit) 11 1111 1111 (10-bit) 1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit) | Same | Yes |
| 0011 | -Full-scale short | 0000 0000 (8-bit) 00 0000 0000 (10-bit) 0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit) | Same | Yes |
| 0100 | Checkerboard | 1010 1010 (8-bit) 10 1010 1010 (10-bit) 1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit) | 0101 0101 (8-bit) 01 0101 0101 (10-bit) 0101 0101 0101 (12-bit) 01 0101 0101 0101 (14-bit) | No |
| 0101 | PN sequence long ¹ | N/A | N/A | Yes |
| 0110 | PN sequence short ¹ | N/A | N/A | Yes |
| 0111 | One-/zero-word toggle | 1111 1111 (8-bit) 11 1111 1111 (10-bit) 1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit) | 0000 0000 (8-bit) 00 0000 0000 (10-bit) 0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit) | No |
| 1000 | User input | Register 0x19 to Register 0x1A | Register 0x1B to Register 0x1C | No |
| 1001 | 1-/0-bit toggle | 1010 1010 (8-bit) 10 1010 1010 (10-bit) 1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit) | N/A | No |
| 1010 | 1× sync | 0000 1111 (8-bit) 00 0001 1111 (10-bit) 0000 0011 1111 (12-bit) 00 0000 0111 1111 (14-bit) | N/A | No |
| 1011 | One bit high | 1000 0000 (8-bit) 10 0000 0000 (10-bit) 1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit) | N/A | No |
| 1100 | Mixed frequency | 1010 0011 (8-bit) 10 0110 0011 (10-bit) 1010 0011 0011 (12-bit) 10 1000 0110 0111 (14-bit) | N/A | No |

¹ All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins if required. The default DCO+ and DCO– timing, as shown in Figure 2, is 90° relative to the output data edge.

An 8-, 10-, or 12-bit serial stream can also be initiated from the SPI. This allows the user to implement and test compatibility with lower resolution systems. When changing the resolution to an 8-, 10-, or 12-bit serial stream, the data stream is shortened. See Figure 3 for a 12-bit example.

When the SPI is used, all of the data outputs can also be inverted from their nominal state. This is not to be confused with inverting the serial stream to an LSB-first mode. In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. However, this can be inverted so that the LSB is first in the data output serial stream (see Figure 4).

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 9 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. Note that some patterns do not adhere to the data format select option. In addition, custom user-defined test patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses. All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths to verify data capture to the receiver.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The only difference is that the starting value must be a specific value instead of all 1s (see Table 10 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The only differences are that the starting value must be a specific value instead of all 1s (see Table 10 for the initial values) and the AD9259 inverts the bit stream with relation to the ITU standard.

Table 10. PN Sequence

| Sequence | Initial Value | First Three Output Samples (MSB First) |
|-------------------|---------------|--|
| PN Sequence Short | 0x0df | 0x37e4, 0x3533, 0x0063 |
| PN Sequence Long | 0x26e028 | 0x191f, 0x35c2, 0x2359 |

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO/ODM Pin

The SDIO/ODM pin is for use in applications that do not require SPI mode operation. This pin can enable a low power, reduced signal option (similar to the IEEE 1596.3 reduced range link output standard) if it and the CSB pin are tied to AVDD during device power-up. This option should only be used when the digital output trace lengths are less than 2 inches from the LVDS receiver. When this option is used, the FCO, DCO, and outputs function normally, but the LVDS signal swing of all channels is reduced from 350 mV p-p to 200 mV p-p, allowing the user to further reduce the power on the DRVDD supply.

For applications where this pin is not used, it should be tied low. In this case, the device pin can be left open, and the 30 kΩ internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant. If applications require this pin to be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

Table 11. Output Driver Mode Pin Settings

| Selected ODM | ODM Voltage | Resulting Output Standard | Resulting FCO and DCO |
|------------------|---------------|----------------------------------|----------------------------------|
| Normal Operation | 10 kΩ to AGND | ANSI-644 (default) | ANSI-644 (default) |
| ODM | AVDD | Low power, reduced signal option | Low power, reduced signal option |

SCLK/DTP Pin

The SCLK/DTP pin is for use in applications that do not require SPI mode operation. This pin can enable a single digital test pattern if it and the CSB pin are held high during device power-up. When SCLK/DTP is tied to AVDD, the ADC channel outputs shift out the following pattern: 10 0000 0000 0000. The FCO and DCO function normally while all channels shift out the repeatable test pattern. This pattern allows the user to perform timing alignment adjustments among the FCO, DCO, and output data. For normal operation, this pin should be tied to AGND through a 10 k Ω resistor. This pin is both 1.8 V and 3.3 V tolerant.

Table 12. Digital Test Pattern Pin Settings

| Selected DTP | DTP Voltage | Resulting D + x and D - x | Resulting FCO and DCO |
|------------------|-----------------------|---------------------------|-----------------------|
| Normal Operation | 10 k Ω to AGND | Normal operation | Normal operation |
| DTP | AVDD | 10 0000 0000 0000 | Normal operation |

Additional and custom test patterns can also be observed when commanded from the SPI port. Consult the Memory Map section for information about the options available.

CSB Pin

The CSB pin should be tied to AVDD for applications that do not require SPI mode operation. By tying CSB high, all SCLK and SDIO information is ignored. This pin is both 1.8 V and 3.3 V tolerant.

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor (nominally equal to 10.0 k Ω) to ground at the RBIAS pin. The resistor current is derived on-chip and sets the AVDD current of the ADC to a nominal 185 mA at 50 MSPS. Therefore, it is imperative that at least a 1% tolerance on this resistor be used to achieve consistent performance.

Voltage Reference

A stable, accurate 0.5 V voltage reference is built into the AD9259. This is gained up internally by a factor of 2, setting V_{REF} to 1.0 V, which results in a full-scale differential input span of 2 V p-p. The V_{REF} is set internally by default; however, the VREF pin can be driven externally with a 1.0 V reference to improve accuracy.

When applying the decoupling capacitors to the VREF, REFT, and REFB pins, use ceramic low ESR capacitors. These capacitors should be close to the ADC pins and on the same layer of the PCB as the AD9259. The recommended capacitor values and configurations for the AD9259 reference pin are shown in Figure 53.

Table 13. Reference Settings

| Selected Mode | SENSE Voltage | Resulting VREF (V) | Resulting Differential Span (V p-p) |
|-----------------------|---------------|--------------------|-------------------------------------|
| External Reference | AVDD | N/A | 2 \times external reference |
| Internal, 2 V p-p FSR | AGND to 0.2 V | 1.0 | 2.0 |

Internal Reference Operation

A comparator within the AD9259 detects the potential at the SENSE pin and configures the reference. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 53), setting VREF to 1 V.

The REFT and REFB pins establish the input span of the ADC core from the reference configuration. The analog input full-scale range of the ADC equals twice the voltage of the reference pin for either an internal or an external reference configuration.

If the reference of the AD9259 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 55 depicts how the internal reference voltage is affected by loading.

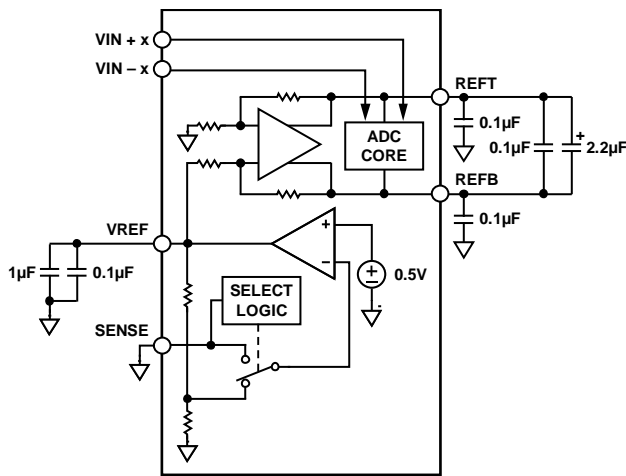
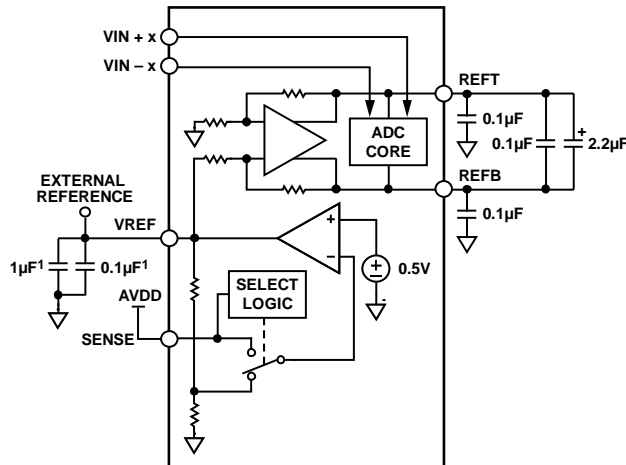


Figure 53. Internal Reference Configuration

05965-010



¹OPTIONAL.

Figure 54. External Reference Operation

05965-046

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. Figure 56 shows the typical drift characteristics of the internal reference in 1 V mode.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. The external reference is loaded with an equivalent 6 kΩ load. An internal reference buffer generates the positive and negative full-scale references, REFT and REFB, for the ADC core. Therefore, the external reference must be limited to a nominal 1.0 V.

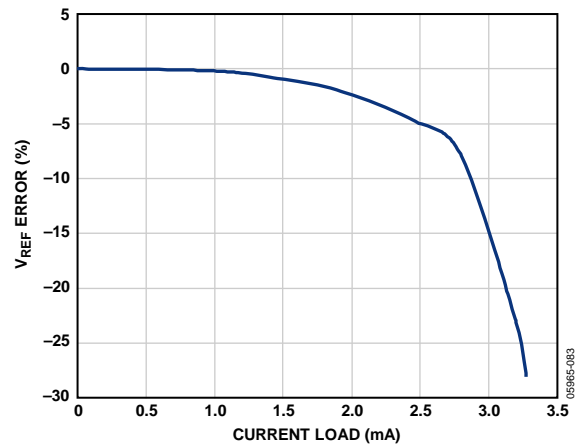


Figure 55. VREF Accuracy vs. Load

05965-083

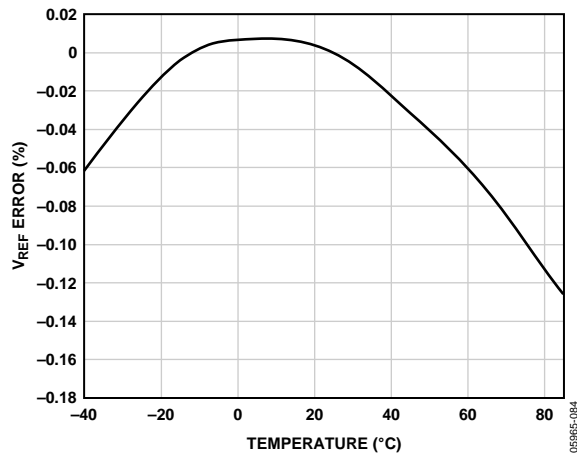


Figure 56. Typical VREF Drift

05965-084

SERIAL PORT INTERFACE (SPI)

The AD9259 serial port interface allows the user to configure the converter for specific functions or operations through a structured register space provided in the ADC. This may provide the user with additional flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. Detailed operational information can be found in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI* at www.analog.com.

There are three pins that define the SPI: SCLK, SDIO, and CSB (see Table 14). The SCLK pin is used to synchronize the read and write data presented to the ADC. The SDIO pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 14. Serial Port Pins

| Pin | Function |
|------|--|
| SCLK | Serial Clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes. |
| SDIO | Serial Data Input/Output. A dual-purpose pin. The typical role for this pin is as an input or output, depending on the instruction sent and the relative position in the timing frame. |
| CSB | Chip Select Bar (Active Low). This control gates the read and write cycles. |

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. An example of the serial timing and its definitions can be found in Figure 58 and Table 15. During normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDIO to obtain instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until CSB is taken high to end the communication cycle. This allows complete memory transfers without requiring additional instructions. Regardless of the mode, if CSB is taken high in the middle of a byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port configuration influences how the AD9259 operates. For applications that do not require a control port, the CSB line can be tied and held high. This places the remainder of the SPI pins into their secondary modes, as defined in the SDIO/ODM Pin and SCLK/DTP Pin sections. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDIO are the only pins required for communication. Although the device is synchronized during power-up, the user should ensure that the serial port remains synchronized with the CSB line when using this mode. When operating in 2-wire mode, it is recommended to use a 1-, 2-, or 3-byte transfer exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI* at www.analog.com.

HARDWARE INTERFACE

The pins described in Table 14 compose the physical interface between the user's programming device and the serial port of the AD9259. The SCLK and CSB pins function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

If multiple SDIO pins share a common connection, care should be taken to ensure that proper V_{OH} levels are met. Assuming the same load for each AD9259, Figure 57 shows the number of SDIO pins that can be connected together and the resulting V_{OH} level. This interface is flexible enough to be controlled by either serial PROMS or PIC microcontrollers, providing the user with an alternative method, other than a full SPI controller, to program the ADC (see the AN-812 Application Note).

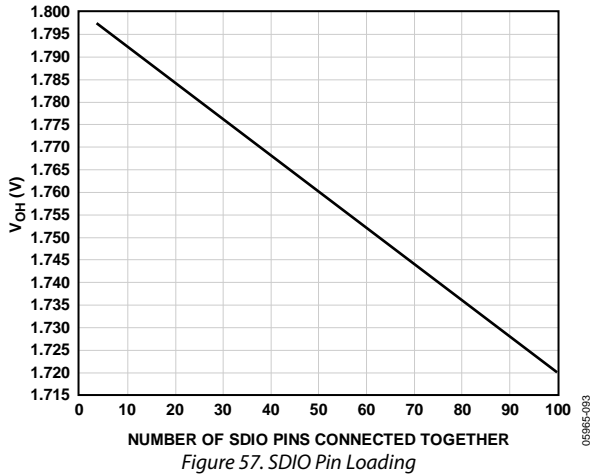


Figure 57. SDIO Pin Loading

If the user chooses not to use the SPI, these dual-function pins serve their secondary functions when the CSB is strapped to AVDD during device power-up. See the Theory of Operation section for details on which pin-strappable functions are supported on the SPI pins.

For users who wish to operate the ADC without using the SPI, remove any connections from the CSB, SCLK/DTP, and SDIO/ODM pins. By disconnecting these pins from the control bus, the ADC can function in its most basic operation. Each of these pins has an internal termination that floats to its respective level.

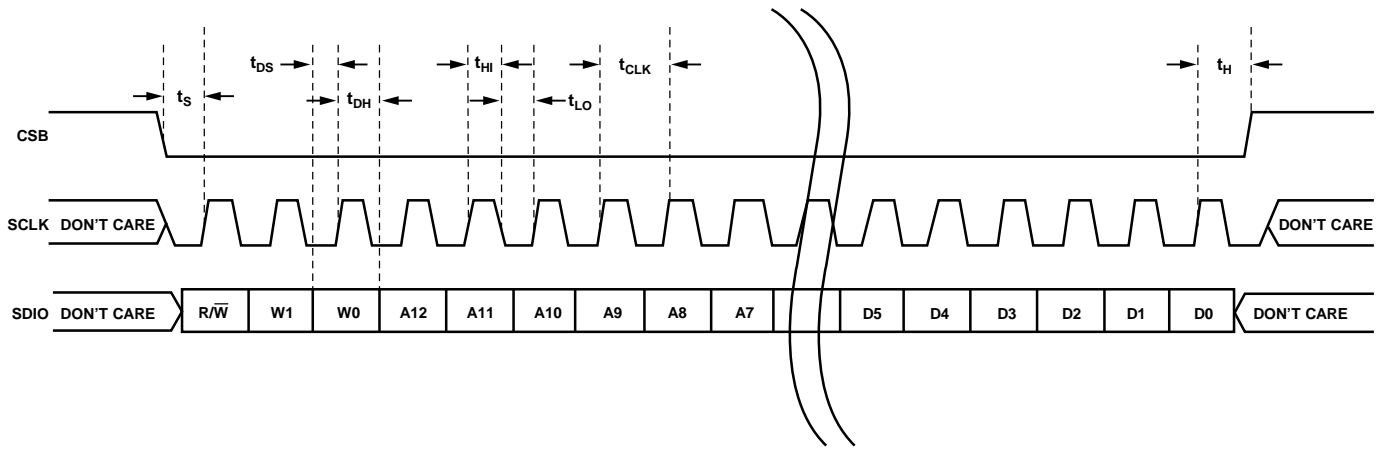


Figure 58. Serial Timing Details

Table 15. Serial Timing Definitions

| Parameter | Timing (Minimum, ns) | Description |
|-----------------|----------------------|---|
| t_{DS} | 5 | Setup time between the data and the rising edge of SCLK |
| t_{DH} | 2 | Hold time between the data and the rising edge of SCLK |
| t_{CLK} | 40 | Period of the clock |
| t_s | 5 | Setup time between CSB and SCLK |
| t_H | 2 | Hold time between CSB and SCLK |
| t_{HI} | 16 | Minimum period that SCLK should be in a logic high state |
| t_{LO} | 16 | Minimum period that SCLK should be in a logic low state |
| t_{EN_SDIO} | 10 | Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 58) |
| t_{DIS_SDIO} | 10 | Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 58) |

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map register table (Table 16) has eight address locations. The memory map is divided into three sections: the chip configuration register map (Address 0x00 to Address 0x02), the device index and transfer register map (Address 0x05 and Address 0xFF), and the ADC functions register map (Address 0x08 to Address 0x22).

The leftmost column of the memory map indicates the register address number, and the default value is shown in the second rightmost column. The (MSB) Bit 7 column is the start of the default hexadecimal value given. For example, Address 0x09, the clock register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 6 of this address followed by a 0x01 in Register 0xFF (transfer bit), the duty cycle stabilizer turns off. It is important to follow each writing sequence with a transfer bit to update the SPI registers. For more information on this and other functions, consult the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI* at www.analog.com.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

When the AD9259 comes out of a reset, critical registers are preloaded with default values. These values are indicated in Table 16, where an X refers to an undefined feature.

LOGIC LEVELS

An explanation of various registers follows: “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly, “clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

AD9259

Table 16. Memory Map Register

| Addr. (Hex) | Register Name | (MSB) Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | (LSB) Bit 0 | Default Value (Hex) | Default Notes/Comments | |
|-------------------------------------|------------------|--|--|---|--|---|---|--|---|---------------------|--|--|
| Chip Configuration Registers | | | | | | | | | | | | |
| 00 | chip_port_config | 0 | LSB first 1 = on 0 = off (default) | Soft reset 1 = on 0 = off (default) | 1 | 1 | Soft reset 1 = on 0 = off (default) | LSB first 1 = on 0 = off (default) | 0 | 0x18 | The nibbles should be mirrored so that LSB- or MSB-first mode is set correctly regardless of shift mode. | |
| 01 | chip_id | 8-bit Chip ID Bits [7:0] (AD9259 = 0x04), (default) | | | | | | | | 0x04 | Default is unique chip ID. This is a read-only register. | |
| 02 | chip_grade | X | Child ID [6:4] (identify device variants of Chip ID) 100 = 50 MSPS | | | X | X | X | X | | | Child ID used to differentiate graded devices. This is a read-only register. |
| Device Index and Transfer Registers | | | | | | | | | | | | |
| 05 | device_index_A | X | X | Clock channel DCO 1 = on 0 = off (default) | Clock channel FCO 1 = on 0 = off (default) | Data Channel D 1 = on (default) 0 = off | Data Channel C 1 = on (default) 0 = off | Data Channel B 1 = on (default) 0 = off | Data Channel A 1 = on (default) 0 = off | 0x0F | Bits are set to determine which on-chip device receives the next write command. | |
| FF | device_update | X | X | X | X | X | X | X | SW transfer 1 = on 0 = off (default) | 0x00 | Synchronously transfers data from the master shift register to the slave. | |
| ADC Functions | | | | | | | | | | | | |
| 08 | modes | X | X | X | X | X | Internal power-down mode 000 = chip run (default) 001 = full power-down 010 = standby 011 = reset | | | 0x00 | Determines various generic modes of chip operation. | |
| 09 | clock | X | X | X | X | X | X | X | Duty cycle stabilizer 1 = on (default) 0 = off | 0x01 | Turns the internal duty cycle stabilizer on and off. | |
| 0D | test_io | User test mode 00 = off (default) 01 = on, single alternate 10 = on, single once 11 = on, alternate once | | Reset PN long gen 1 = on 0 = off (default) | Reset PN short gen 1 = on 0 = off (default) | Output test mode—see Table 9 in the Digital Outputs and Timing section 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = -FS short 0100 = checkerboard output 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = 1-/0-word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency (format determined by output_mode) | | | | 0x00 | When this register is set, the test data is placed on the output pins in place of normal data. | |

| Addr. (Hex) | Register Name | (MSB) Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | (LSB) Bit 0 | Default Value (Hex) | Default Notes/Comments |
|-------------|----------------|--|---|--|-------|---|---|--|---|---------------------|--|
| 14 | output_mode | X | 0 = LVDS ANSI-644 (default) 1 = LVDS low power (IEEE 1596.3 similar) | X | X | X | Output invert 1 = on 0 = off (default) | 00 = offset binary (default) 01 = twos complement | | 0x00 | Configures the outputs and the format of the data. |
| 15 | output_adjust | X | X | Output driver termination 00 = none (default) 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω | | X | X | X | X | 0x00 | Determines LVDS or other output properties. Primarily functions to set the LVDS span and common-mode levels in place of an external resistor. |
| 16 | output_phase | X | X | X | X | 0011 = output clock phase adjust (0000 through 1010) 0000 = 0° relative to data edge 0001 = 60° relative to data edge 0010 = 120° relative to data edge 0011 = 180° relative to data edge (default) 0101 = 300° relative to data edge 0110 = 360° relative to data edge 1000 = 480° relative to data edge 1001 = 540° relative to data edge 1010 = 600° relative to data edge 1011 to 1111 = 660° relative to data edge | | | | 0x03 | On devices that utilize global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected. |
| 19 | user_patt1_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User-defined pattern, 1 LSB. |
| 1A | user_patt1_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User-defined pattern, 1 MSB. |
| 1B | user_patt2_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User-defined pattern, 2 LSB. |
| 1C | user_patt2_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User-defined pattern, 2 MSB. |
| 21 | serial_control | LSB first 1 = on 0 = off (default) | X | X | X | <10 MSPS, low encode rate mode 1 = on 0 = off (default) | 000 = 14 bits (default, normal bit stream) 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 14 bits | | | 0x00 | Serial stream control. Default causes MSB first and the native bit stream (global). |
| 22 | serial_ch_stat | X | X | X | X | X | X | Channel output reset 1 = on 0 = off (default) | Channel power-down 1 = on 0 = off (default) | 0x00 | Used to power down individual sections of a converter (local). |

Power and Ground Recommendations

When connecting power to the AD9259, it is recommended that two separate 1.8 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one supply is available, it should be routed to the AVDD first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts, with minimal trace lengths.

A single PC board ground plane should be sufficient when using the AD9259. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance can be easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9259. An exposed continuous copper plane on the PCB should mate to the AD9259 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 59 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)* at www.analog.com.

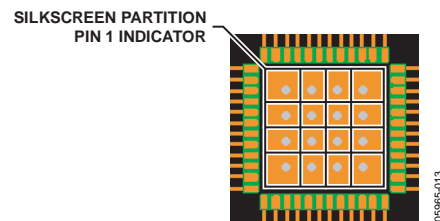


Figure 59. Typical PCB Layout

EVALUATION BOARD

The AD9259 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially using a transformer (default) or a [AD8332](#) driver. The ADC can also be driven in a single-ended fashion. Separate power pins are provided to isolate the DUT from the drive circuitry of the AD8332. Each input configuration can be selected by changing the connection of various jumpers (see Figure 62 to Figure 66). Figure 60 shows the typical bench characterization setup used to evaluate the ac performance of the AD9259. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 62 to Figure 70 for the complete schematics and layout diagrams demonstrating the routing and grounding techniques that should be applied at the system level.

POWER SUPPLIES

This evaluation board has a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The other end of the supply is a 2.1 mm inner diameter jack that connects to the PCB at P503. Once on the PC board, the 6 V supply is fused and conditioned before connecting to three low dropout linear regulators that supply the proper bias to each of the various sections on the board.

When operating the evaluation board in a nondefault condition, L504 to L507 can be removed to disconnect the switching power supply. This enables the user to bias each section of the board individually. Use P501 to connect a different supply for

each section. At least one 1.8 V supply is needed for AVDD_DUT and DRVDD_DUT; however, it is recommended that separate supplies be used for analog and digital signals and that each supply have a current capability of 1 A. To operate the evaluation board using the VGA option, a separate 5.0 V analog supply (AVDD_5 V) is needed. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply (AVDD_3.3 V) is needed in addition to the other supplies.

INPUT SIGNALS

When connecting the clock and analog source to the evaluation board, use clean signal generators with low phase noise, such as Rohde & Schwarz SMA or HP8644 signal generators or the equivalent, as well as a 1 m, shielded, RG-58, 50 Ω coaxial cable. Enter the desired frequency and amplitude from the ADC specifications tables. Typically, most Analog Devices, Inc., evaluation boards can accept approximately 2.8 V p-p or 13 dBm sine wave input for the clock. When connecting the analog input source, it is recommended to use a multipole, narrow-band, band-pass filter with 50 Ω terminations. Good choices of such band-pass filters are available from TTE, Allen Avionics, and K&L Microwave, Inc. The filter should be connected directly to the evaluation board if possible.

OUTPUT SIGNALS

The default setup uses the Analog Devices HSC-ADC-FPGA-4/ HSC-ADC-FPGA-8 high speed deserialization board to deserialize the digital output data and convert it to parallel CMOS. These two channels interface directly with the Analog Devices standard dual-channel FIFO data capture board (HSC-ADC-EVALB-DC). Two of the four channels can then be evaluated at the same time. For more information on the channel settings and optional settings of these boards, visit www.analog.com/FIFO.

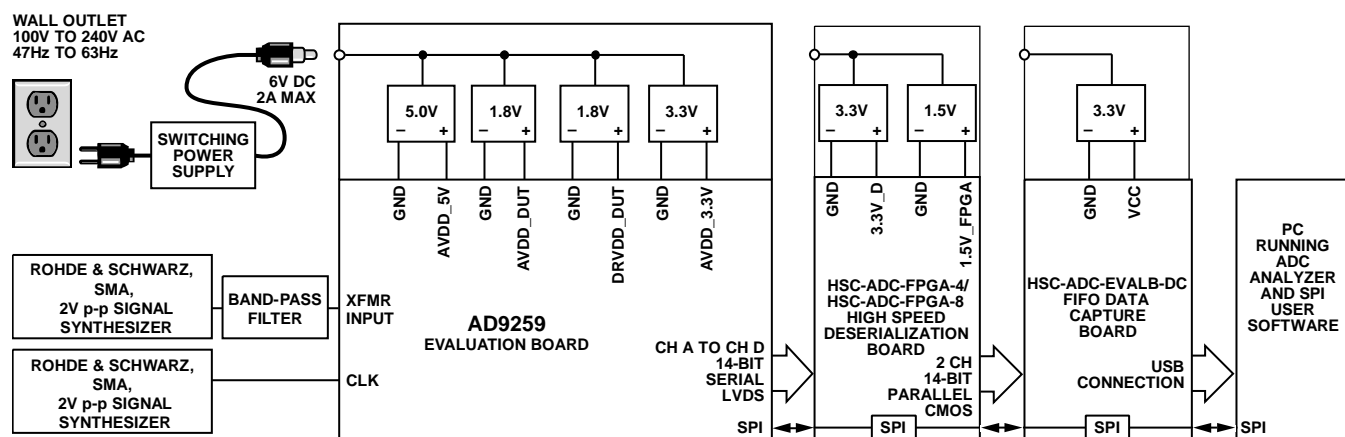


Figure 60. Evaluation Board Connection

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

The following is a list of the default and optional settings or modes allowed on the AD9259 Rev. A evaluation board.

- **POWER:** Connect the switching power supply that is provided in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P503.
- **AIN:** The evaluation board is set up for a transformer-coupled analog input with an optimum 50 Ω impedance match of 200 MHz of bandwidth (see Figure 61). For more bandwidth response, the differential capacitor across the analog inputs can be changed or removed. The common mode of the analog inputs is developed from the center tap of the transformer or AVDD_DUT/2.

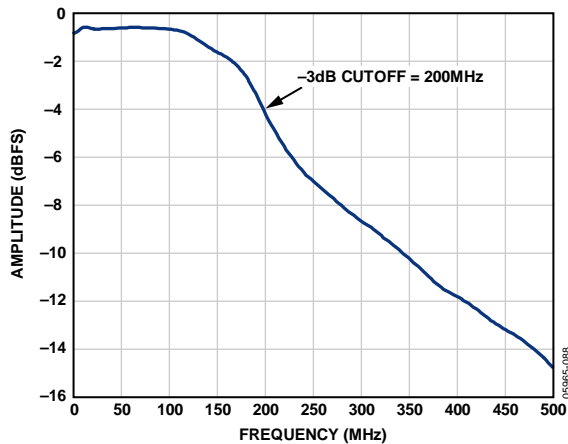


Figure 61. Evaluation Board Full-Power Bandwidth

- **VREF:** VREF is set to 1.0 V by tying the SENSE pin to ground, R237. This causes the ADC to operate in 2.0 V p-p full-scale range. A separate external reference option using the [ADR510](#) or [ADR520](#) is also included on the evaluation board. Populate R231 and R235 and remove C214. Proper use of the VREF options is noted in the Voltage Reference section.
- **RBIAS:** RBIAS has a default setting of 10 k Ω (R201) to ground and is used to set the ADC core bias current.
- **CLOCK:** The default clock input circuitry is derived from a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T201) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped before entering the ADC clock inputs.

A differential LVPECL clock can also be used to clock the ADC input using the [AD9515](#) (U202). Populate R225 and R227 with 0 Ω resistors and remove R217 and R218 to disconnect the default clock path inputs. In addition, populate C207 and C208 with a 0.1 μ F capacitor and remove C210 and C211 to disconnect the default clock path outputs. The AD9515 has many pin-strappable options that are set to a default mode of operation. Consult the AD9515 data sheet for more information about these and other options.

In addition, an on-board oscillator is available on the OSC201 and can act as the primary clock source. The setup is quick and involves installing R212 with a 0 Ω resistor and setting the enable jumper (J205) to the on position. If the user wishes to employ a different oscillator, two oscillator footprint options are available (OSC201) to check the ADC performance.

- **PDWN:** To enable the power-down feature, short J201 to AVDD on the PDWN pin.
- **SCLK/DTP:** To enable the digital test pattern on the digital outputs of the ADC, use J204. If J204 is tied to AVDD during device power-up, Test Pattern 10 0000 0000 0000 is enabled. See the SCLK/DTP Pin section for details.
- **SDIO/ODM:** To enable the low power, reduced signal option (similar to the IEEE 1595.3 reduced range link LVDS output standard), use J203. If J203 is tied to AVDD during device power-up, it enables the LVDS outputs in a low power, reduced signal option from the default ANSI-644 standard. This option changes the signal swing from 350 mV p-p to 200 mV p-p, reducing the power of the DRVDD supply. See the SDIO/ODM Pin section for more details.
- **CSB:** To enable processing of the SPI information on the SDIO and SCLK pins, tie J202 low in the always enable mode. To ignore the SDIO and SCLK information, tie J202 to AVDD.
- **Non-SPI Mode:** For users who wish to operate the DUT without using SPI, remove Jumpers J202, J203, and J204. This disconnects the CSB, SCLK/DTP, and SDIO/ODM pins from the control bus, allowing the DUT to operate in its simplest mode. Each of these pins has internal termination and will float to its respective level.
- **D + x, D - x:** If an alternative data capture method to the setup shown in Figure 60 is used, optional receiver terminations, R206 to R211, can be installed next to the high speed back-plane connector.

ALTERNATIVE ANALOG INPUT DRIVE CONFIGURATION

The following is a brief description of the alternative analog input drive configuration using the [AD8332](#) dual VGA. If this drive option is in use, some components may need to be populated, in which case all the necessary components are listed in Table 17. For more details on the AD8332 dual VGA, including how it works and its optional pin settings, consult the AD8332 data sheet.

To configure the analog input to drive the VGA instead of the default transformer option, the following components need to be removed and/or changed.

- Remove R102, R115, R128, R141, R161, R162, R163, R164, T101, T102, T103, and T104 in the default analog input path.

- Populate R101, R114, R127, and R140 with 0 Ω resistors in the analog input path.
- Populate R105, R113, R118, R124, R131, R137, R151, and R160 with 0 Ω resistors in the analog input path to connect the AD8332.
- Populate R152, R153, R154, R155, R156, R157, R158, R159, C103, C105, C110, C112, C117, C119, C124, and C126 with 10 k Ω resistors to provide an input common-mode level to the ADC analog inputs.
- Remove R305, R306, R313, R314, R405, R406, R412, and R424 to configure the AD8332.

In this configuration, L301 to L308 and L401 to L408 are populated with 0 Ω resistors to allow signal connection and use of a filter if additional requirements are necessary.

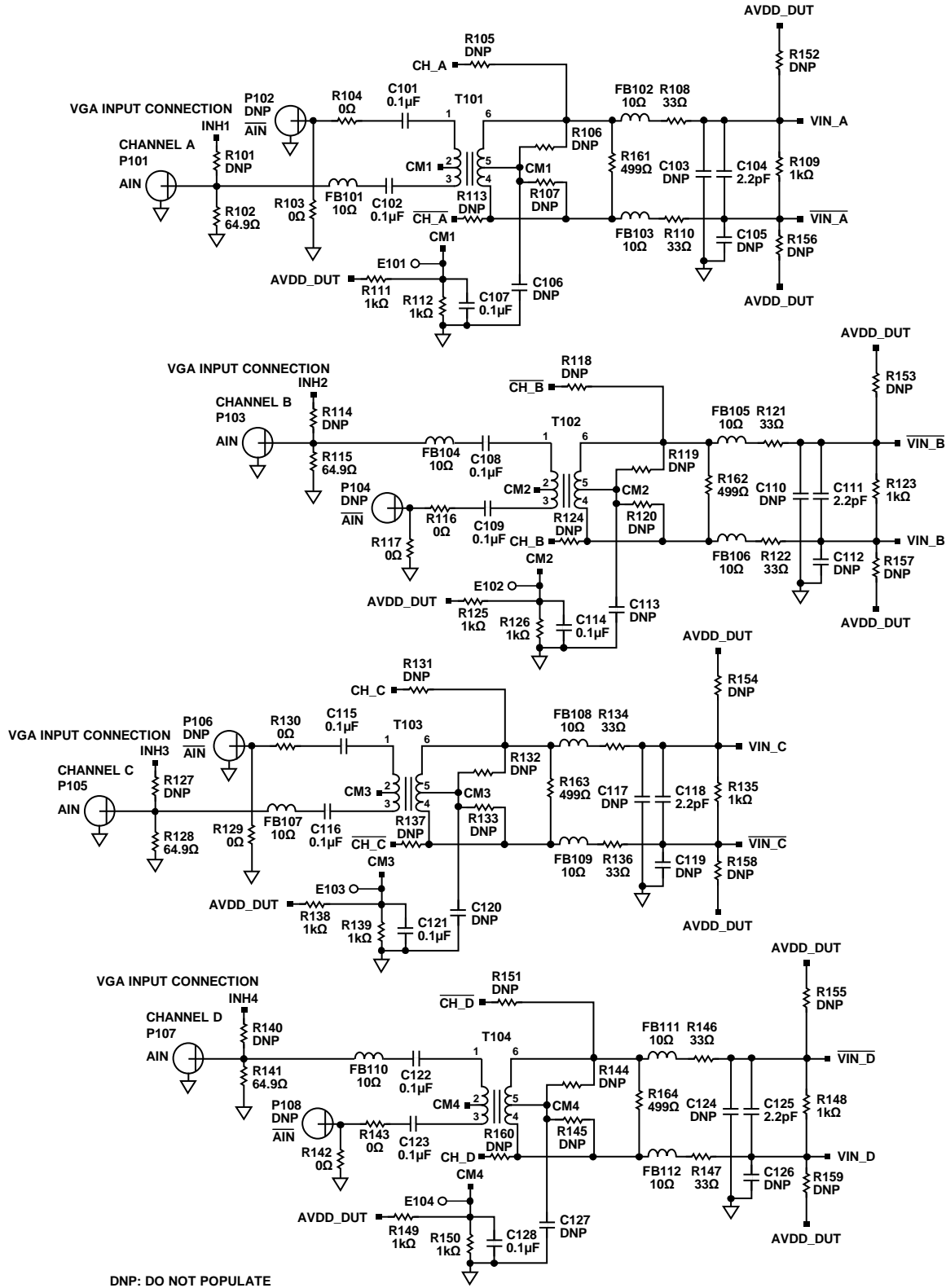


Figure 62. Evaluation Board Schematic, DUT Analog Inputs

05985-015

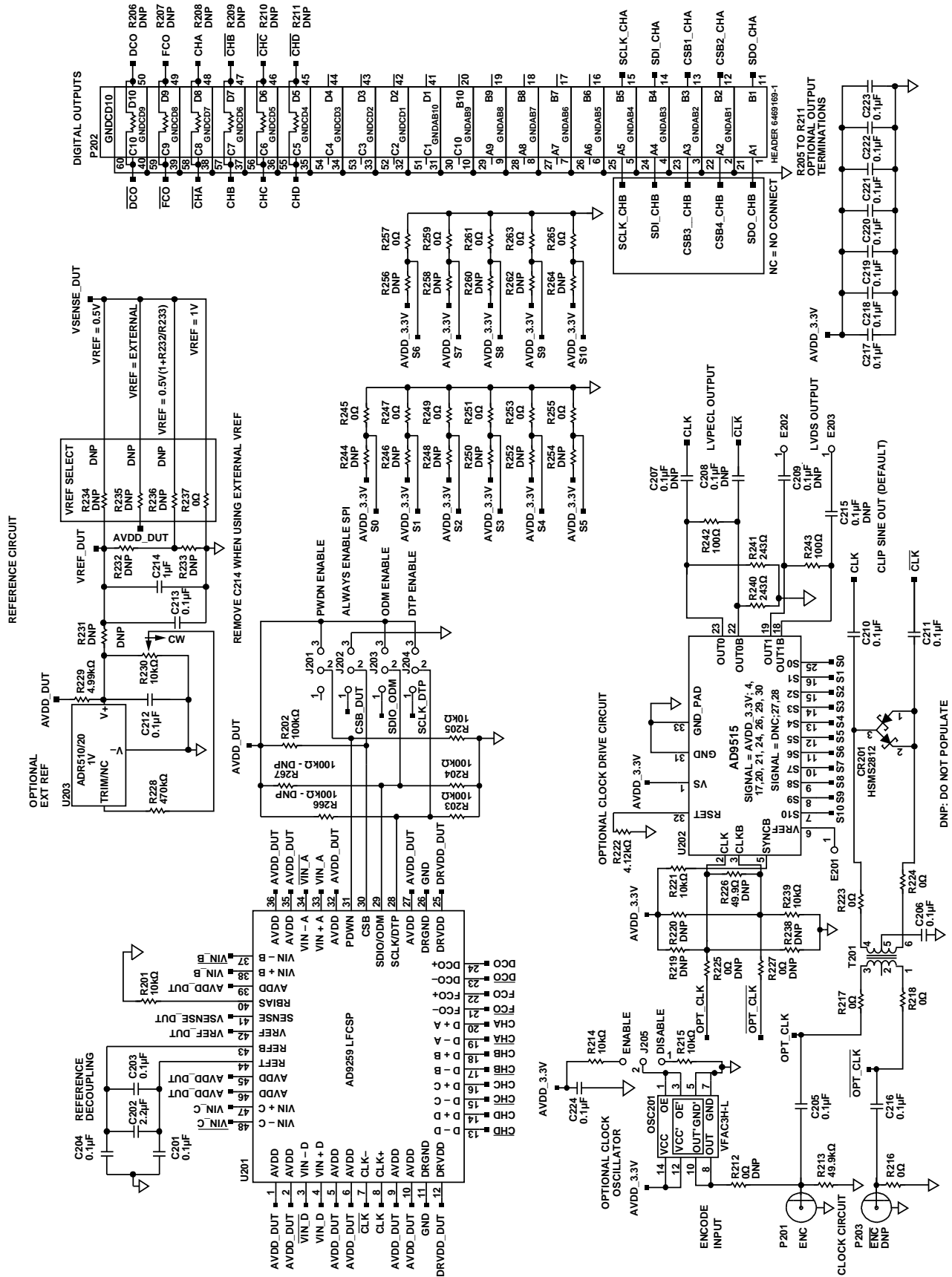


Figure 63. Evaluation Board Schematic, DUT, VREF, Clock Inputs, and Digital Output Interface

POPULATE L301 TO L308 WITH 0Ω RESISTORS OR DESIGN YOUR OWN FILTER.

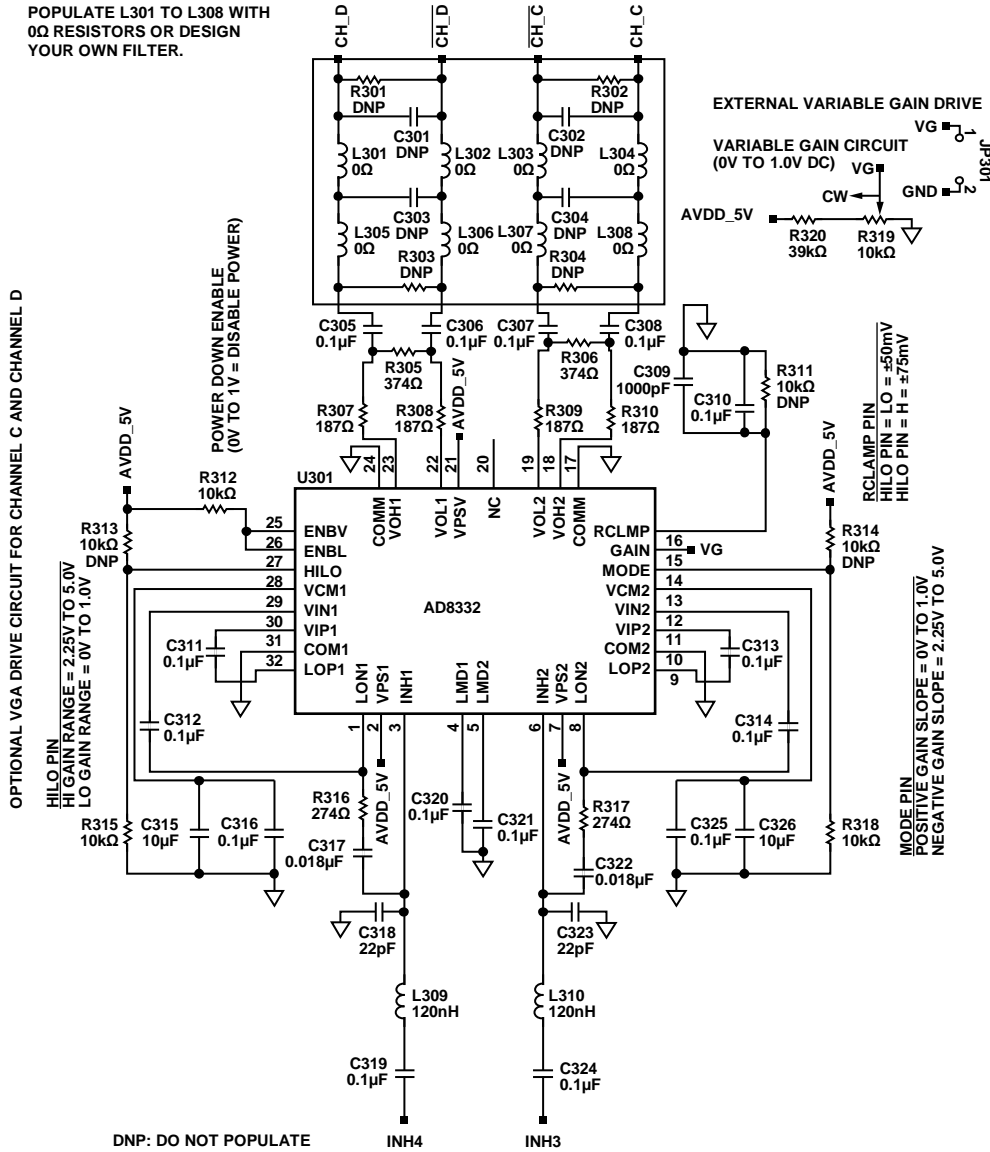


Figure 64. Evaluation Board Schematic, Optional DUT Analog Input Drive and SPI Interface Circuit

05985-017

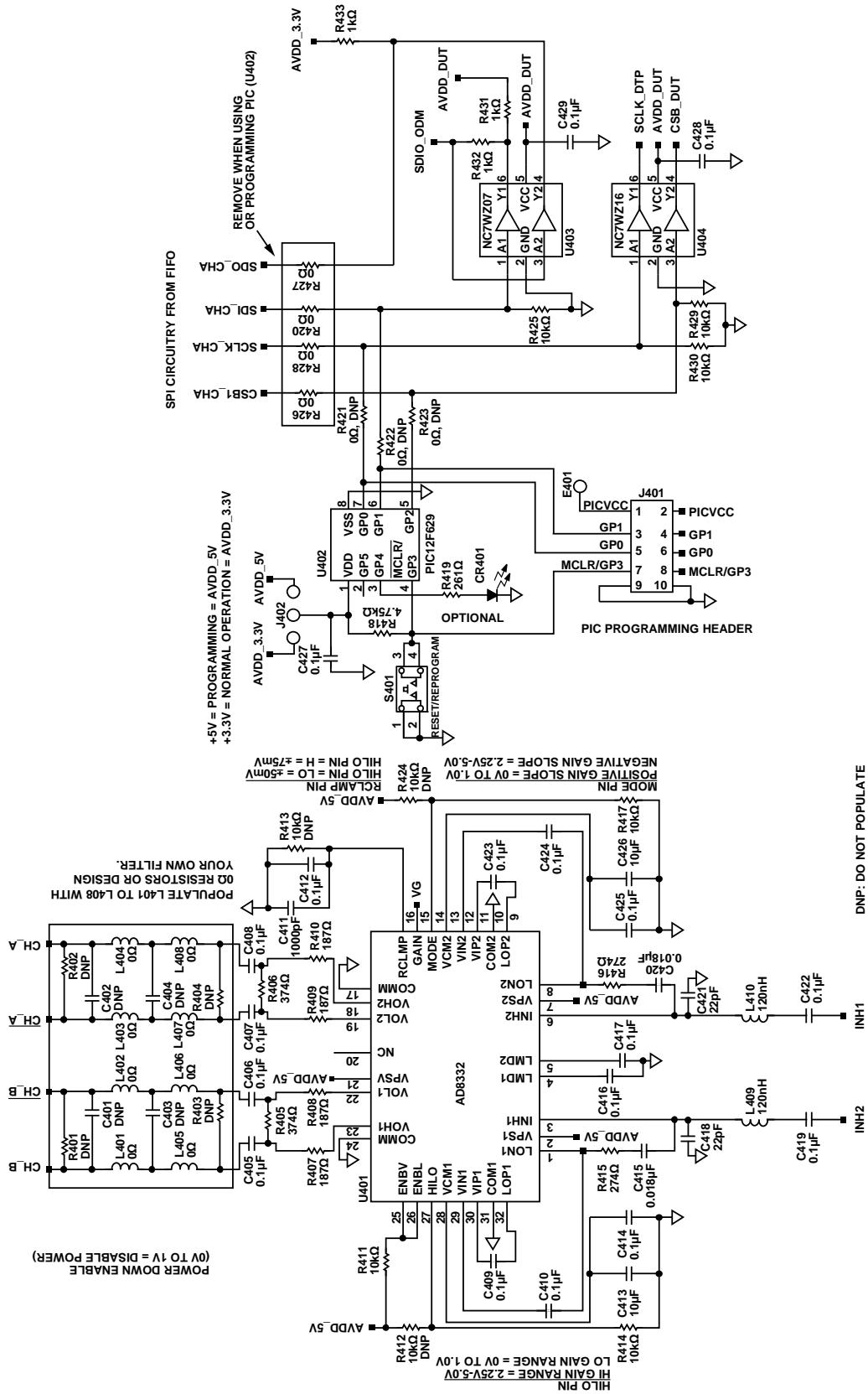


Figure 65. Evaluation Board Schematic, Optional DUT Analog Input Drive and SPI Interface Circuit (Continued)

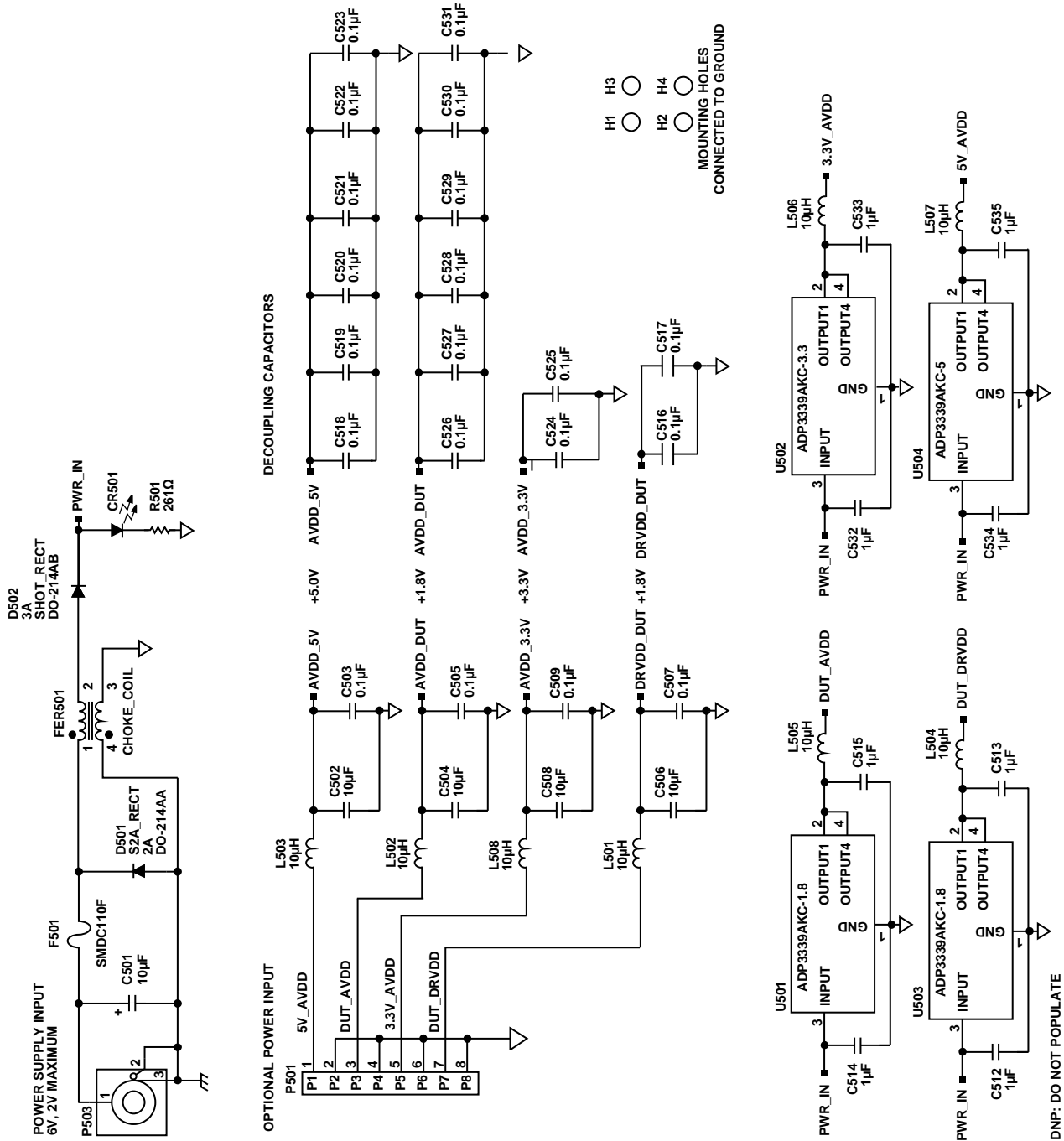


Figure 66. Evaluation Board Schematic, Power Supply Inputs

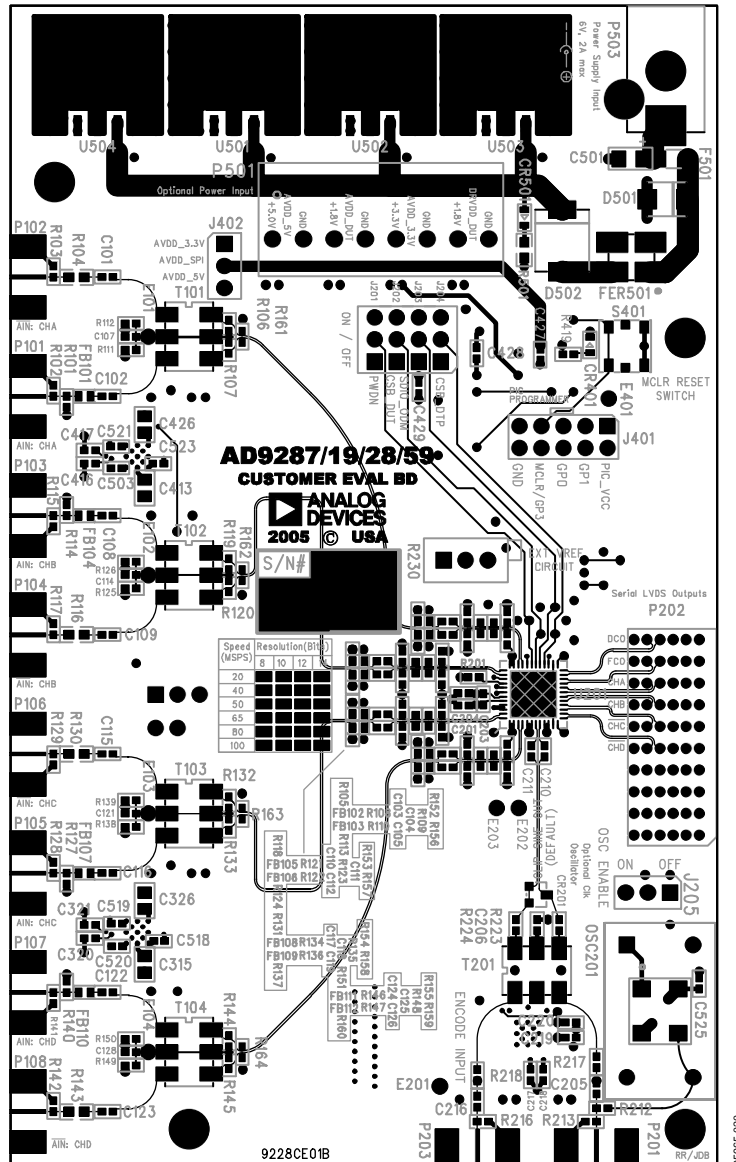
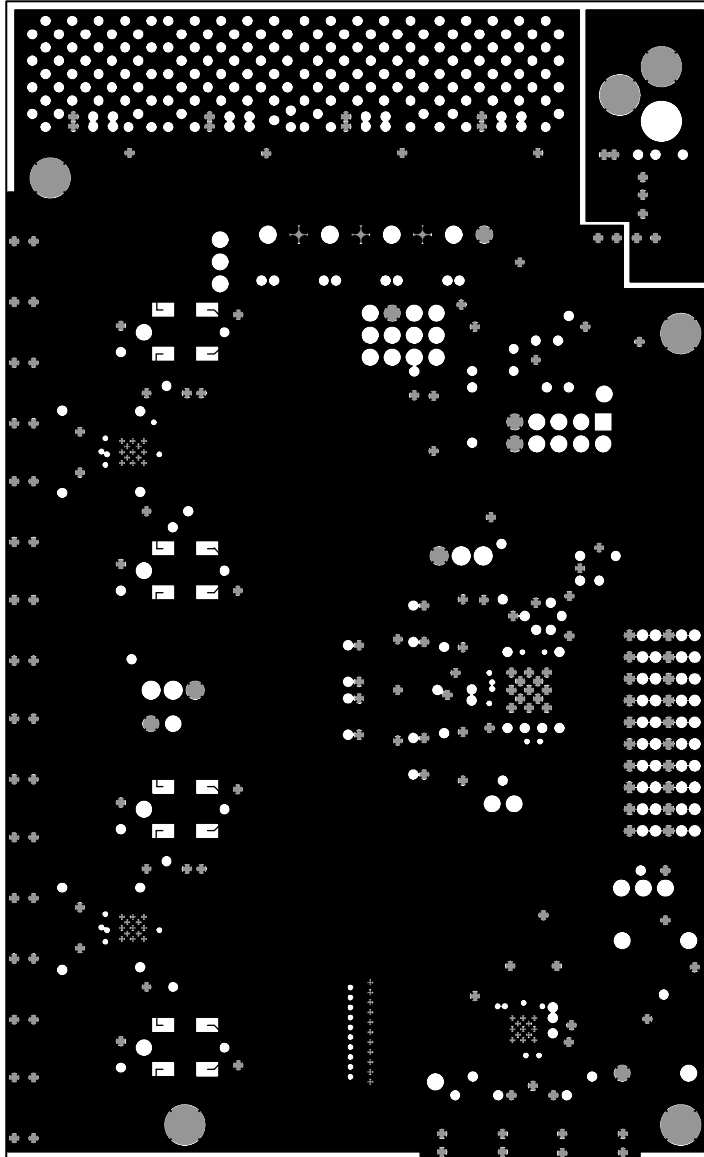
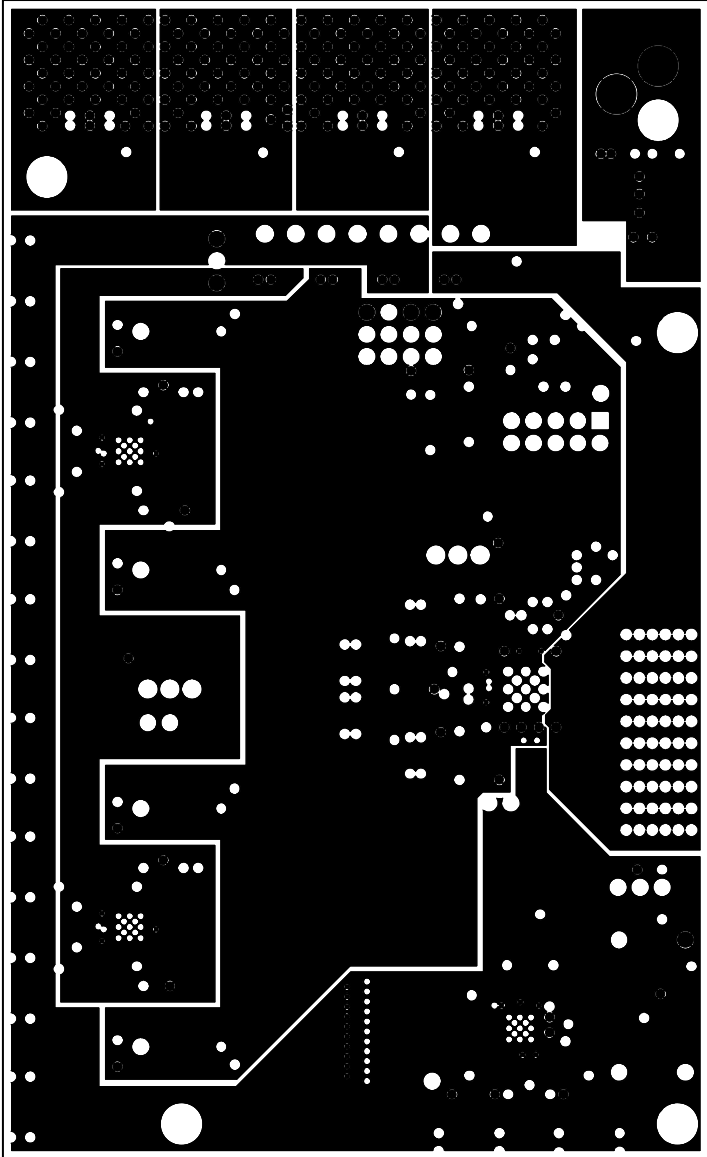


Figure 67. Evaluation Board Layout, Primary Side



05965-021

Figure 68. Evaluation Board Layout, Ground Plane



0596E-022

Figure 69. Evaluation Board Layout, Power Plane

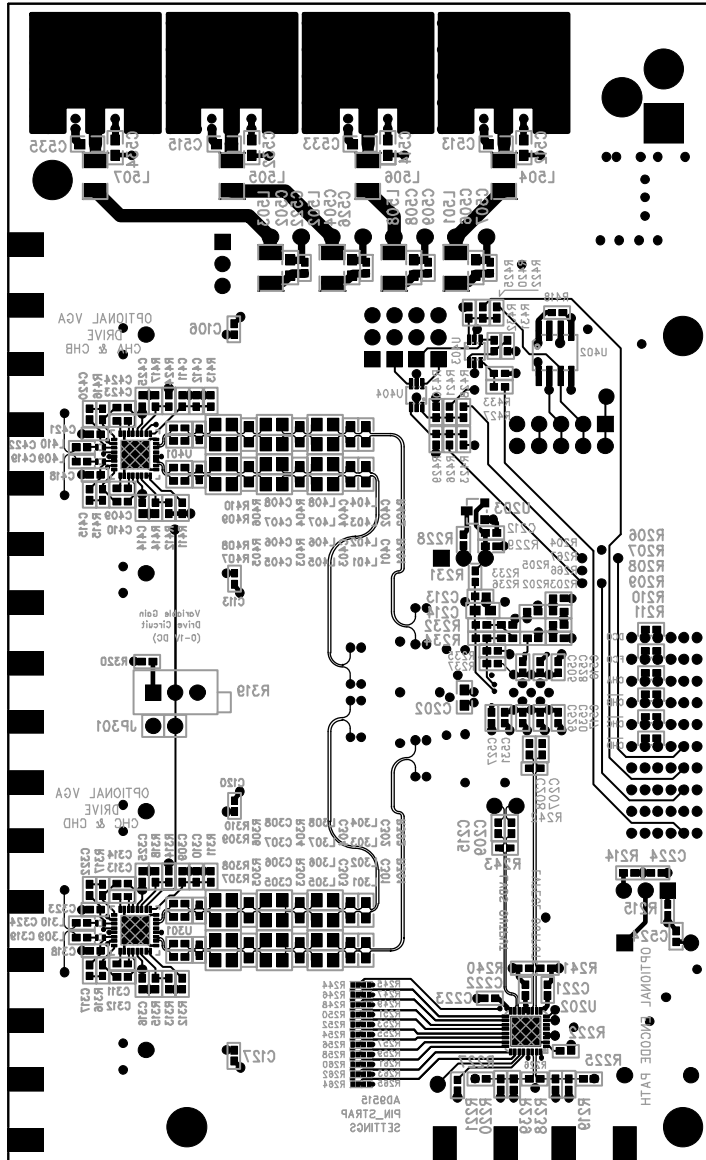


Figure 70. Evaluation Board Layout, Secondary Side (Mirrored Image)

05865-023

Table 17. Evaluation Board Bill of Materials (BOM)¹

| Item | Qty. | Reference Designator | Device | Package | Value | Manufacturer | Manufacturer's Part Number |
|------|------|--|-----------|----------|--|----------------------|----------------------------|
| 1 | 1 | AD9259LFCSP_REVA | PCB | PCB | PCB | | |
| 2 | 75 | C101, C102, C107, C108, C109, C114, C115, C116, C121, C122, C123, C128, C201, C203, C204, C205, C206, C210, C211, C212, C213, C216, C217, C218, C219, C220, C221, C222, C223, C224, C310, C311, C312, C313, C314, C316, C319, C320, C321, C324, C325, C409, C410, C412, C414, C416, C417, C419, C422, C423, C424, C425, C427, C428, C429, C503, C505, C507, C509, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531 | Capacitor | 402 | 0.1 μ F, ceramic, X5R, 10 V, 10% tol | Murata | GRM155R71C104KA88D |
| 3 | 4 | C104, C111, C118, C125 | Capacitor | 402 | 2.2 pF, ceramic, COG, 0.25 pF tol, 50 V | Murata | GRM1555C1H2R2GZ01B |
| 4 | 4 | C315, C326, C413, C426 | Capacitor | 805 | 10 μ F, 6.3 V \pm 10% ceramic, X5R | Murata | GRM219R60J106KE19D |
| 5 | 1 | C202 | Capacitor | 603 | 2.2 μ F, ceramic, X5R, 6.3 V, 10% tol | Murata | GRM188C70J225KE20D |
| 6 | 2 | C309, C411 | Capacitor | 402 | 1000 pF, ceramic, X7R, 25 V, 10% tol | Murata | GRM155R71H102KA01D |
| 7 | 4 | C317, C322, C415, C420 | Capacitor | 402 | 0.018 μ F, ceramic, X7R, 16 V, 10% tol | AVX | 0402YC183KAT2A |
| 8 | 4 | C318, C323, C418, C421 | Capacitor | 402 | 22 pF, ceramic, NPO, 5% tol, 50 V | Murata | GRM1555C1H220JZ01D |
| 9 | 1 | C501 | Capacitor | 1206 | 10 μ F, tantalum, 16 V, 20% tol | Rohm | TCA1C106M8R |
| 10 | 9 | C214, C512, C513, C514, C515, C532, C533, C534, C535 | Capacitor | 603 | 1 μ F, ceramic, X5R, 6.3 V, 10% tol | Murata | GRM188R61C105KA93D |
| 11 | 8 | C305, C306, C307, C308, C405, C406, C407, C408 | Capacitor | 805 | 0.1 μ F, ceramic, X7R, 50 V, 10% tol | Murata | GRM21BR71H104KA01L |
| 12 | 4 | C502, C504, C506, C508 | Capacitor | 603 | 10 μ F, ceramic, X5R, 6.3 V, 20% tol | Murata | GRM188R60J106M |
| 13 | 1 | CR201 | Diode | SOT-23 | 30 V, 20 mA, dual Schottky | Agilent Technologies | HSMS2812-TRIG |
| 14 | 2 | CR401, CR501 | LED | 603 | Green, 4 V, 5 m candela | Panasonic | LNJ314G8TRA |
| 15 | 1 | D502 | Diode | DO-214AB | 3 A, 30 V, SMC | Micro Commercial Co. | SK33-TP |
| 16 | 1 | D501 | Diode | DO-214AA | 2 A, 50 V, SMC | Micro Commercial Co. | S2A-TP |

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| Item | Qty. | Reference Designator | Device | Package | Value | Manufacturer | Manufacturer's Part Number |
|------|------|--|--------------|------------|--|--------------------|----------------------------|
| 17 | 1 | F501 | Fuse | 1210 | 6.0 V, 2.2 A trip-current resettable fuse | Tyco/Raychem | NANOSMDC110F-2 |
| 18 | 1 | FER501 | Choke coil | 2020 | 10 μ H, 5 A, 50 V, 190 Ω @ 100 MHz | Murata | DLW5BSN191SQ2L |
| 19 | 12 | FB101, FB102, FB103, FB104, FB105, FB106, FB107, FB108, FB109, FB110, FB111, FB112 | Ferrite bead | 603 | 10 Ω , test freq 100 MHz, 25% tol, 500 mA | Murata | BLM18BA100SN1B |
| 20 | 1 | JP301 | Connector | 2-pin | 100 mil header jumper, 2-pin | Samtec | TSW-102-07-G-S |
| 21 | 2 | J205, J402 | Connector | 3-pin | 100 mil header jumper, 3-pin | Samtec | TSW-103-07-G-S |
| 22 | 4 | J201 to J204 | Connector | 12-pin | 100 mil header male, 4 \times 3 triple row straight | Samtec | TSW-104-08-G-T |
| 23 | 1 | J401 | Connector | 10-pin | 100 mil header, male, 2 \times 5 double row straight | Samtec | TSW-105-08-G-D |
| 24 | 8 | L501, L502, L503, L504, L505, L506, L507, L508 | Ferrite bead | 1210 | 10 μ H, bead core 3.2 \times 2.5 \times 1.6 SMD, 2 A | Murata | BLM31PG500SN1L |
| 25 | 4 | L309, L310, L409, L410 | Inductor | 402 | 120 nH, test freq 100 MHz, 5% tol, 150 mA | Murata | LQG15HNR12J02B |
| 26 | 16 | L301, L302, L303, L304, L305, L306, L307, L308, L401, L402, L403, L404, L405, L406, L407, L408 | Resistor | 805 | 0 Ω , 1/8 W, 5% tol | NIC Components | NRC10ZOTRF |
| 27 | 1 | OSC201 | Oscillator | SMT | Clock oscillator, 50.00 MHz, 3.3 V | Valpey Fisher | VFAC3H-L-50MHz |
| 28 | 5 | P101, P103, P105, P107, P201 | Connector | SMA | Side-mount SMA for 0.063" board thickness | Johnson Components | 142-0710-851 |
| 29 | 1 | P202 | Connector | Header | 1469169-1, right angle 2-pair, 25 mm, header assembly | Tyco | 6469169-1 |
| 30 | 1 | P503 | Connector | 0.1", PCMT | SC1153, power supply connector | Switchcraft | RAPC722X |
| 31 | 15 | R201, R205, R214, R215, R221, R239, R312, R315, R318, R411, R414, R417, R425, R429, R430 | Resistor | 402 | 10 k Ω , 1/16 W, 5% tol | NIC Components | NRC04J103TRF |
| 32 | 14 | R103, R117, R129, R142, R216, R217, R218, R223, R224, R237, R420, R426, R427, R428 | Resistor | 402 | 0 Ω , 1/16 W, 5% tol | NIC Components | NRC04Z0TRF |
| 33 | 4 | R102, R115, R128, R141 | Resistor | 402 | 64.9 Ω , 1/16 W, 1% tol | NIC Components | NRC04F64R9TRF |
| 34 | 4 | R104, R116, R130, R143 | Resistor | 603 | 0 Ω , 1/10 W, 5% tol | NIC Components | NRC06Z0TRF |

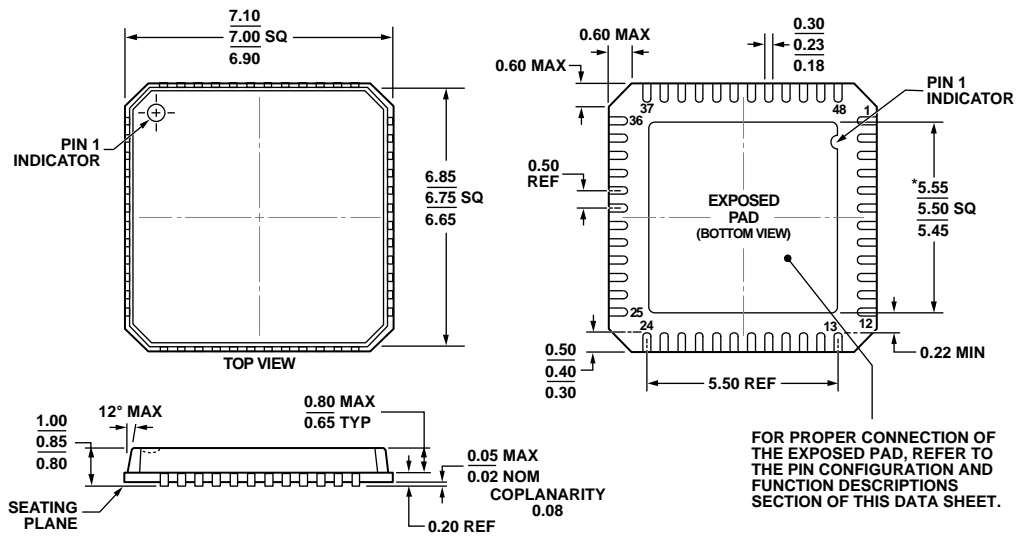
| Item | Qty. | Reference Designator | Device | Package | Value | Manufacturer | Manufacturer's Part Number |
|------|------|--|---------------|---------|--|----------------|----------------------------|
| 35 | 15 | R109, R111, R112, R123, R125, R126, R135, R138, R139, R148, R149, R150, R431, R432, R433 | Resistor | 402 | 1 k Ω , 1/16 W, 1% tol | NIC Components | NRC04F1001TRF |
| 36 | 8 | R108, R110, R121, R122, R134, R136, R146, R147 | Resistor | 402 | 33 Ω , 1/16 W, 5% tol | NIC Components | NRC04J330TRF |
| 37 | 4 | R161, R162, R163, R164 | Resistor | 402 | 499 Ω , 1/16 W, 1% tol | NIC Components | NRC04F4990TRF |
| 38 | 3 | R202, R203, R204 | Resistor | 402 | 100 k Ω , 1/16 W, 1% tol | NIC Components | NRC04F1003TRF |
| 39 | 1 | R222 | Resistor | 402 | 4.12 k Ω , 1/16 W, 1% tol | NIC Components | NRC04F4121TRF |
| 40 | 1 | R213 | Resistor | 402 | 49.9 Ω , 1/16 W, 0.5% tol | Susumu | RR0510R-49R9-D |
| 41 | 1 | R229 | Resistor | 402 | 4.99 k Ω , 1/16 W, 5% tol | NIC Components | NRC04F4991TRF |
| 42 | 2 | R230, R319 | Potentiometer | 3-lead | 10 k Ω , cermet trimmer potentiometer, 18-turn top adjust, 10%, 1/2 W | BC Components | CT94EW103 |
| 43 | 1 | R228 | Resistor | 402 | 470 k Ω , 1/16 W, 5% tol | NIC Components | NRC04J474TRF |
| 44 | 1 | R320 | Resistor | 402 | 39 k Ω , 1/16 W, 5% tol | NIC Components | NRC04J393TRF |
| 45 | 8 | R307, R308, R309, R310, R407, R408, R409, R410 | Resistor | 402 | 187 Ω , 1/16 W, 1% tol | NIC Components | NRC04F1870TRF |
| 46 | 4 | R305, R306, R405, R406 | Resistor | 402 | 374 Ω , 1/16 W, 1% tol | NIC Components | NRC04F3740TRF |
| 47 | 4 | R316, R317, R415, R416 | Resistor | 402 | 274 Ω , 1/16 W, 1% tol | NIC Components | NRC04F2740TRF |
| 48 | 11 | R245, R247, R249, R251, R253, R255, R257, R259, R261, R263, R265 | Resistor | 201 | 0 Ω , 1/20 W, 5% tol | Panasonic | ERJ-1GE0R00C |
| 49 | 1 | R418 | Resistor | 402 | 4.75 k Ω , 1/16 W, 1% tol | NIC Components | NRC04J472TRF |
| 50 | 1 | R419 | Resistor | 402 | 261 Ω , 1/16 W, 1% tol | NIC Components | NRC04F2610TRF |
| 51 | 1 | R501 | Resistor | 603 | 261 Ω , 1/16 W, 1% tol | NIC Components | NRC06F2610TRF |
| 52 | 2 | R240, R241 | Resistor | 402 | 243 Ω , 1/16 W, 1% tol | NIC Components | NRC04F2430TRF |
| 53 | 2 | R242, R243 | Resistor | 402 | 100 Ω , 1/16 W, 1% tol | NIC Components | NRC04F1000TRF |
| 54 | 1 | S401 | Switch | SMD | Light touch, 100GE, 5 mm | Panasonic | EVQ-PLDA15 |
| 55 | 5 | T101, T102, T103, T104, T201 | Transformer | CD542 | ADT1-1WT, 1:1 impedance ratio transformer | Mini-Circuits | ADT1-1WT+ |
| 56 | 2 | U501, U503 | IC | SOT-223 | ADP3339AKC-1.8, 1.5 A, 1.8 V LDO regulator | Analog Devices | ADP3339AKCZ-1.8 |

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| Item | Qty. | Reference Designator | Device | Package | Value | Manufacturer | Manufacturer's Part Number |
|------|------|----------------------|--------|-------------------|--|----------------|----------------------------|
| 57 | 2 | U301, U401 | IC | LFCSP, CP-32 | AD8332ACP, ultralow noise precision dual VGA | Analog Devices | AD8332ACPZ |
| 58 | 1 | U504 | IC | SOT-223 | ADP3339AKC-5 | Analog Devices | ADP3339AKCZ-5 |
| 59 | 1 | U502 | IC | SOT-223 | ADP3339AKC-3.3 | Analog Devices | ADP3339AKCZ-3.3 |
| 60 | 1 | U201 | IC | LFCSP, CP-48-1 | AD9259BCPZ-50, quad, 14-bit, 50 MSPS serial LVDS 1.8 V ADC | Analog Devices | AD9259BCPZ-50 |
| 61 | 1 | U203 | IC | SOT-23 | ADR510ARTZ, 1.0V, precision low noise shunt voltage reference | Analog Devices | ADR510ARTZ |
| 62 | 1 | U202 | IC | LFCSP CP-32-2 | AD9515BCPZ | Analog Devices | AD9515BCPZ |
| 63 | 1 | U403 | IC | SC70, MAA06A | NC7WZ07 | Fairchild | NC7WZ07P6X_NL |
| 64 | 1 | U404 | IC | SC70, MAA06A | NC7WZ16 | Fairchild | NC7WZ16P6X_NL |
| 65 | 1 | U402 | IC | 8-SOIC | Flash prog mem 1k × 14, RAM size 64 × 8, 20 MHz speed, PIC12F controller series | Microchip | PIC12F629-I/SN |

¹ This BOM is RoHS compliant.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2 WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 71. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad (CP-48-8)
Dimensions shown in millimeters

02-23-2010-C

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| AD9259ABCPZ-50 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-48-8 |
| AD9259ABCPZRL7-50 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ] 7" Tape and Reel | CP-48-8 |
| AD9259-50EBZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

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NOTES