#### INTEGRATED CIRCUITS

# DATA SHEET

### **PZXPLAPRO**

Design tools for Philips Semiconductors CoolRunner™ CPLDs

Product specification

1999 Jan 26

IC27 Data Handbook





Philips Semiconductors Product specification

### Design tools for Philips Semiconductors CoolRunner CPLDs

**PZXPLAPRO** 

#### **FEATURES**

- Design support for all CoolRunner™ CPLDs and the CoolRunner 22V10
- Hierarchical design entry, including
  - Schematic capture
  - Philips Hardware Description Language (PHDL)
  - Verilog HDL
  - VHDL
- Fitter support for EDIF flows from popular third party tools
- Graphical simulation environment
  - Functional simulation
  - AC timing simulation
  - Dynamic current consumption estimation
- Generates VHDL and Verilog device level timing models for board level simulation
- Graphical signal pin placement editor
- Free upgrades and technical support
- Full manual and introductory tutorial
- Runs on Windows<sup>™</sup> NT and Windows 95

#### SYSTEM REQUIREMENTS

It is recommended that your system have the following as a minimum for using  $XPLA^{\text{\tiny TM}}$  Professional:

- Pentium PC running at 100MHz or better
- 32 Megabytes of RAM
- 30 Megabytes of free disk space
- Microsoft Windows 95 or Windows NT 4.0

#### **DESCRIPTION**

Philips Semiconductors' XPLA Professional CAE Tool is a Windows based software package used to develop digital designs for the CoolRunner line of Complex Programmable Logic Devices (CPLDs). Hierarchical design entry methods include schematic capture, Philips Hardware Description Language (PHDL), Verilog HDL, and VHDL. Also included is a graphical simulation environment that provides functional simulation, AC timing simulation, and dynamic current consumption estimation. XPLA Professional includes device fitters for all currently released CoolRunner CPLDs, and free upgrades are published on the www.coolpld.com website as new devices are released. The fitter produces a JEDEC file used by industry standard programmers or our own ISP software to configure the targeted device; and also Verilog and VHDL device level timing models which can be used in third party simulators for board level simulation.

For more information or for technical support, contact the Philips Semiconductors Programmable Logic Business Line at 1–888–COOLPLD (1–505–858–2996 outside the USA) or through email at coolpld@abq.sc.philips.com.

#### ORDERING INFORMATION

ORDER CODE	DESCRIPTION	12NC
PZXPLAPRO MSC	XPLA Professional Design Tool Package	935262422112

1999 Jan 26 2 853–2139 20699

<sup>™</sup> Windows is a trademark of Microsoft Corporation

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**NOTES** 

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#### Data sheet status

Data sheet status	Product status	Definition [1]	
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.	
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date.  Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.	
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.	

<sup>[1]</sup> Please consult the most recently issued datasheet before initiating or completing a design.

#### **Definitions**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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