MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 270 µA at 1 MHz, 2.2 V
  - Standby Mode (VLO): 0.3 µA
  - Off Mode (RAM Retention): 0.1 µA
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations:
  - Internal Frequencies up to 16 MHz
  - Internal Very Low-Power LF Oscillator
  - 32-kHz Crystal
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%
  - Resonator
  - External Digital Clock Source
  - External Resistor
- 12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Seven Capture/Compare With Shadow Registers
- Four Universal Serial Communication Interfaces (USCI)
  - USCI_A0 and USCI_A1
  - Enhanced UART Supporting Auto-Baudrate Detection
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - USCI_B0 and USCI_B1
  - I^2C
  - Synchronous SPI
- On-Chip Comparator
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Brownout Detector
- Bootstrap Loader
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Family Members Include:
  - MSP430F233
    - 8KB+256B Flash Memory,
    - 1KB RAM
  - MSP430F235
    - 16KB+256B Flash Memory
    - 2KB RAM
  - MSP430F247, MSP430F2471 (1)
    - 32KB+256B Flash Memory
    - 4KB RAM
  - MSP430F248, MSP430F2481
    - 48KB+256B Flash Memory
    - 4KB RAM
  - MSP430F249, MSP430F2491
    - 60KB+256B Flash Memory
    - 2KB RAM
  - MSP430F2410
    - 56KB+256B Flash Memory
    - 4KB RAM
- Available in 64-Pin QFP and 64-Pin QFN Packages (See Available Options)
- For Complete Module Descriptions, See *MSP430x2xx Family User's Guide*, Literature Number SLAU144

(1) The MSP430F24x1 devices are identical to the MSP430F24x devices, with the exception that the ADC12 module is not implemented on the MSP430F24x1.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The Texas Instruments MSP430™ family of ultra-low power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The calibrated digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430F23x/24x(1)/2410 series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter (not MSP430F24x1), a comparator, four (two in MSP430F23x) universal serial communication interface (USCI) modules, and up to 48 I/O pins. The MSP430F24x1 devices are identical to the MSP430F24x devices, with the exception that the ADC12 module is not implemented. The MSP430F23x devices are identical to the MSP430F24x devices, with the exception that a reduced Timer_B, one USCI module, and less RAM are integrated.

Typical applications include sensor systems, industrial control applications, hand-held meters, etc.

Table 1. Available Options

T_A	PACKAGED DEVICES(1)(2)	
	PLASTIC 64-PIN QFP (PM)	PLASTIC 64-PIN QFN (RGC)
-40°C to 105°C	MSP430F233TPM	MSP430F233TRGC
	MSP430F235TPM	MSP430F235TRGC
	MSP430F247TPM	MSP430F247TRGC
	MSP430F2471TPM	MSP430F2471TRGC
	MSP430F248TPM	MSP430F248TRGC
	MSP430F2481TPM	MSP430F2481TRGC
	MSP430F249TPM	MSP430F249TRGC
	MSP430F2491TPM	MSP430F2491TRGC
	MSP430F2410TPM	MSP430F2410TRGC

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

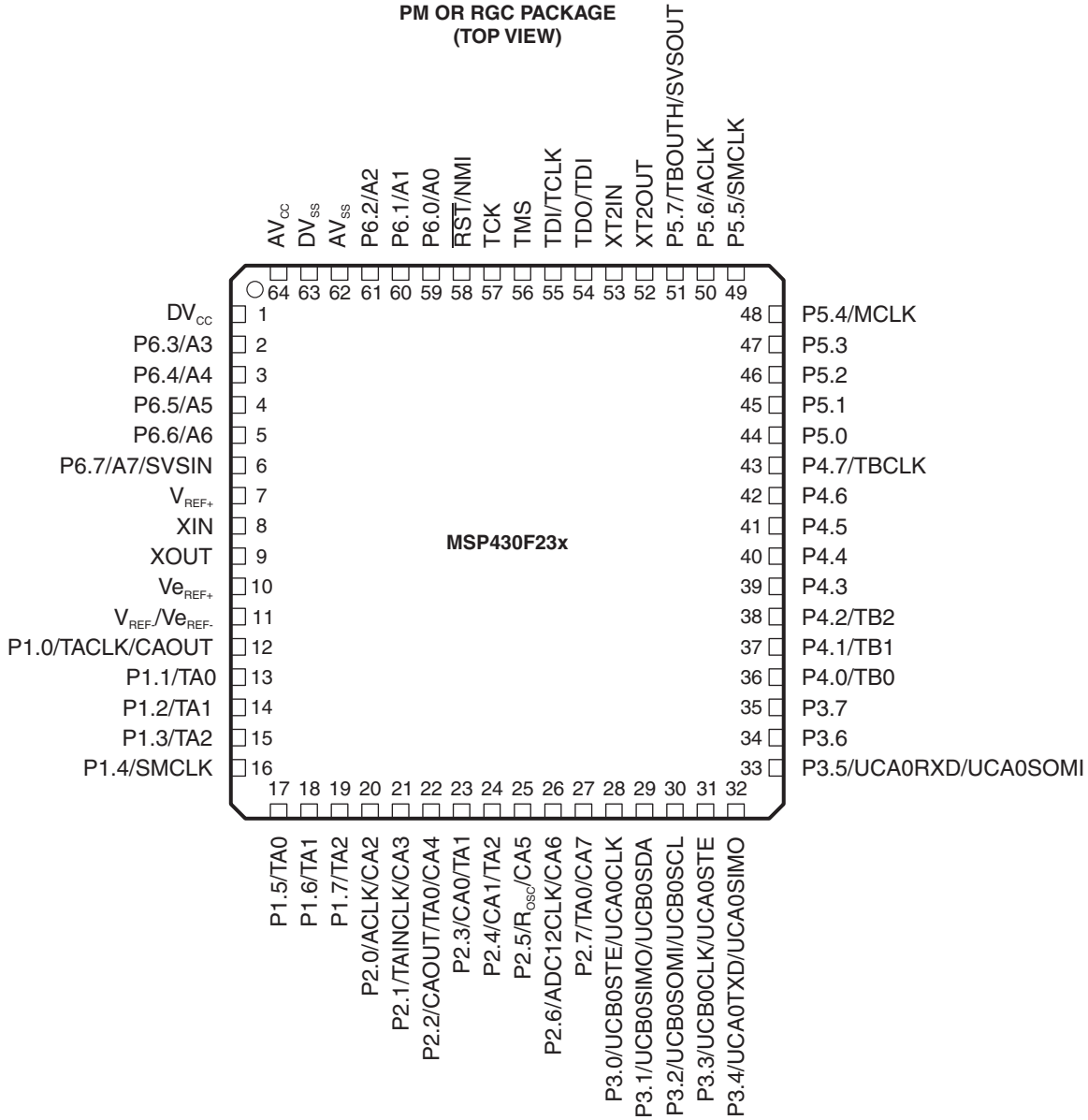
Development Tool Support

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

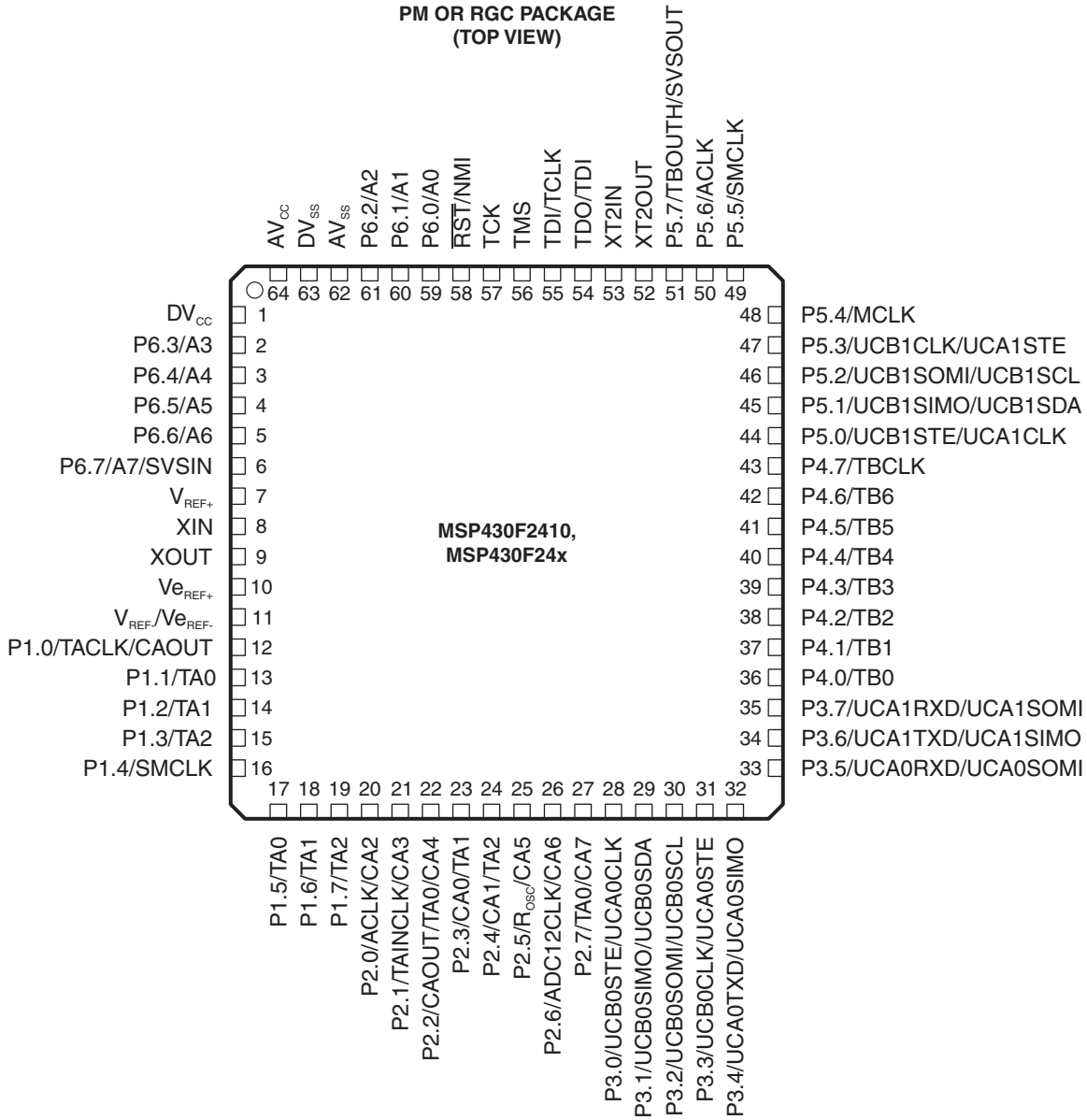
- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U64 (PM package)
- Standalone Target Board
  - MSP-TS430PM64 (PM package)
- Production Programmer
  - MSP-GANG430

Device Pinout, MSP430F23x

PM OR RGC PACKAGE
(TOP VIEW)

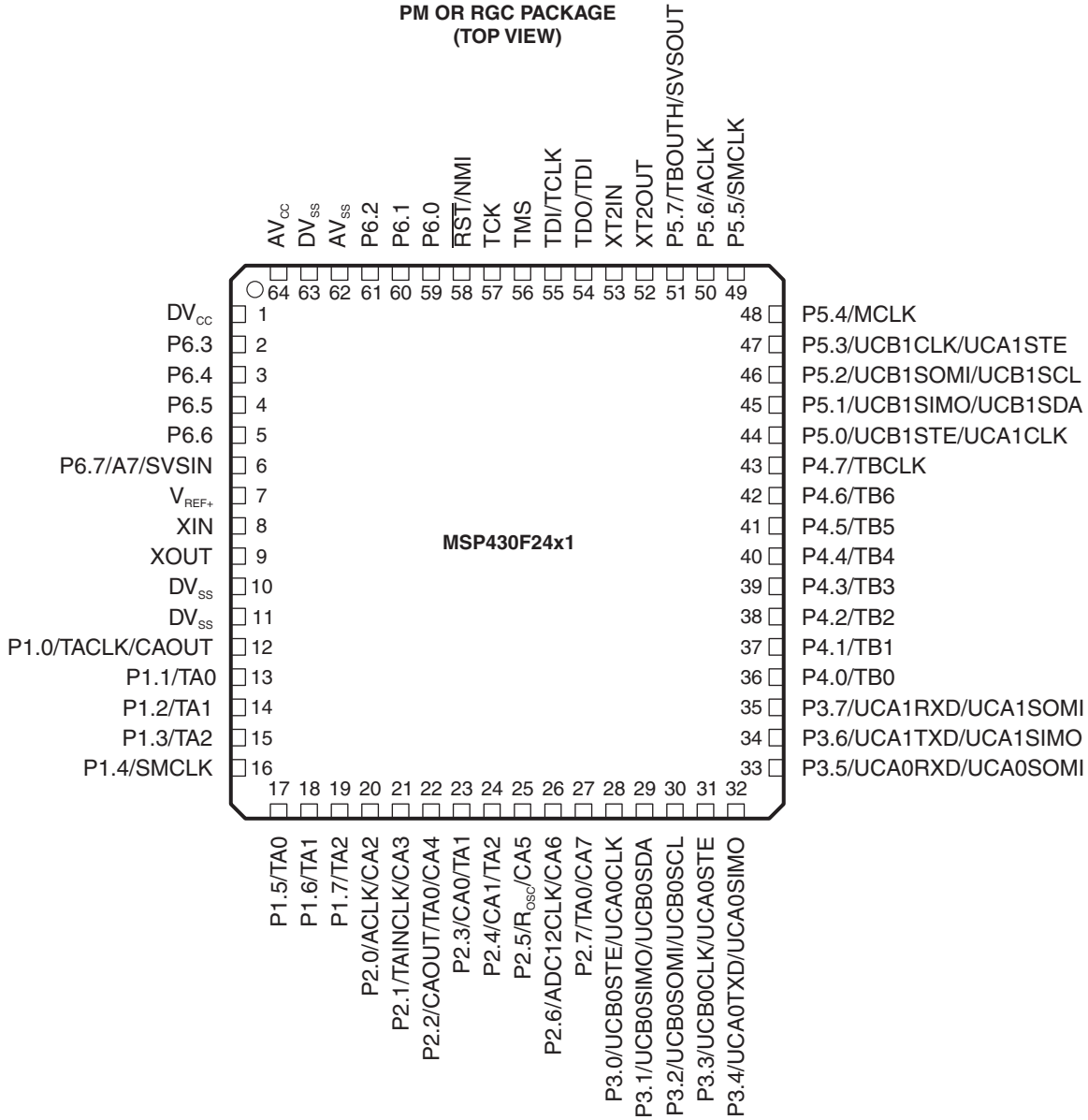


Device Pinout, MSP430F24x, MSP430F2410

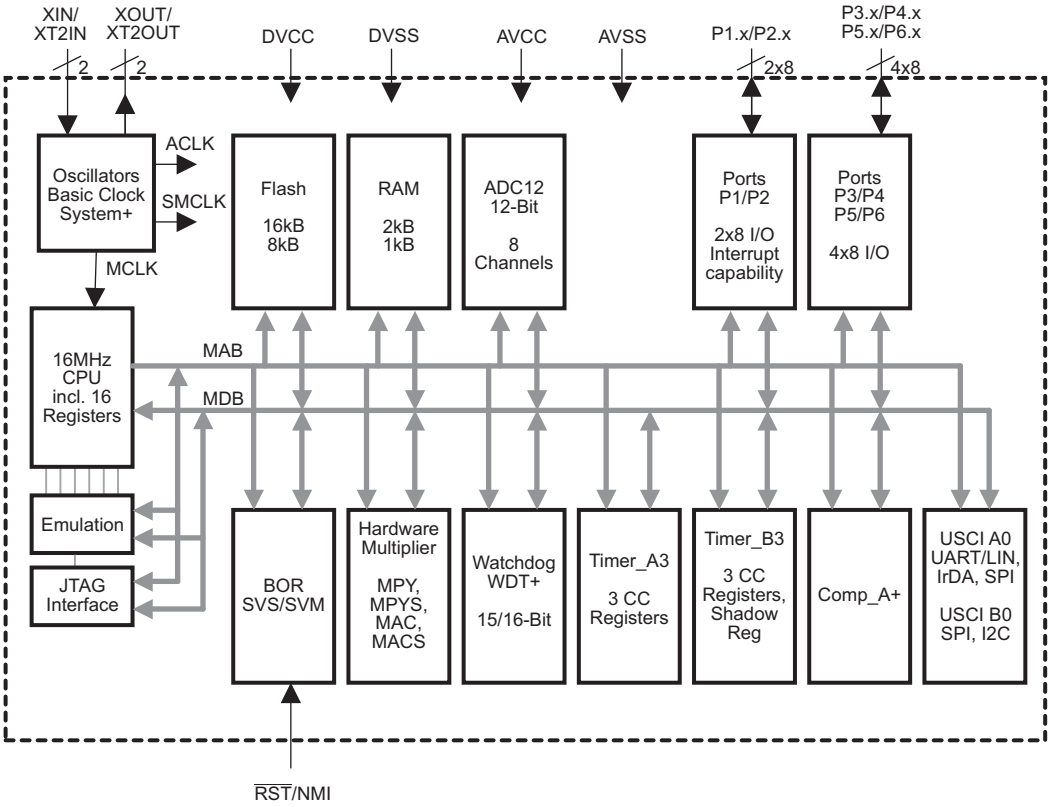


Device Pinout, MSP430F24x1

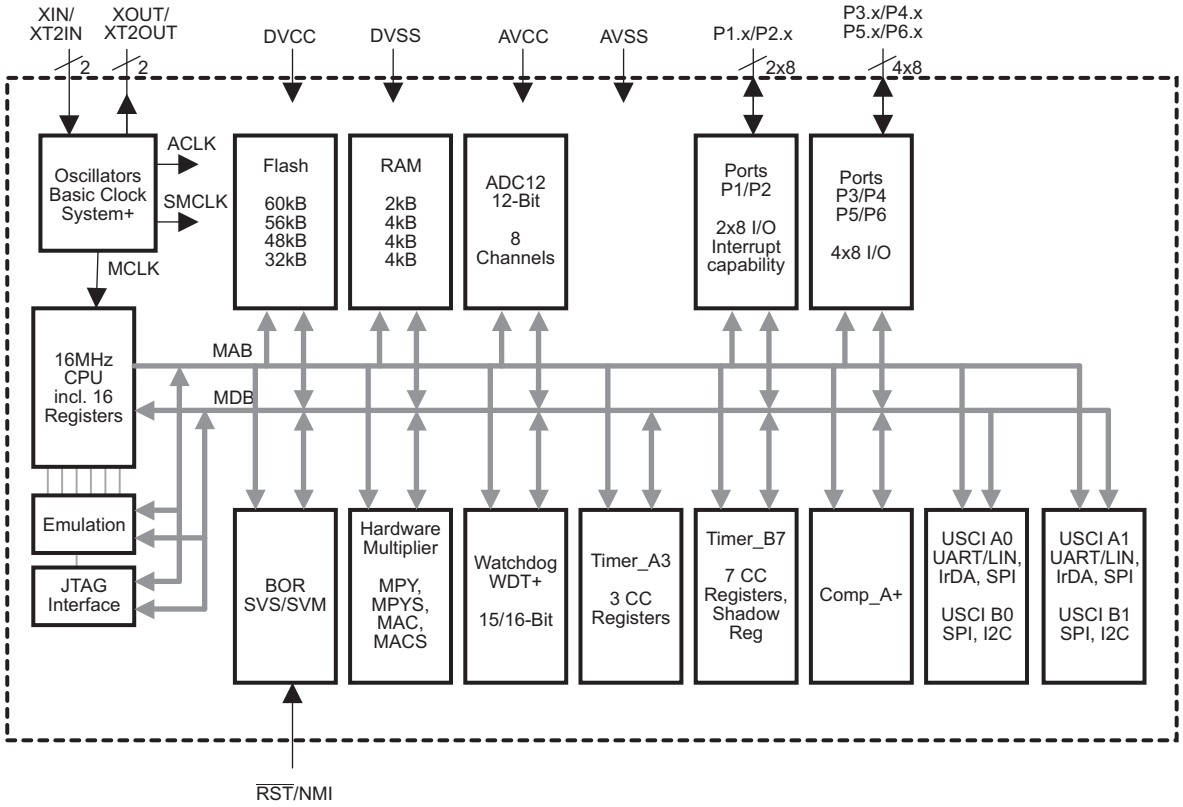
PM OR RGC PACKAGE
(TOP VIEW)



Functional Block Diagram, MSP430F23x



Functional Block Diagram, MSP430F24x, MSP430F2410



Functional Block Diagram, MSP430F24x1

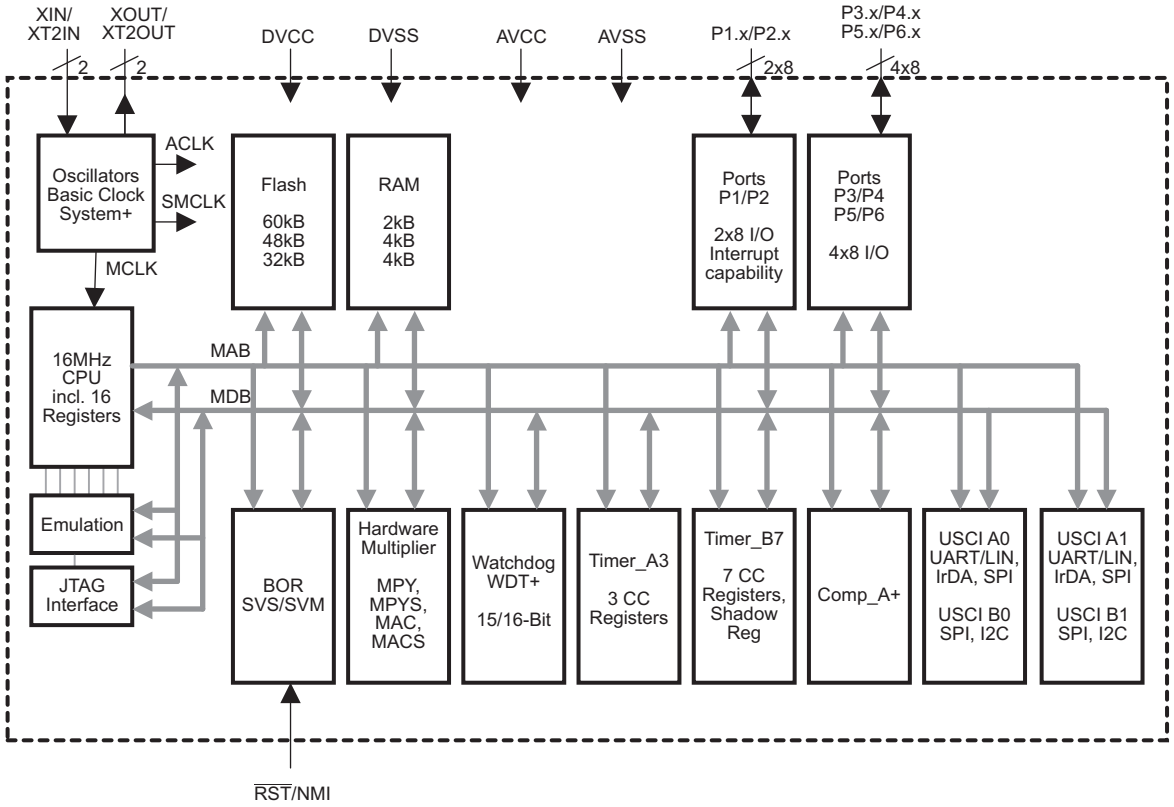


Table 2. Terminal Functions, MSP430F23x

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AV_{CC}	64		Analog supply voltage, positive. Supplies only the analog portion of ADC12.
AV_{SS}	62		Analog supply voltage, negative. Supplies only the analog portion of ADC12.
DV_{CC}	1		Digital supply voltage, positive. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative. Supplies all digital parts.
P1.0/TACLK/CAOUT	12	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input/Comparator_A output
P1.1/TA0	13	I/O	General-purpose digital I/O / Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O / Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O / Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O / SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	I/O	General-purpose digital I/O / ACLK output/Comparator_A input
P2.1/TAINCLK/CA3	21	I/O	General-purpose digital I/O / Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0/CA4	22	I/O	General-purpose digital I/O / Timer_A, capture: CCI0B input/Comparator_A output/BSL receive/Comparator_A input
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output/Comparator_A input
P2.5/R_{OSC}/CA5	25	I/O	General-purpose digital I/O / input for external resistor defining the DCO nominal frequency/Comparator_A input
P2.6/ADC12CLK/CA6	26	I/O	General-purpose digital I/O / conversion clock - 12-bit ADC/Comparator_A input
P2.7/TA0/CA7	27	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output/Comparator_A input
P3.0/UCB0STE/ UCA0CLK	28	I/O	General-purpose digital I/O / USCI_B0 slave transmit enable/USCI A0 clock input/output
P3.1/UCB0SIMO/UCB0SDA	29	I/O	General-purpose digital I/O / USCI_B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/ UCB0SCL	30	I/O	General-purpose digital I/O / USCI_B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/UCA0STE	31	I/O	General-purpose digital I/O / USCI_B0 clock input/output, USCI A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	32	I/O	General-purpose digital I/O / USCI_A0 transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	33	I/O	General-purpose digital I/O / USCI_A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6	34	I/O	General-purpose digital I/O
P3.7	35	I/O	General-purpose digital I/O
P4.0/TB0	36	I/O	General-purpose digital I/O / Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O / Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O / Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3	39	I/O	General-purpose digital I/O
P4.4	40	I/O	General-purpose digital I/O
P4.5	41	I/O	General-purpose digital I/O
P4.6	42	I/O	General-purpose digital I/O
P4.7/TBCLK	43	I/O	General-purpose digital I/O / Timer_B, clock signal TBCLK input
P5.0	44	I/O	General-purpose digital I/O
P5.1	45	I/O	General-purpose digital I/O
P5.2	46	I/O	General-purpose digital I/O
P5.3	47	I/O	General-purpose digital I/O
P5.4/MCLK	48	I/O	General-purpose digital I/O / main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O / submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O / auxiliary clock ACLK output
P5.7/TBOUTH/SVSOUT	51	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance - Timer_B TB0 to TB6/SVS comparator output
P6.0/A0	59	I/O	General-purpose digital I/O / analog input A0 - 12-bit ADC
P6.1/A1	60	I/O	General-purpose digital I/O / analog input A1 - 12-bit ADC
P6.2/A2	61	I/O	General-purpose digital I/O / analog input A2 - 12-bit ADC

Table 2. Terminal Functions, MSP430F23x (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P6.3/A3	2	I/O	General-purpose digital I/O / analog input A3 - 12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O / analog input A4 - 12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O / analog input A5 - 12-bit ADC
P6.6/A6	5	I/O	General-purpose digital I/O / analog input A6 - 12-bit ADC
P6.7/A7/SVSIN	6	I/O	General-purpose digital I/O / analog input A7 - 12-bit ADC/SVS input
XT2OUT	52	O	Output terminal of crystal oscillator XT2
XT2IN	53	I	Input port for crystal oscillator XT2
RST/NMI	58	I	Reset input, nonmaskable interrupt input, or bootstrap loader start (in flash devices)
TCK	57	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start.
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output. TDO/TDI data output or programming data input terminal.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
V_{eREF+}	10	I	Input for an external reference voltage
V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC12
V_{REF-}/V_{eREF-}	11	I	Negative terminal for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output for crystal oscillator XT1. Standard or watch crystals can be connected.
QFN Pad	NA	NA	QFN package pad connection to DV_{SS} recommended

Table 3. Terminal Functions, MSP430F24x, MSP430F2410

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK/CAOUT	12	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input/Comparator_A output
P1.1/TA0	13	I/O	General-purpose digital I/O / Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O / Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O / Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O / SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	I/O	General-purpose digital I/O / ACLK output/Comparator_A input
P2.1/TAINCLK/CA3	21	I/O	General-purpose digital I/O / Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0/CA4	22	I/O	General-purpose digital I/O / Timer_A, capture: CCI0B input / Comparator_A output/BSL receive/Comparator_A input
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output / Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output / Comparator_A input
P2.5/R_{OSC}/CA5	25	I/O	General-purpose digital I/O / Input for external resistor defining the DCO nominal frequency / Comparator_A input
P2.6/ADC12CLK/CA6	26	I/O	General-purpose digital I/O / Conversion clock - 12-bit ADC / Comparator_A input
P2.7/TA0/CA7	27	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output / Comparator_A input
P3.0/UCB0STE/ UCA0CLK	28	I/O	General-purpose digital I/O / USCI_B0 slave transmit enable / USCI A0 clock input/output
P3.1/UCB0SIMO/UCB0SDA	29	I/O	General-purpose digital I/O / USCI_B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/ UCB0SCL	30	I/O	General-purpose digital I/O / USCI_B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/UCA0STE	31	I/O	General-purpose digital I/O / USCI_B0 clock input/output, USCI A0 slave transmit enable
P3.4/UCA0TXD/UCA0SIMO	32	I/O	General-purpose digital I/O / USCI_A- transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	33	I/O	General-purpose digital I/O / USCI_A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6/UCA1TXD/UCA1SIMO	34	I/O	General-purpose digital I/O / USCI_A1 transmit data output in UART mode, slave data in/master out in SPI mode
P3.7/UCA1RXD/ UCA1SOMI	35	I/O	General-purpose digital I/O / USCI_A1 receive data input in UART mode, slave data out/master in in SPI mode
P4.0/TB0	36	I/O	General-purpose digital I/O / Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O / Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O / Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3/TB3	39	I/O	General-purpose digital I/O / Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4	40	I/O	General-purpose digital I/O / Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5	41	I/O	General-purpose digital I/O / Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6	42	I/O	General-purpose digital I/O / Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O / Timer_B, clock signal TBCLK input
P5.0/UCB1STE/UCA1CLK	44	I/O	General-purpose digital I/O / USCI_B1 slave transmit enable / USCI_A1 clock input/output
P5.1/UCB1SIMO/UCB1SDA	45	I/O	General-purpose digital I/O / USCI_B1 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P5.2/UCB1SOMI/UCB1SCL	46	I/O	General-purpose digital I/O / USCI_B1 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P5.3/UCB1CLK/UCA1STE	47	I/O	General-purpose digital I/O / USCI_B1 clock input/output, USCI_A1 slave transmit enable
P5.4/MCLK	48	I/O	General-purpose digital I/O / main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O / submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O / auxiliary clock ACLK output
P5.7/TBOUTH/SVSOUT	51	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance - Timer_B TB0 to TB6/SVS comparator output
P6.0/A0	59	I/O	General-purpose digital I/O / analog input A0 - 12-bit ADC

Table 3. Terminal Functions, MSP430F24x, MSP430F2410 (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P6.1/A1	60	I/O	General-purpose digital I/O / analog input A1 - 12-bit ADC
P6.2/A2	61	I/O	General-purpose digital I/O / analog input A2 - 12-bit ADC
P6.3/A3	2	I/O	General-purpose digital I/O / analog input A3 - 12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O / analog input A4 - 12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O / analog input A5 - 12-bit ADC
P6.6/A6	5	I/O	General-purpose digital I/O / analog input A6 - 12-bit ADC
P6.7/A7/SVSIN	6	I/O	General-purpose digital I/O / analog input A7 - 12-bit ADC/SVS input
XT2OUT	52	O	Output of crystal oscillator XT2
XT2IN	53	I	Input for crystal oscillator XT2
RST/NMI	58	I	Reset input, nonmaskable interrupt input, or bootstrap loader start (in flash devices)
TCK	57	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start.
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output. TDO/TDI data output or programming data input terminal.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
V_{eREF+}	10	I	Input for an external reference voltage
V_{REF+}	7	O	Positive output of the reference voltage in the ADC12
V_{REF-}/V_{eREF-}	11	I	Negative input for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output for crystal oscillator XT1. Standard or watch crystals can be connected.
QFN Pad	NA	NA	QFN package pad connection to DV_{SS} recommended (RGC package only)

Table 4. Terminal Functions, MSP430F24x1

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AV_{CC}	64		Analog supply voltage, positive. Supplies only the analog portion of ADC12.
AV_{SS}	62		Analog supply voltage, negative. Supplies only the analog portion of ADC12.
DV_{CC}	1		Digital supply voltage, positive. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative. Supplies all digital parts.
P1.0/TACLK/CAOUT	12	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / Comparator_A output
P1.1/TA0	13	I/O	General-purpose digital I/O / Timer_A, capture: CCI0A input, compare: Out0 output / BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O / Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O / Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O / SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	I/O	General-purpose digital I/O / ACLK output/Comparator_A input
P2.1/TAINCLK/CA3	21	I/O	General-purpose digital I/O / Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0/CA4	22	I/O	General-purpose digital I/O / Timer_A, capture: CCI0B input / Comparator_A output/BSL receive/Comparator_A input
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output / Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output / Comparator_A input
P2.5/R_{OSC}/CA5	25	I/O	General-purpose digital I/O / input for external resistor defining the DCO nominal frequency / Comparator_A input
P2.6/ADC12CLK/CA6	26	I/O	General-purpose digital I/O / conversion clock - 12-bit ADC / Comparator_A input
P2.7/TA0/CA7	27	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output/Comparator_A input
P3.0/UCB0STE/ UCA0CLK	28	I/O	General-purpose digital I/O / USCI_B0 slave transmit enable/USCI A0 clock input/output
P3.1/UCB0SIMO/UCB0SDA	29	I/O	General-purpose digital I/O / USCI_B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/ UCB0SCL	30	I/O	General-purpose digital I/O / USCI_B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/UCA0STE	31	I/O	General-purpose digital I/O / USCI_B0 clock input/output, USCI A0 slave transmit enable
P3.4/UCA0TXD/UCA0SIMO	32	I/O	General-purpose digital I/O / USCI_A0 transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	33	I/O	General-purpose digital I/O / USCI_A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6/UCA1TXD/UCA1SIMO	34	I/O	General-purpose digital I/O / USCI_A1 transmit data output in UART mode, slave data in/master out in SPI mode
P3.7/UCA1RXD/ UCA1SOMI	35	I/O	General-purpose digital I/O / USCI_A1 receive data input in UART mode, slave data out/master in in SPI mode
P4.0/TB0	36	I/O	General-purpose digital I/O / Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O / Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O / Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3/TB3	39	I/O	General-purpose digital I/O / Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4	40	I/O	General-purpose digital I/O / Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5	41	I/O	General-purpose digital I/O / Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6	42	I/O	General-purpose digital I/O / Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O / Timer_B, clock signal TBCLK input
P5.0/UCB1STE/UCA1CLK	44	I/O	General-purpose digital I/O / USCI_B1 slave transmit enable/USCI_A1 clock input/output
P5.1/UCB1SIMO/UCB1SDA	45	I/O	General-purpose digital I/O / USCI_B1 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P5.2/UCB1SOMI/UCB1SCL	46	I/O	General-purpose digital I/O / USCI_B1 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P5.3/UCB1CLK/UCA1STE	47	I/O	General-purpose digital I/O / USCI_B1 clock input/output, USCI_A1 slave transmit enable
P5.4/MCLK	48	I/O	General-purpose digital I/O / main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O / submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O / auxiliary clock ACLK output
P5.7/TBOUTH/SVSOUT	51	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance - Timer_B TB0 to TB6/SVS comparator output
P6.0	59	I/O	General-purpose digital I/O

Table 4. Terminal Functions, MSP430F24x1 (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P6.1	60	I/O	General-purpose digital I/O
P6.2	61	I/O	General-purpose digital I/O
P6.3	2	I/O	General-purpose digital I/O
P6.4	3	I/O	General-purpose digital I/O
P6.5	4	I/O	General-purpose digital I/O
P6.6	5	I/O	General-purpose digital I/O
P6.7/SVSIN	6	I/O	General-purpose digital I/O / SVS input
XT2OUT	52	O	Output terminal of crystal oscillator XT2
XT2IN	53	I	Input port for crystal oscillator XT2
RST/NMI	58	I	Reset input, nonmaskable interrupt input, or bootstrap loader start (in flash devices).
TCK	57	I	Test clock (JTAG). TCK is the clock input for device programming test and bootstrap loader start.
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output. TDO/TDI data output or programming data input terminal.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
DV_{SS}	10	I	Connected to DV_{SS}
Reserved	7	O	Reserved, do not connect externally
DV_{SS}	11	I	Connected to DV_{SS}
XIN	8	I	Input for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output for crystal oscillator XT1. Standard or watch crystals can be connected.
QFN Pad	NA	NA	QFN package pad connection to DV_{SS} recommended (RGC package only)

SHORT-FORM DESCRIPTION

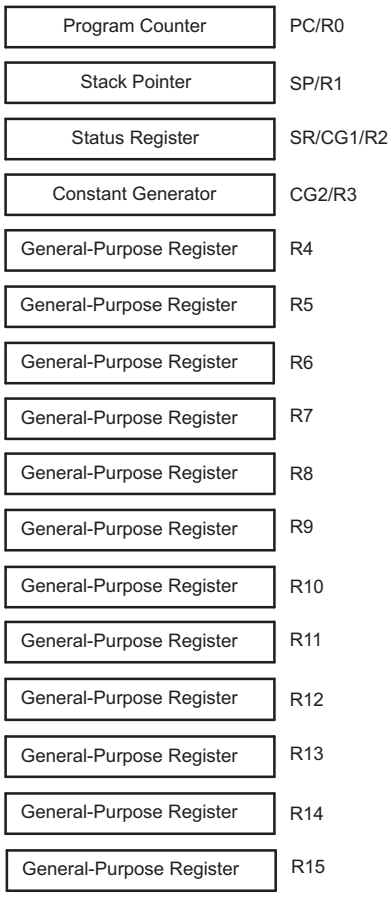
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 5 shows examples of the three types of instruction formats; Table 6 shows the address modes.

Table 5. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional/conditional	JNE	Jump-on-equal bit = 0

Table 6. Address Mode Descriptions

ADDRESS MODE	S (1)	D (2)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
  - DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - Crystal oscillator is stopped.

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. If the reset vector (0xFFFE) contains 0xFFFF (for example, if flash is not programmed) the CPU enters LPM4 after power-up.

Table 7. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out of range(1)	PORIFG WDTIFG RSTIFG KEYV (see (2))	Reset	0xFFFE	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(Non)maskable (Non)maskable (Non)maskable	0xFFFC	30
Timer_B7(4)	TBCCR0 CCIFG(5)	Maskable	0xFFFA	29
Timer_B7(4)	TBCCR1 to TBCCR6 CCIFGs, TBIFG(2)(5)	Maskable	0xFFF8	28
Comparator_A+	CAIFG	Maskable	0xFFF6	27
Watchdog timer+	WDTIFG	Maskable	0xFFF4	26
Timer_A3	TACCR0 CCIFG(5)	Maskable	0xFFF2	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG TAIFG(2)(5)	Maskable	0xFFF0	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(6)	Maskable	0xFFEE	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive / transmit	UCA0TXIFG, UCB0TXIFG(2)(7)	Maskable	0xFFEC	22
ADC12(8)	ADC12IFG(2)(5)	Maskable	0xFFEA	21
			0xFFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(2)(5)	Maskable	0xFFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(2)(5)	Maskable	0xFFE4	18
USCI_A1/USCI_B1 receive USCI_B1 I2C status	UCA1RXIFG, UCB1RXIFG(2)(6)	Maskable	0xFFE2	17
USCI_A1/USCI_B1 transmit USCI_B1 I2C receive / transmit	UCA1TXIFG, UCB1TXIFG(2)(7)	Maskable	0xFFE0	16
Reserved(9)(10)	Reserved		0xFFDE to 0xFFC0	15 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0x0000 to 0x01FF) or from within unused address range.
(2) Multiple source flags
(3) (Non)maskable: The individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot.
(4) Timer_B7 in MSP430F24x(1)/MSP430F2410 family has seven CCRs, Timer_B3 in MSP430F23x family has three CCRs. In Timer_B3, there are only interrupt flags TBCCR0 CCIFG, TBCCR1 CCIFG, and TBCCR2 CCIFG, and the interrupt enable bits TBCCTL0 CCIE, TBCCTL1 CCIE, and TBCCTL2 CCIE.
(5) Interrupt flags are located in the module.
(6) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(7) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(8) ADC12 is not implemented in the MSP430F24x1 family.
(9) The address 0xFFDE is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero disables the erasure of the flash if an invalid password is supplied.
(10) The interrupt vectors at addresses 0xFFDE to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

Legend

rw	Bit can be read and written.
rw-0, 1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), (1)	Bit can be read and written. It is Reset or Set by POR.
	SFR bit is not present in device.

Table 8. Interrupt Enable 1

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Table 9. Interrupt Enable 2

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable

Table 10. Interrupt Flag Register 1

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.
PORIFG	Power-on reset interrupt flag. Set on V_{CC} power up.
NMIIFG	Set via $\overline{RST}$/NMI pin

Table 11. Interrupt Flag Register 2

Address	7	6	5	4	3	2	1	0
03h					UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG	USCI_A0 receive-interrupt flag
UCA0TXIFG	USCI_A0 transmit-interrupt flag
UCB0RXIFG	USCI_B0 receive-interrupt flag
UCB0TXIFG	USCI_B0 transmit-interrupt flag

Memory Organization

Table 12. Memory Organization

		MSP430F233	MSP430F235	MSP430F249 MSP430F2491
Memory Main: interrupt vector Main: code memory	Size Flash Flash	8KB 0xFFFF to 0xFFC0 0xFFFF to 0xE000	16KB 0xFFFF to 0xFFC0 0xFFFF to 0xC000	60KB 0xFFFF to 0xFFC0 0xFFFF to 0x1100
RAM (Total)	Size	1KB 0x05FF to 0x0200	2KB 0x09FF to 0x0200	2KB 0x09FF to 0x0200
Information memory	Size Flash	256 Byte 0x10FF to 0x1000	256 Byte 0x10FF to 0x1000	256 Byte 0x10FF to 0x1000
Boot memory	Size ROM	1KB 0x0FFF to 0x0C00	1KB 0x0FFF to 0x0C00	1KB 0x0FFF to 0x0C00
RAM	Size	1KB 0x05FF to 0x0200	2KB 0x09FF to 0x0200	2KB 0x09FF to 0x0200
Peripherals	16 bit 8 bit SFR	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000

		MSP430F247 MSP430F2471	MSP430F248 MSP430F2481	MSP430F2410
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32KB 0xFFFF to 0xFFC0 0xFFFF to 0x8000	48KB 0xFFFF to 0xFFC0 0xFFFF to 0x4000	56KB 0xFFFF to 0xFFC0 0xFFFF to 0x2100
RAM (total)	Size	4KB 0x20FF to 0x1100	4KB 0x20FF to 0x1100	4KB 0x20FF to 0x1100
Extended	Size	2KB 0x20FF to 0x1900	2KB 0x20FF to 0x1900	2KB 0x20FF to 0x1900
Mirrored	Size	2KB 0x18FF to 0x1100	2KB 0x18FF to 0x1100	2KB 0x18FF to 0x1100
Information memory	Size Flash	256 Byte 0x10FF to 0x1000	256 Byte 0x10FF to 0x1000	256 Byte 0x10FF to 0x1000
Boot memory	Size ROM	1KB 0x0FFF to 0x0C00	1KB 0x0FFF to 0x0C00	1KB 0x0FFF to 0x0C00
RAM (mirrored at 0x18FF to 0x1100)	Size	2KB 0x09FF to 0x0200	2KB 0x09FF to 0x0200	2KB 0x09FF to 0x0200
Peripherals	16 bit 8 bit SFR	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000

Bootstrap Loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 13. BSL Function Pins

BSL FUNCTION	PM, RGC PACKAGE PINS
Data transmit	13 - P1.1
Data receive	22 - P2.2

Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or the internal very-low-power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

Calibration Data Stored in Information Memory Segment A

Calibration data is stored for the DCO and for the ADC12. It is organized in a tag-length-value (TLV) structure.

Table 14. Tags Used by the ADC Calibration Tags

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3 V andT_A = 25°C at calibration
TAG_ADC12_1	0x10DA	0x10	ADC12_1 calibration tag
TAG_EMPTY	-	0xFE	Identifier for empty memory areas

Table 15. Labels Used by the ADC Calibration Tags

LABEL	CONDITION AT CALIBRATION / DESCRIPTION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010, REF2_5 = 1, T_A = 85°C	word	0x000E
CAL_ADC_25T30	INCHx = 0x1010, REF2_5 = 1, T_A = 30°C	word	0x000C
CAL_ADC_25VREF_FACTOR	REF2_5 = 1, T_A = 30°C, I_{VREF+} = 1.0 mA	word	0x000A
CAL_ADC_15T85	INCHx = 0x1010, REF2_5 = 0, T_A = 85°C	word	0x0008
CAL_ADC_15T30	INCHx = 0x1010, REF2_5 = 0, T_A = 30°C	word	0x0006
CAL_ADC_15VREF_FACTOR	REF2_5 = 0, T_A = 30°C, I_{VREF+} = 0.5 mA	word	0x0004
CAL_ADC_OFFSET	External Vref = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	word	0x0002
CAL_ADC_GAIN_FACTOR	External Vref = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	word	0x0000
CAL_BC1_1MHZ	-	byte	0x0007
CAL_DCO_1MHZ	-	byte	0x0006
CAL_BC1_8MHZ	-	byte	0x0005
CAL_DCO_8MHZ	-	byte	0x0004
CAL_BC1_12MHZ	-	byte	0x0003
CAL_DCO_12MHZ	-	byte	0x0002
CAL_BC1_16MHZ	-	byte	0x0001
CAL_DCO_16MHZ	-	byte	0x0000

Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

Digital I/O

There are up to six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 16. Timer_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DV_{SS}	GND			27 - P2.7
	DV_{CC}	V_{CC}			
14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2
	CAOUT (internal)	CCI1B			18 - P1.6
	DV_{SS}	GND			23 - P2.3
	DV_{CC}	V_{CC}			ADC12(1) (internal)
15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3
	ACLK (internal)	CCI2B			19 - P1.7
	DV_{SS}	GND			24 - P2.4
	DV_{CC}	V_{CC}			

(1) Not available in the MSP430F24x1 devices.

Timer_B7 (MSP430F24x(1) and MSP430F2410 Devices)

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 17. Timer_B7 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	TBCLK	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12(1) (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12(2) (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

(1) Not available in the MSP430F24x1 devices.
(2) Not available in the MSP430F24x1 devices.

Timer_B3 (MSP430F23x Devices)

Timer_B3 is a 16-bit timer/counter with seven capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 18. Timer_B3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	TBCLK	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

Universal Serial Communications Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols, such as SPI (3 or 4 pin) or I^2C, and asynchronous combination protocols, such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

The USCI A module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

The USCI B module provides support for SPI (3 or 4 pin) and I^2C.

Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12 (MSP430F23x, MSP430F24x, and MSP430F2410 Devices)

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

Peripheral File Map

Table 19. Peripheral File Map

MODULE	REGISTER NAME	SHORT FORM	ADDRESS
ADC12 (MSP430F24x, MSP430F2410, and MSP430F23x)	Interrupt-vector-word register	ADC12IV	0x01A8
	Interrupt-enable register	ADC12IE	0x01A6
	Interrupt-flag register	ADC12IFG	0x01A4
	Control register 1	ADC12CTL1	0x01A2
	Control register 0	ADC12CTL0	0x01A0
	Conversion memory 15	ADC12MEM15	0x015E
	Conversion memory 14	ADC12MEM14	0x015C
	Conversion memory 13	ADC12MEM13	0x015A
	Conversion memory 12	ADC12MEM12	0x0158
	Conversion memory 11	ADC12MEM11	0x0156
	Conversion memory 10	ADC12MEM10	0x0154
	Conversion memory 9	ADC12MEM9	0x0152
	Conversion memory 8	ADC12MEM8	0x0150
	Conversion memory 7	ADC12MEM7	0x014E
	Conversion memory 6	ADC12MEM6	0x014C
	Conversion memory 5	ADC12MEM5	0x014A
	Conversion memory 4	ADC12MEM4	0x0148
	Conversion memory 3	ADC12MEM3	0x0146
	Conversion memory 2	ADC12MEM2	0x0144
	Conversion memory 1	ADC12MEM1	0x0142
	Conversion memory 0	ADC12MEM0	0x0140
	ADC memory-control register15	ADC12MCTL15	0x008F
	ADC memory-control register14	ADC12MCTL14	0x008E
	ADC memory-control register13	ADC12MCTL13	0x008D
	ADC memory-control register12	ADC12MCTL12	0x008C
	ADC memory-control register11	ADC12MCTL11	0x008B
	ADC memory-control register10	ADC12MCTL10	0x008A
	ADC memory-control register9	ADC12MCTL9	0x0089
	ADC memory-control register8	ADC12MCTL8	0x0088
	ADC memory-control register7	ADC12MCTL7	0x0087
	ADC memory-control register6	ADC12MCTL6	0x0086
	ADC memory-control register5	ADC12MCTL5	0x0085
	ADC memory-control register4	ADC12MCTL4	0x0084
	ADC memory-control register3	ADC12MCTL3	0x0083
	ADC memory-control register2	ADC12MCTL2	0x0082
	ADC memory-control register1	ADC12MCTL1	0x0081
	ADC memory-control register0	ADC12MCTL0	0x0080

Table 19. Peripheral File Map (continued)

MODULE	REGISTER NAME	SHORT FORM	ADDRESS
Timer_B7 (MSP430F24x(1) and MSP430F2410)	Capture/compare register 6	TBCCR6	0x019E
	Capture/compare register 5	TBCCR5	0x019C
	Capture/compare register 4	TBCCR4	0x019A
	Capture/compare register 3	TBCCR3	0x0198
	Capture/compare register 2	TBCCR2	0x0196
	Capture/compare register 1	TBCCR1	0x0194
	Capture/compare register 0	TBCCR0	0x0192
	Timer_B register	TBR	0x0190
	Capture/compare control 6	TBCCTL6	0x018E
	Capture/compare control 5	TBCCTL5	0x018C
	Capture/compare control 4	TBCCTL4	0x018A
	Capture/compare control 3	TBCCTL3	0x0188
	Capture/compare control 2	TBCCTL2	0x0186
	Capture/compare control 1	TBCCTL1	0x0184
	Capture/compare control 0	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E
Timer_B3 (MSP430F23x)	Capture/compare register 2	TBCCR2	0x0196
	Capture/compare register 1	TBCCR1	0x0194
	Capture/compare register 0	TBCCR0	0x0192
	Timer_B register	TBR	0x0190
	Capture/compare control 2	TBCCTL2	0x0186
	Capture/compare control 1	TBCCTL1	0x0184
	Capture/compare control 0	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E
Timer_A3	Capture/compare register 2	TACCR2	0x0176
	Capture/compare register 1	TACCR1	0x0174
	Capture/compare register 0	TACCR0	0x0172
	Timer_A register	TAR	0x0170
	Reserved		0x016E
	Reserved		0x016C
	Reserved		0x016A
	Reserved		0x0168
	Capture/compare control 2	TACCTL2	0x0166
	Capture/compare control 1	TACCTL1	0x0164
	Capture/compare control 0	TACCTL0	0x0162
	Timer_A control	TACTL	0x0160
	Timer_A interrupt vector	TAIV	0x012E
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed + accumulate/operand1	MACS	0x0136
	Multiply + accumulate/operand1	MAC	0x0134
	Multiply signed/operand1	MPYS	0x0132
	Multiply unsigned/operand1	MPY	0x0130

Table 19. Peripheral File Map (continued)

MODULE	REGISTER NAME	SHORT FORM	ADDRESS
Flash	Flash control 4	FCTL4	0x01BE
	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog	Watchdog Timer control	WDTCTL	0x0120
USCI A0/B0	USCI A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI A0 transmit buffer	UCA0TXBUF	0x0067
	USCI A0 receive buffer	UCA0RXBUF	0x0066
	USCI A0 status	UCA0STAT	0x0065
	USCI A0 modulation control	UCA0MCTL	0x0064
	USCI A0 baud rate control 1	UCA0BR1	0x0063
	USCI A0 baud rate control 0	UCA0BR0	0x0062
	USCI A0 control 1	UCA0CTL1	0x0061
	USCI A0 control 0	UCA0CTL0	0x0060
	USCI A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI A0 IrDA transmit control	UCA0IRTCLT	0x005E
	USCI B0 transmit buffer	UCB0TXBUF	0x006F
	USCI B0 receive buffer	UCB0RXBUF	0x006E
	USCI B0 status	UCB0STAT	0x006D
	USCI B0 I2C Interrupt enable	UCB0CIE	0x006C
	USCI B0 baud rate control 1	UCB0BR1	0x006B
	USCI B0 baud rate control 0	UCB0BR0	0x006A
	USCI B0 control 1	UCB0CTL1	0x0069
	USCI B0 control 0	UCB0CTL0	0x0068
	USCI B0 I2C slave address	UCB0SA	0x011A
	USCI B0 I2C own address	UCB0OA	0x0118

Table 19. Peripheral File Map (continued)

MODULE	REGISTER NAME	SHORT FORM	ADDRESS
USCI A1/B1 (MSP430F24x(1) and MSP430F2410)	USCI A1 auto baud rate control	UCA1ABCTL	0x00CD
	USCI A1 transmit buffer	UCA1TXBUF	0x00D7
	USCI A1 receive buffer	UCA1RXBUF	0x00D6
	USCI A1 status	UCA1STAT	0x00D5
	USCI A1 modulation control	UCA1MCTL	0x00D4
	USCI A1 baud rate control 1	UCA1BR1	0x00D3
	USCI A1 baud rate control 0	UCA1BR0	0x00D2
	USCI A1 control 1	UCA1CTL1	0x00D1
	USCI A1 control 0	UCA1CTL0	0x00D0
	USCI A1 IrDA receive control	UCA1IRRCTL	0x00CF
	USCI A1 IrDA transmit control	UCA1IRTCLT	0x00CE
	USCI B1 transmit buffer	UCB1TXBUF	0x00DF
	USCI B1 receive buffer	UCB1RXBUF	0x00DE
	USCI B1 status	UCB1STAT	0x00DD
	USCI B1 I2C Interrupt enable	UCB1CIE	0x00DC
	USCI B1 baud rate control 1	UCB1BR1	0x00DB
	USCI B1 baud rate control 0	UCB1BR0	0x00DA
	USCI B1 control 1	UCB1CTL1	0x00D9
	USCI B1 control 0	UCB1CTL0	0x00D8
	USCI B1 I2C slave address	UCB1SA	0x017E
	USCI B1 I2C own address	UCB1OA	0x017C
	USCI A1/B1 interrupt enable	UC1IE	0x0006
	USCI A1/B1 interrupt flag	UC1IFG	0x0007
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control2	CACTL2	0x005A
	Comparator_A control1	CACTL1	0x0059
Basic Clock	Basic clock system control3	BCSCTL3	0x0053
	Basic clock system control2	BCSCTL2	0x0058
	Basic clock system control1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	0x0055
Port P6	Port P6 resistor enable	P6REN	0x0013
	Port P6 selection	P6SEL	0x0037
	Port P6 direction	P6DIR	0x0036
	Port P6 output	P6OUT	0x0035
	Port P6 input	P6IN	0x0034
Port P5	Port P5 resistor enable	P5REN	0x0012
	Port P5 selection	P5SEL	0x0033
	Port P5 direction	P5DIR	0x0032
	Port P5 output	P5OUT	0x0031
	Port P5 input	P5IN	0x0030
Port P4	Port P4 resistor enable	P4REN	0x0011
	Port P4 selection	P4SEL	0x001F
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C

Table 19. Peripheral File Map (continued)

MODULE	REGISTER NAME	SHORT FORM	ADDRESS
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt-edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt-edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Functions	SFR interrupt flag2	IFG2	0x0003
	SFR interrupt flag1	IFG1	0x0002
	SFR interrupt enable2	IE2	0x0001
	SFR interrupt enable1	IE1	0x0000

Absolute Maximum Ratings(1)

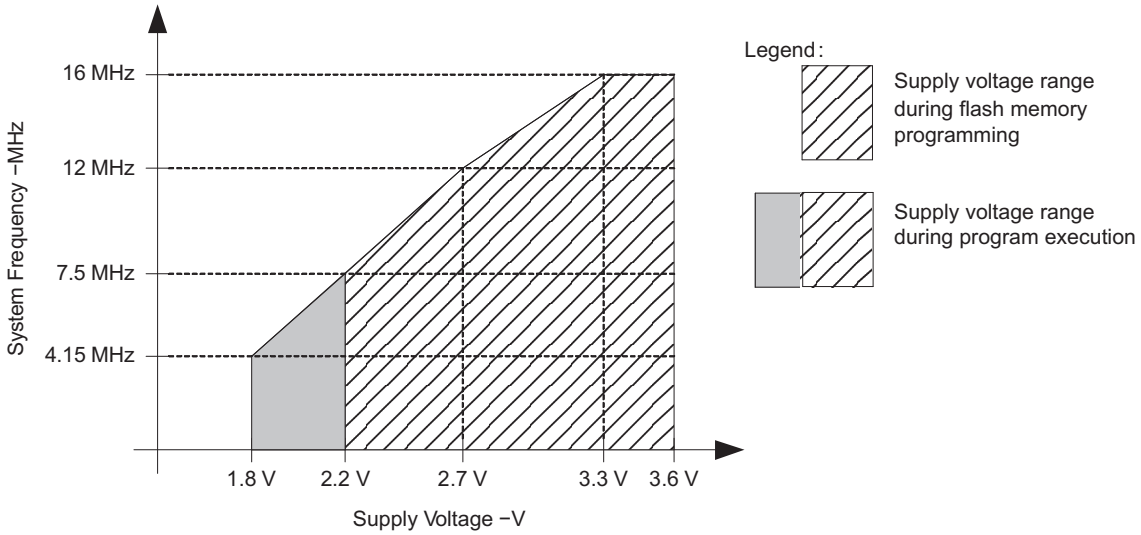
Voltage applied at V_{CC} to V_{SS}		-0.3 V to 4.1 V
Voltage applied to any pin (2)		-0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal		±2 mA
Storage temperature, T_{stg} (3)	Unprogrammed device	-55°C to 150°C
	Programmed device	-55°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions(1)(2)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(3)	$AV_{CC} = DV_{CC} = V_{CC}$	During program execution	1.8		3.6	V
			During program/erase flash memory	2.2		3.6	V
V_{SS}	Supply voltage	$AV_{SS} = DV_{SS} = V_{SS}$			0		V
T_A	Operating free-air temperature		I version	-40		85	°C
			T version	-40		105	
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2) (see Figure 1)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%		dc		4.15	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ±10%		dc		12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%		dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(3) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power-up.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

Active Mode Supply Current (Into DV_{CC} + AV_{CC}) Excluding External Current[1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		275	312	µA
			105°C			295	318	
			-40°C to 85°C	3 V		386	445	
			105°C			417	449	
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		230	261	µA
			105°C			248	267	
			-40°C to 85°C	3.3 V		321	366	
			105°C			344	370	
$I_{AM,4kHz}$	Active mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32768 Hz/8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		1.5	3.8	µA
			105°C			6	10.5	
			-40°C to 85°C	3 V		2	4.7	
			105°C			7	12.2	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		55	72	µA
			105°C			70	81	
			-40°C to 85°C	3 V		67	89	
			105°C			84	100	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics - Active-Mode Supply Current (Into DV_{CC} + AV_{CC})

ACTIVE-MODE CURRENT
vs
SUPPLY VOLTAGE
T_A = 25°C

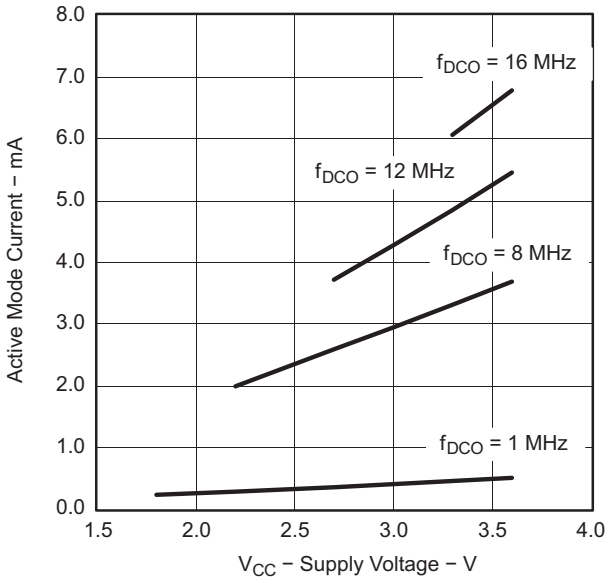


Figure 2.

ACTIVE-MODE CURRENT
vs
DCO FREQUENCY

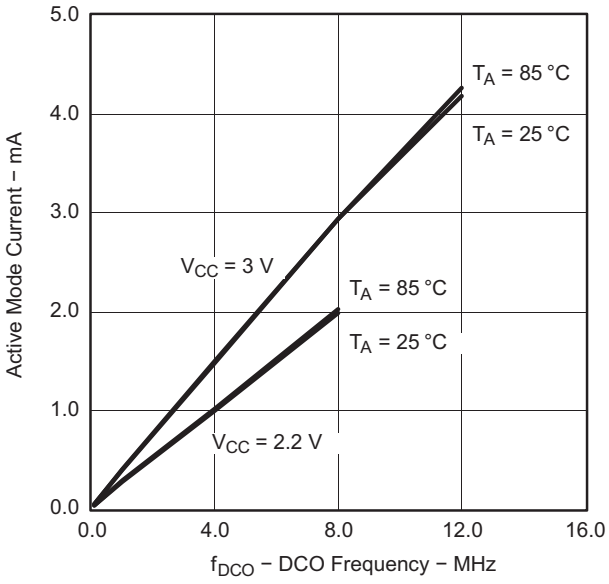


Figure 3.

Low-Power-Mode Supply Currents (Into V_{CC}) Excluding External Current[1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current[3]	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		60	65	µA
			105°C			63	72	
			-40°C to 85°C	3 V		75	90	
			105°C			80	95	
$I_{LPM0,100kHz}$	Low-power mode 0 (LPM0) current[3]	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO(0, 0)} \approx 100$ kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		33	38	µA
			105°C			36	43	
			-40°C to 85°C	3 V		36	42	
			105°C			40	47	
I_{LPM2}	Low-power mode 2 (LPM2) current[4]	$f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		20	25	µA
			105°C			25	30	
			-40°C to 85°C	3 V		23	30	
			105°C			28	35	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current[4]	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.8	1.2	µA
			25°C			0.9	1.3	
			85°C			2.4	3	
			105°C			6	13	
			-40°C	3 V		0.9	1.3	
			25°C			1	1.4	
			85°C			3.9	4.3	
			105°C			10	15	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3)[4]	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.3	0.9	µA
			25°C			0.3	0.9	
			85°C			1.8	2.4	
			105°C			5.5	13	
			-40°C	3 V		0.4	1	
			25°C			0.4	1	
			85°C			2	3	
			105°C			9	15	
I_{LPM4}	Low-power mode 4 (LPM4) current[5]	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V/3 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			1.6	2.5	
			105°C			6.5	13	

(1) All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
(3) Current for Brownout and WDT+ is included. The WDT+ is clocked by SMCLK.
(4) Current for Brownout and WDT+ is included. The WDT+ is clocked by ACLK.
(5) Current for Brownout is included.

Typical Characteristics - LPM4 Current

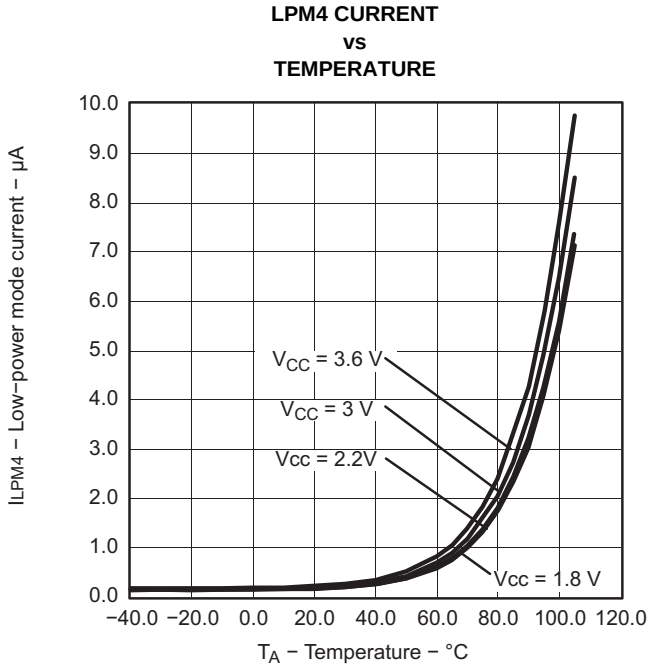


Figure 4.

Schmitt-Trigger Inputs (Ports P1, P2, P3, P4, P5, P6, $\overline{RST}$/NMI, JTAG, XIN, XT2IN)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			2.2 V	1		1.65	
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			2.2 V	0.55		1.20	
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		2.2 V	0.2		1	V
			3 V	0.3		1	
R_{Pull}	Pullup/pulldown resistor	For pullup: V_{IN} = V_{SS}, For pulldown: V_{IN} = V_{CC}	3 V	20	35	50	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}			5		pF

Inputs (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag(1)	2.2 V/3 V	20		ns
t_{cap}	Timer_A Timer_B capture timing	TA0, TA1, TA2	2.2 V	62		ns
		TB0, TB1, TB2, TB3, TB4, TB5, TB6	3 V	50		
f_{TAext}, f_{TBext}	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)}$ = $t_{(L)}$	2.2 V		8	MHz
			3 V		10	
f_{TAint}, f_{TBint}	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
			3 V		10	

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

Leakage Current (Ports P1, P2, P3, P4, P5, P6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	See (1) (2)	2.2 V/3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Standard Inputs ($\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage		2.2 V/3 V	V_{SS}	V_{SS} + 0.6	V
V_{IH}	High-level input voltage		2.2 V/3 V	0.8 V_{CC}	V_{CC}	V

Outputs (Ports P1, P2, P3, P4, P5, P6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = -1.5 mA (1)	2.2 V	V_{CC} - 0.25	V_{CC}	V
		$I_{OH(max)}$ = -6 mA (2)		V_{CC} - 0.6	V_{CC}	
		$I_{OH(max)}$ = -1.5 mA(1)	3 V	V_{CC} - 0.25	V_{CC}	
		$I_{OH(max)}$ = -6 mA(2)		V_{CC} - 0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.6	
		$I_{OL(max)}$ = 1.5 mA(1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{OL(max)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.6	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1, P2, P3, P4, P5, P6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency with load	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ(1)(2)	2.2 V	DC		10	MHz
			3 V	DC		12	
$f_{Port°CLK}$	Clock output frequency	P2.0/ACLK/CA2, P1.4/SMCLK, C_L = 20 pF(2)	2.2 V	DC		12	MHz
			3 V	DC		16	
$t_{(Xdc)}$	Duty cycle of output frequency	P1.0/TACLK/CAOUT, C_L = 20 pF, LF mode		30%	50%	70%	
		P1.0/TACLK/CAOUT, C_L = 20 pF, XT1 mode		40%	50%	60%	
		P1.1/TA0, C_L = 20 pF, XT1 mode		40%		60%	
		P1.1/TA0, C_L = 20 pF, DCO		50% – 15 ns	50%	50% + 15 ns	
		P1.4/SMCLK, C_L = 20 pF, XT2 mode		40%		60%	
		P1.4/SMCLK, C_L = 20 pF, DCO		50% – 15 ns		50% + 15 ns	

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics - Outputs

One output loaded at a time.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

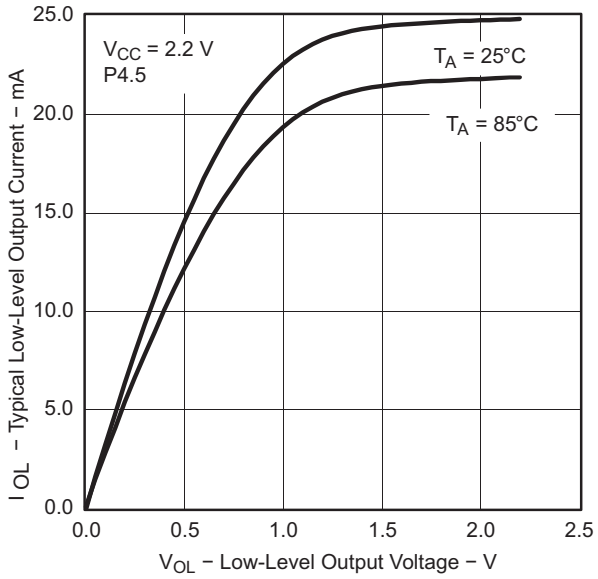


Figure 5.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

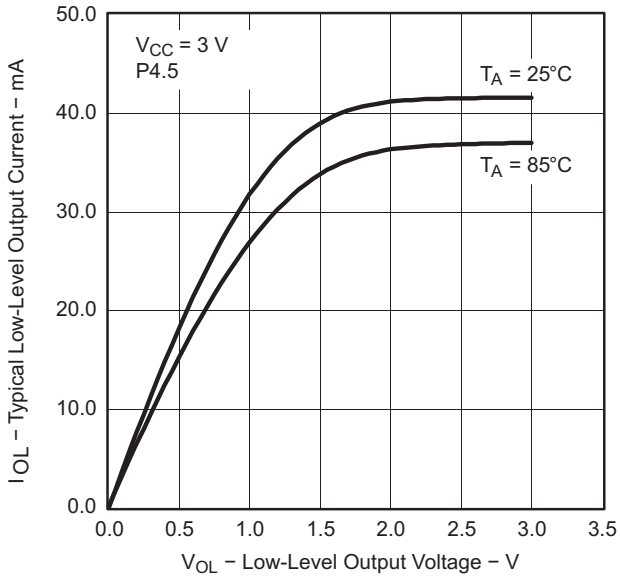


Figure 6.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

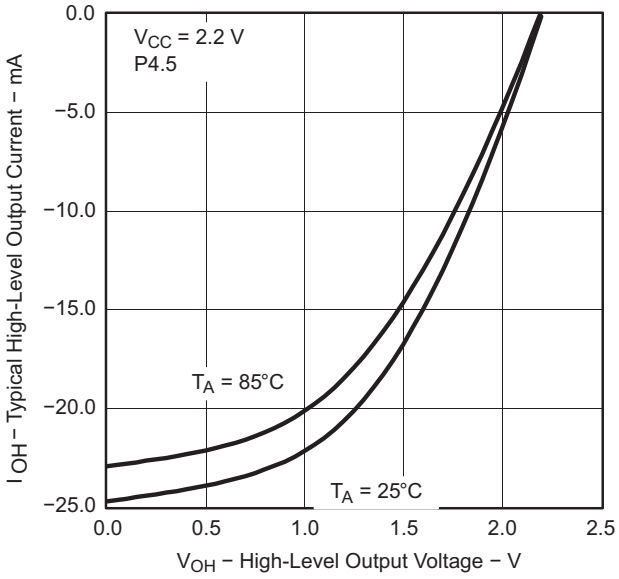


Figure 7.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

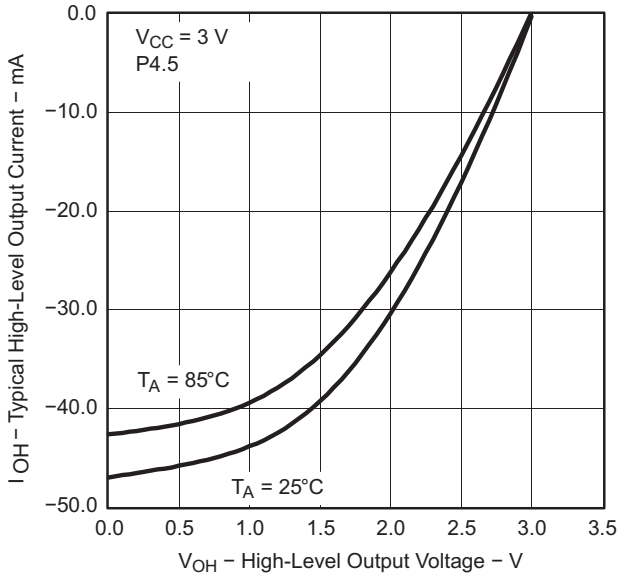


Figure 8.

POR/Brownout Reset (BOR) (1) (2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	Operating voltage	$dV_{CC}/dt \le 3$ V/s				$0.7 \times V_{(B\_IT-)}$	V
$V_{(B\_IT-)}$	Negative going V_{CC} reset threshold voltage	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	V_{CC} reset threshold hysteresis	$dV_{CC}/dt \le 3$ V/s		70	130	210	mV
$t_{d(BOR)}$	BOR reset release delay time					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V/3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

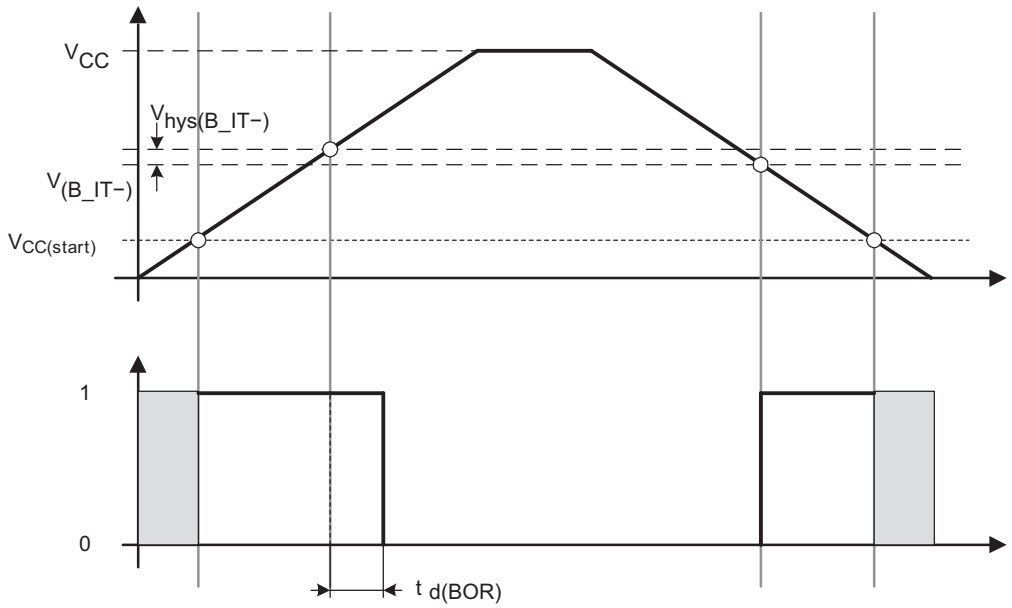


Figure 9. POR/Brownout Reset (BOR) vs Supply Voltage

Typical Characteristics - POR/Brownout Reset (BOR)

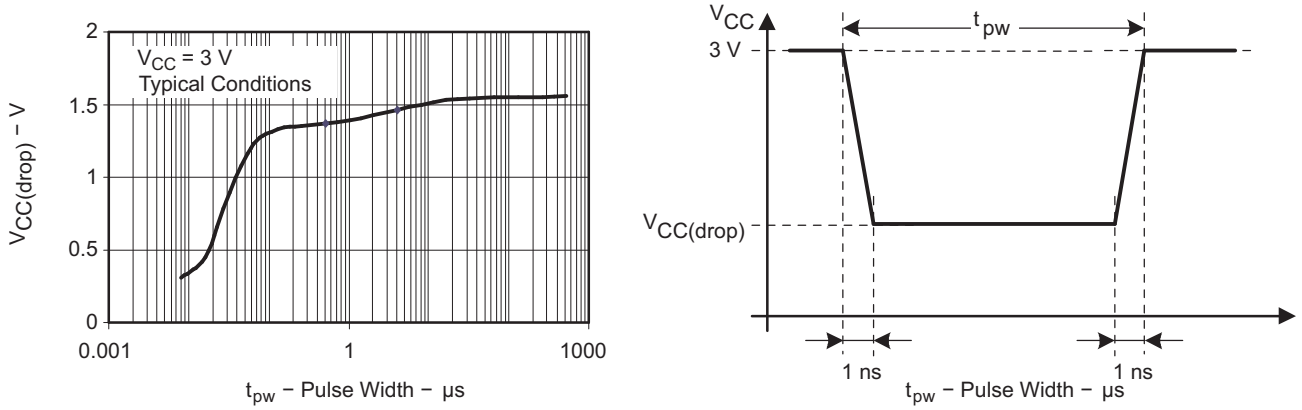


Figure 10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

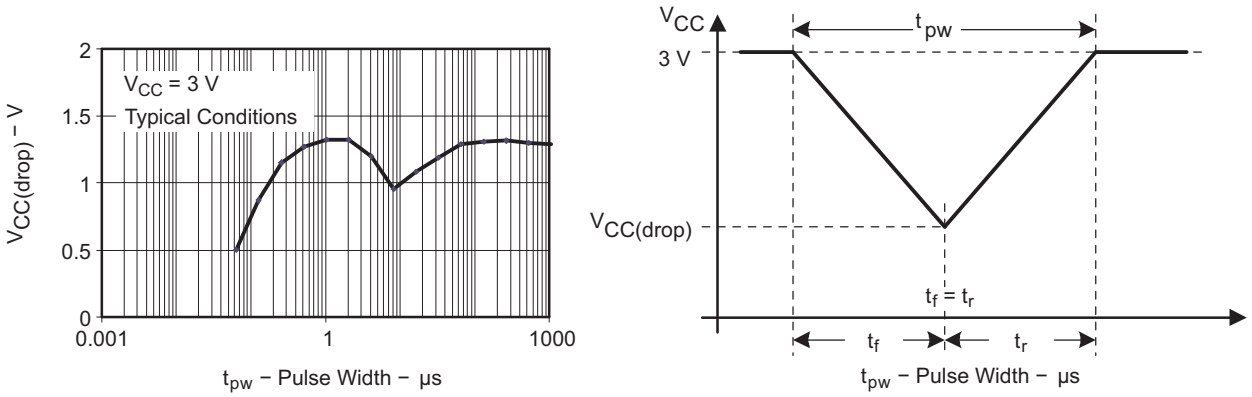


Figure 11. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

SVS (Supply Voltage Supervisor/Monitor)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 12)		1		150	µs
	dV_{CC}/dt ≤ 30 V/ms				2000	
$t_{d(SVSon)}$	SVSon, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V		150		300	µs
t_{settle}	VLD ≠ 0 (1)				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, V_{CC}/dt ≤ 3 V/s (see Figure 12)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 12)	VLD = 1	70	120	155	mV
		VLD = 2 to 14	0.001 × $V_{(SVS\_IT-)}$		0.016 × $V_{(SVS\_IT-)}$	
	V_{CC}/dt ≤ 3 V/s (see Figure 12), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	V_{CC}/dt ≤ 3V/s (see Figure 12 and Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61 (2)	
		VLD = 13	3.24	3.5	3.76 (2)	
		VLD = 14	3.43	3.7 (2)	3.99 (2)	
	V_{CC}/dt ≤ 3 V/s (see Figure 12 and Figure 13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (3)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

(1) t_{settle} is the settling time that the comparator output needs to have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.
(2) The recommended operating voltage range is limited to 3.6 V.
(3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

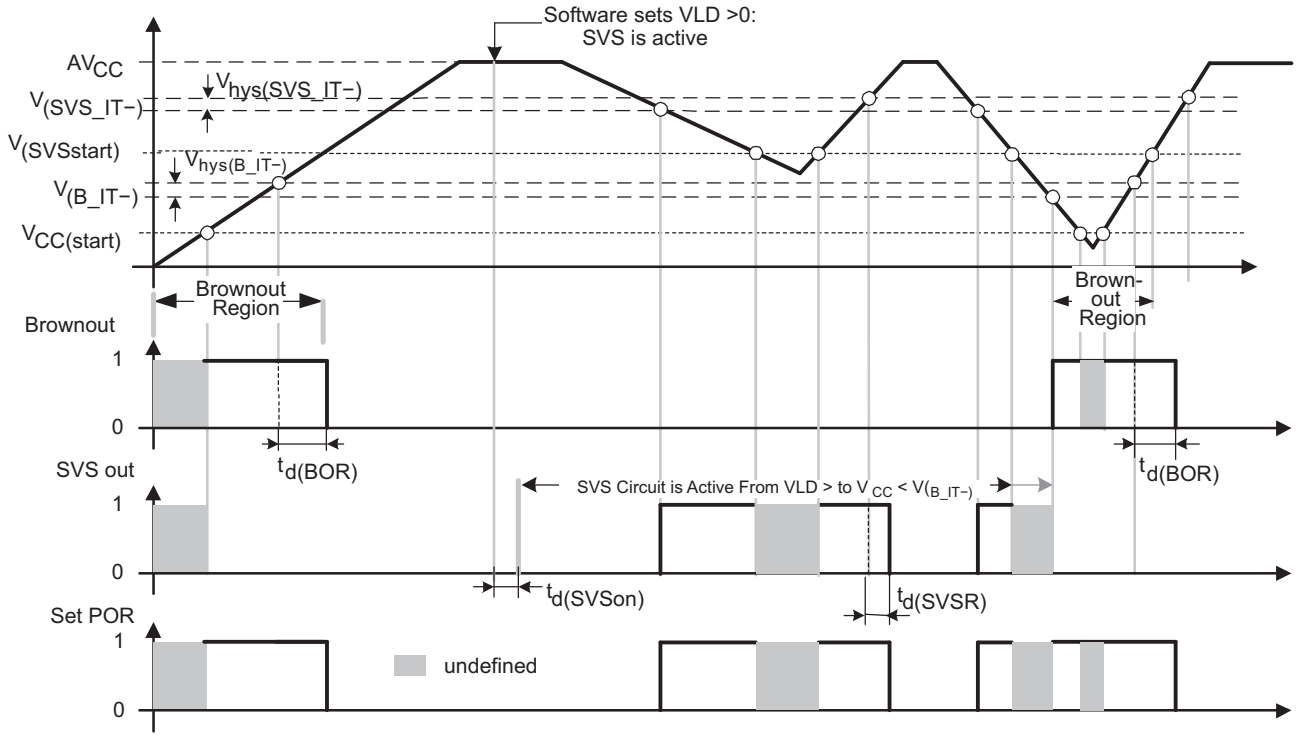


Figure 12. SVS Reset (SVSR) vs Supply Voltage

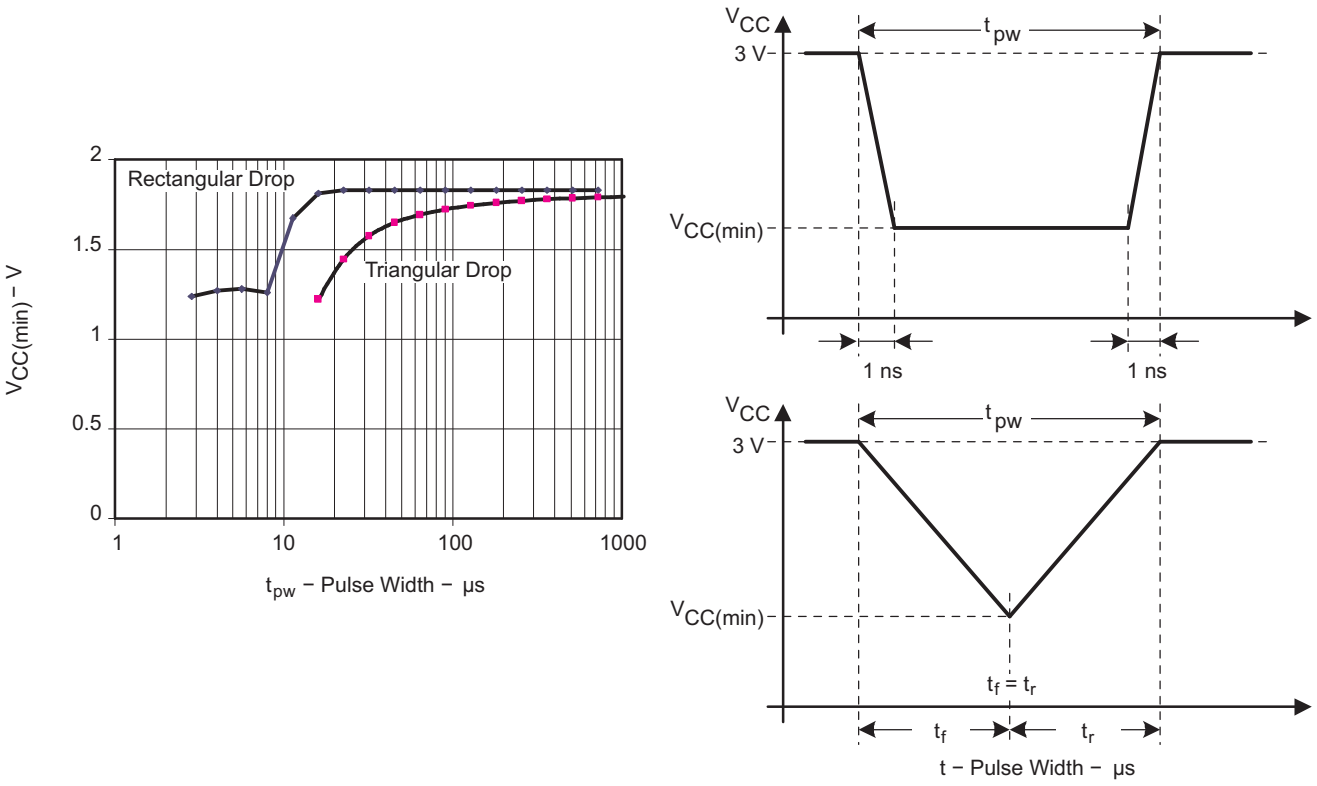


Figure 13. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO} .
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.08	1.12	ratio
	Duty cycle	Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	Frequency tolerance at calibration		25°C	3 V	-1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±0.5	2.5	%
	8-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	2.5	%
	12-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	2.5	%
	16-MHz tolerance over temperature		0°C to 85°C	3 V	-3	±2.0	3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.97	1	1.03	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.97	1	1.03	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.76	8	8.4	MHz
				3 V	7.8	8	8.2	
				3.6 V	7.6	8	8.24	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.64	12	12.36	MHz
				3 V	11.64	12	12.36	
				3.6 V	11.64	12	12.36	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3 V	15.52	16	16.48	MHz
				3.6 V	15	16	16.48	

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
	8-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
	12-MHz tolerance over V_{CC}		25°C	2.2 V to 3.6 V	-3	±2	+3	%
	16-MHz tolerance over V_{CC}		25°C	3 V to 3.6 V	-6	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1	1.03	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8	8.24	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15	16	16.48	MHz

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance overall		-40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
	8-MHz tolerance overall		-40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
	12-MHz tolerance overall		-40°C to 105°C	2.2 V to 3.6 V	-5	±2	+5	%
	16-MHz tolerance overall		-40°C to 105°C	3 V to 3.6 V	-6	±3	+6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	0.95	1	1.05	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	-40°C to 105°C	2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	-40°C to 105°C	3 V to 3.6 V	15	16	17	MHz

Typical Characteristics - Calibrated DCO Frequency

CALIBRATED 1-MHz FREQUENCY vs SUPPLY VOLTAGE

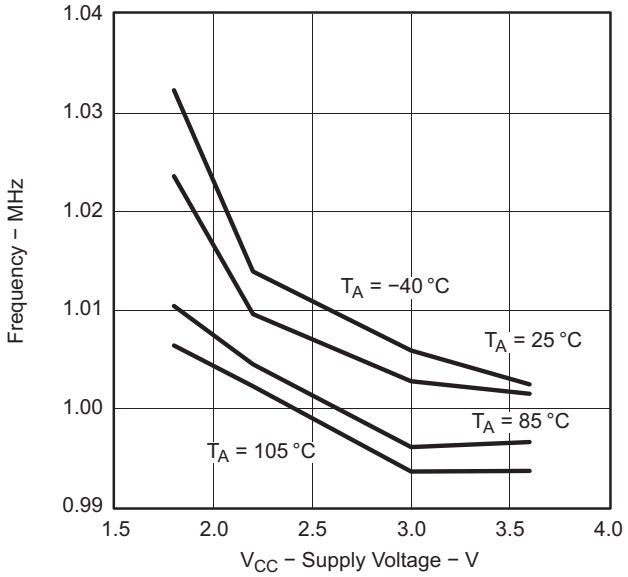


Figure 14.

CALIBRATED 8-MHz FREQUENCY vs SUPPLY VOLTAGE

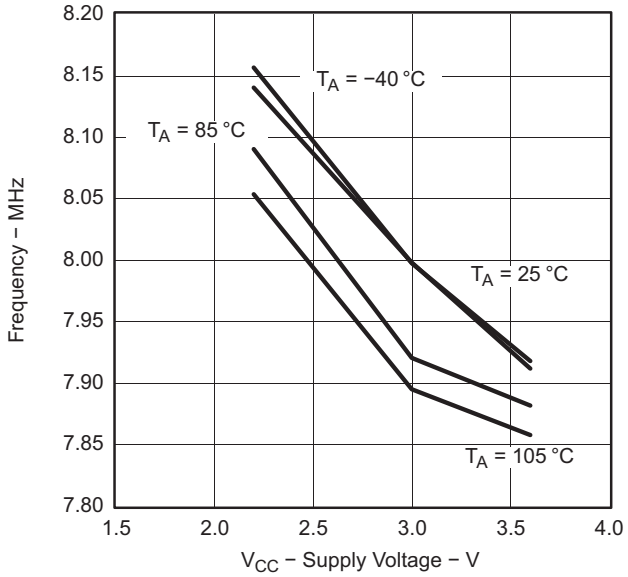


Figure 15.

CALIBRATED 12-MHz FREQUENCY vs SUPPLY VOLTAGE

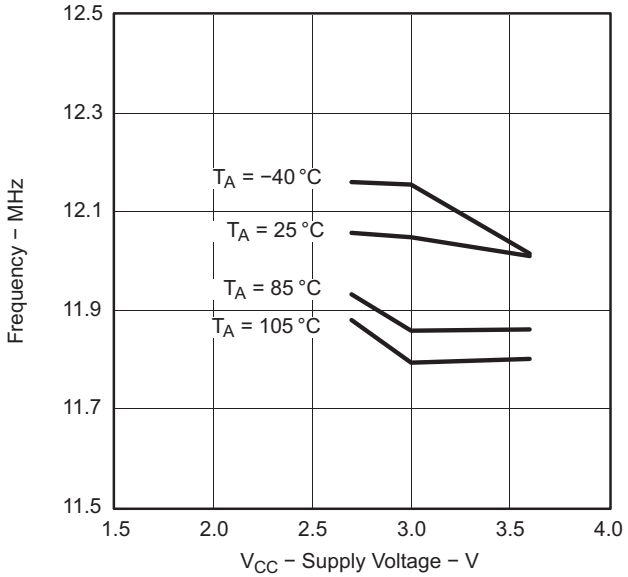


Figure 16.

CALIBRATED 16-MHz FREQUENCY vs SUPPLY VOLTAGE

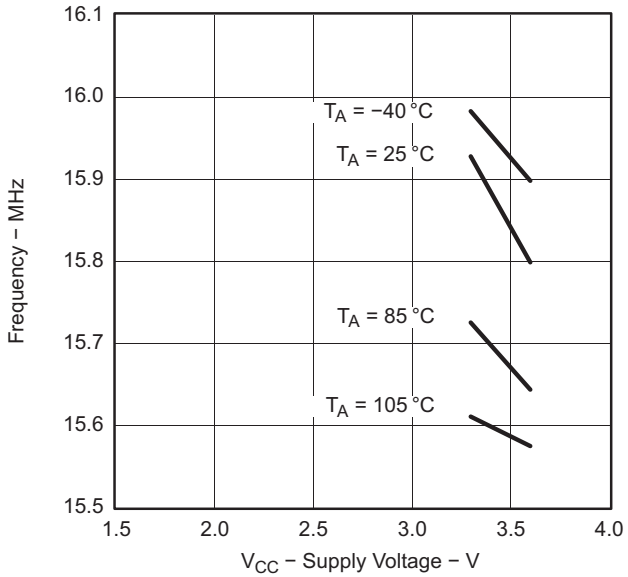


Figure 17.

Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	µs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ				1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ				1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (2)				$1 / f_{MCLK} + t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4

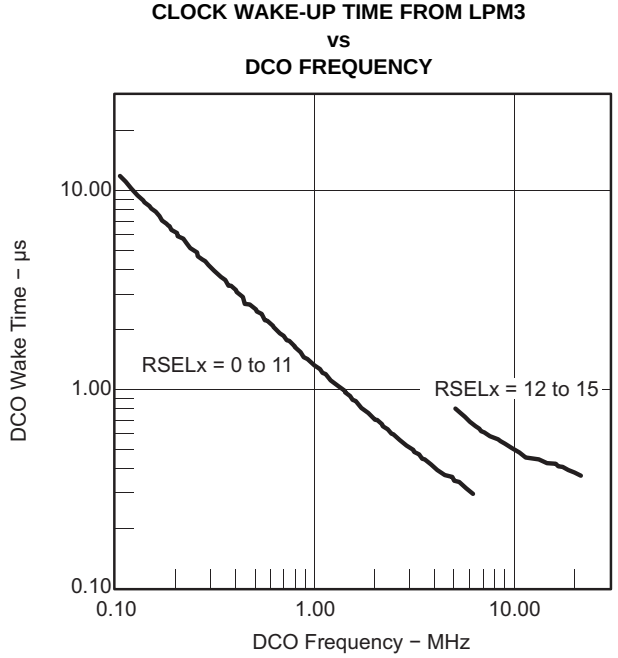


Figure 18.

DCO With External Resistor R_{OSC} (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V	1.8	MHz
			3 V	1.95	
D_T	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	±0.1	%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	10	%/V

(1) R_{OSC} = 100 kΩ. Metal film resistor, type 0257, 0.6 W with 1% tolerance and T_K = ±50 ppm/°C.

Typical Characteristics - DCO With External Resistor R_{OSC}

DCO FREQUENCY vs R_{OSC} V_{CC} = 2.2 V, T_A = 25°C

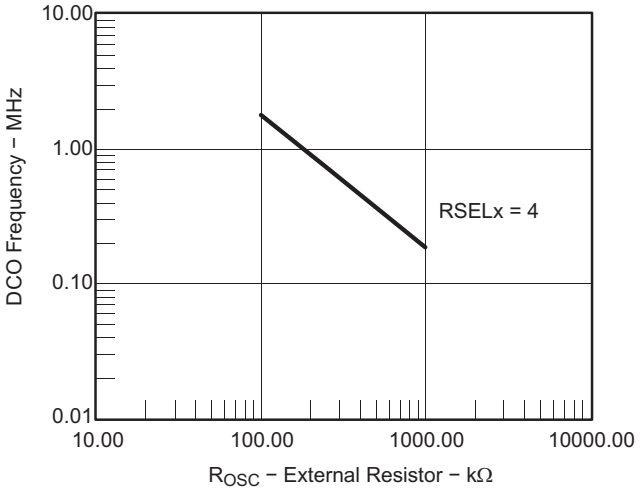


Figure 19.

DCO FREQUENCY vs R_{OSC} V_{CC} = 3 V, T_A = 25°C

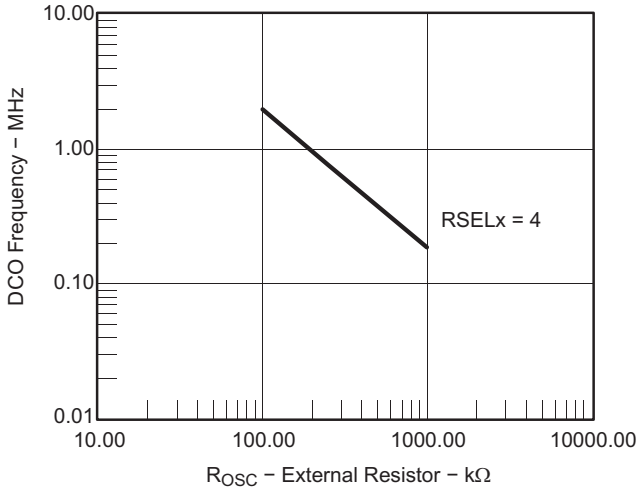


Figure 20.

DCO FREQUENCY vs TEMPERATURE V_{CC} = 3 V

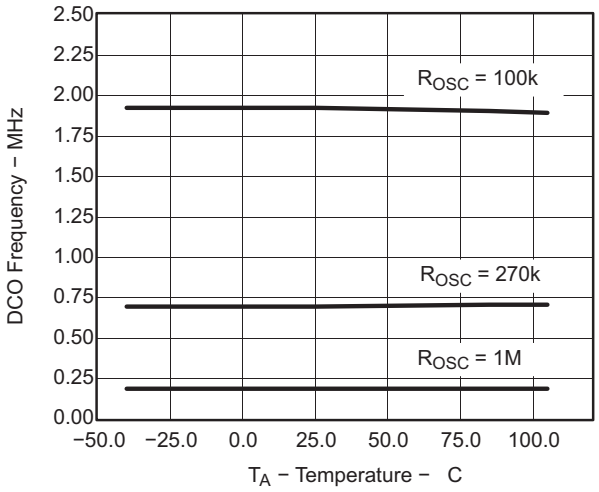


Figure 21.

DCO FREQUENCY vs SUPPLY VOLTAGE T_A = 25°C

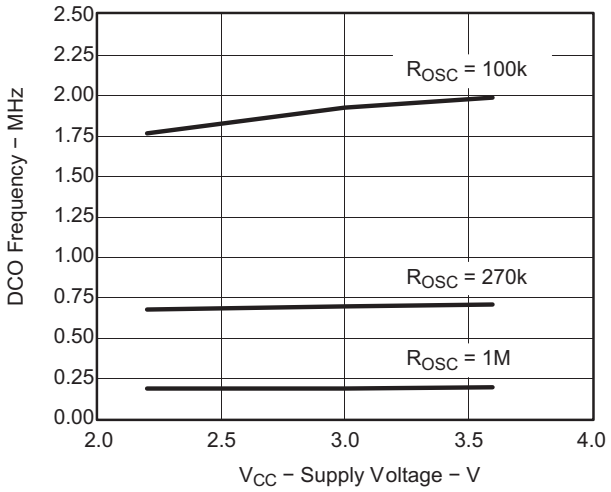


Figure 22.

Crystal Oscillator LFXT1, Low-Frequency Mode[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode[2]	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode[3]	XTS = 0, LFXT1Sx = 3, XCAPx = 0[4]	2.2 V/3 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	2.2 V/3 V	4	12	20	kHz
df_{VLO}/dT	VLO frequency temperature drift [1]	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift [2]	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method:
I version: (MAX(-40 to 85°C) - MIN(-40 to 85°C))/MIN(-40 to 85°C)/(85°C - (-40°C))
T version: (MAX(-40 to 105°C) - MIN(-40 to 105°C))/MIN(-40 to 105°C)/(105°C - (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V))/MIN(1.8 to 3.6 V)/(3.6 V - 1.8 V)

Crystal Oscillator LFXT1, High-Frequency Mode(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0, XCAPx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1, XCAPx = 0	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2, XCAPx = 0	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 23 and Figure 24)	XTS = 1, XCAPx = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, XCAPx = 0, LFXT1Sx = 1, $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, XCAPx = 0, LFXT1Sx = 2, $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(2)	XTS = 1, XCAPx = 0(3)			1		pF
	Duty cycle, HF mode	XTS = 1, XCAPx = 0, Measured at P1.4/SMCLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	50	60	%
		XTS = 1, XCAPx = 0, Measured at P1.4/SMCLK, $f_{LFXT1,HF}$ = 16 MHz		40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency (4)	XTS = 1, LFXT1Sx = 3, XCAPx = 0(5)	2.2 V/3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)

OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

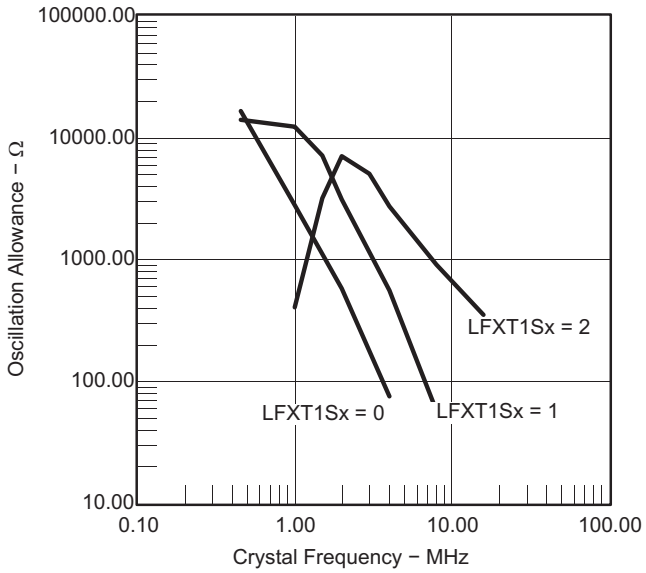


Figure 23.

OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

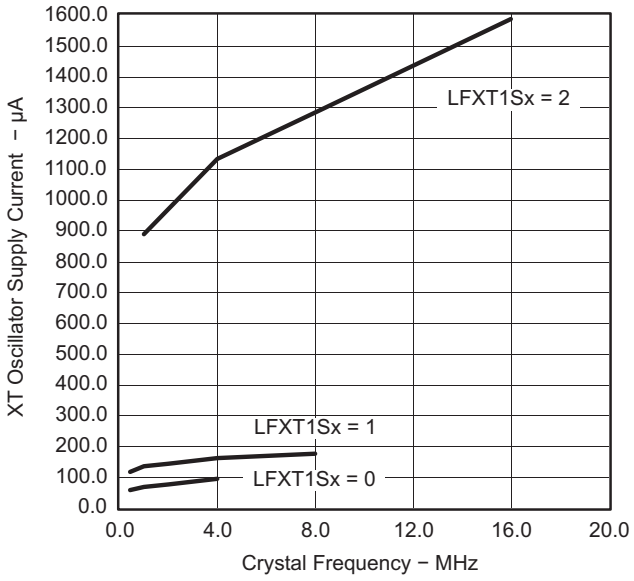


Figure 24.

Crystal Oscillator XT2[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{XT2}	XT2 oscillator crystal frequency, mode 0	XT2Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 1	XT2Sx = 1	1.8 V to 3.6 V	1		4	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 2	XT2Sx = 2	1.8 V to 2.2 V	2		10	MHz
			2.2 V to 3.0 V	2		12	
			3.0 V to 3.6 V	2		16	
f_{XT2}	XT2 oscillator logic-level square-wave input frequency	XT2Sx = 3	1.8 V to 2.2 V	0.4		10	MHz
			2.2 V to 3.0 V	0.4		12	
			3.0 V to 3.6 V	0.4		16	
OA	Oscillation allowance (see Figure 25 and Figure 26)	XT2Sx = 0, f_{XT2} = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XT2Sx = 1, f_{XT2} = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XT2Sx = 2, f_{XT2} = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode[2]	See [3]			1		pF
	Duty cycle	Measured at P1.4/SMCLK, f_{XT2} = 10 MHz	2.2 V/3 V	40	50	60	%
		Measured at P1.4/SMCLK, f_{XT2} = 16 MHz		40	50	60	
f_{Fault}	Oscillator fault frequency, HF mode[4]	XT2Sx = 3[5]	2.2 V/3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

Typical Characteristics - XT2 Oscillator

OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

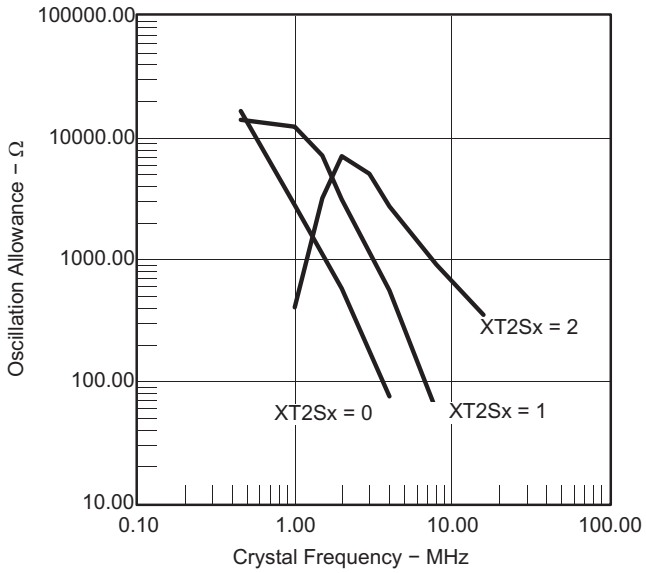


Figure 25.

OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

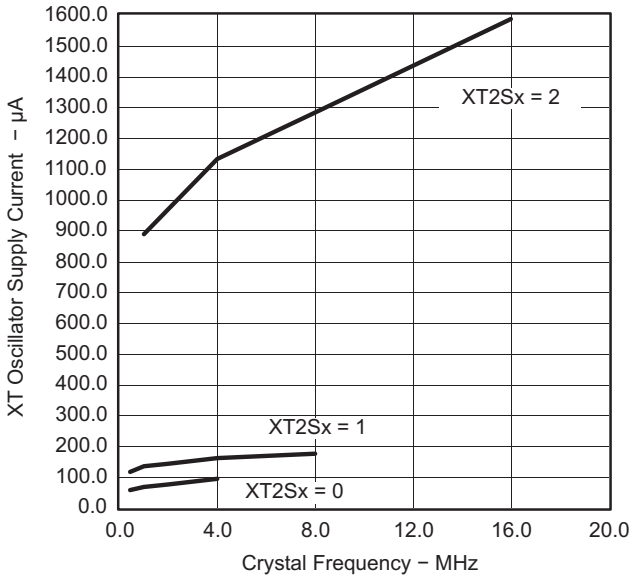


Figure 26.

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V/3 V	20			ns

Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TB,cap}$	Timer_B capture timing	TB0, TB1, TB2	2.2 V/3 V	20			ns

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)(1)		2.2 V/3 V			1	MHz
t_τ	UART receive deglitch time(2)		2.2 V	50	150		ns
			3 V	50	100		

(1) The DCO wake-up time must be considered in LPM3/4 for baudrates above 1 MHz.
(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

USCI (SPI Master Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 27 and Figure 28)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110			ns
			3 V	75			
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0			ns
			3 V	0			
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			30	ns
			3 V			20	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

USCI (SPI Slave Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 29 and Figure 30)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.

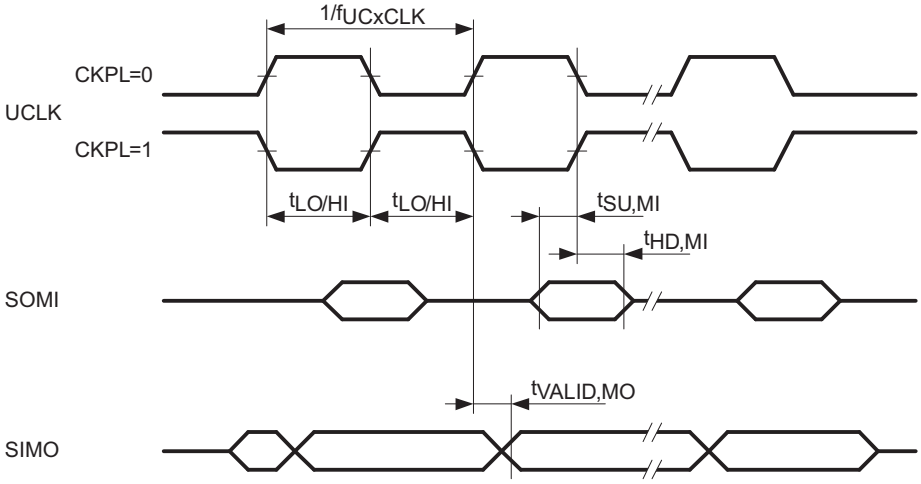


Figure 27. SPI Master Mode, CKPH = 0

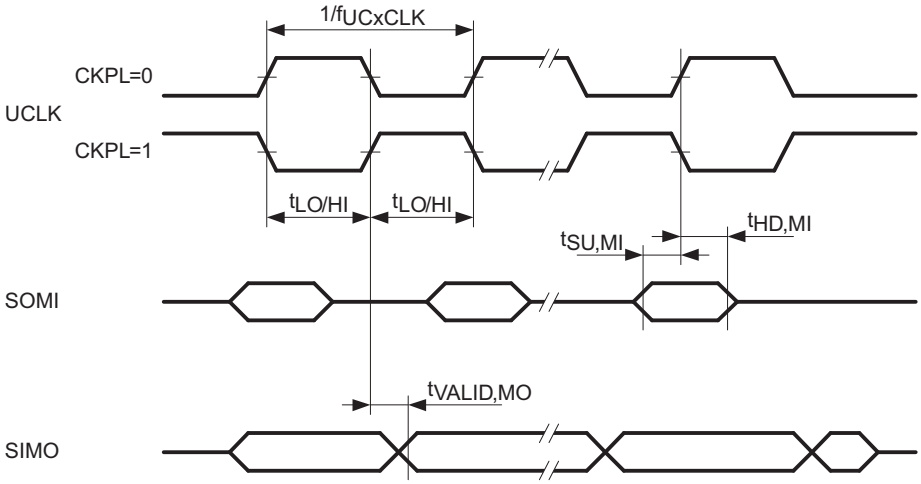


Figure 28. SPI Master Mode, CKPH = 1

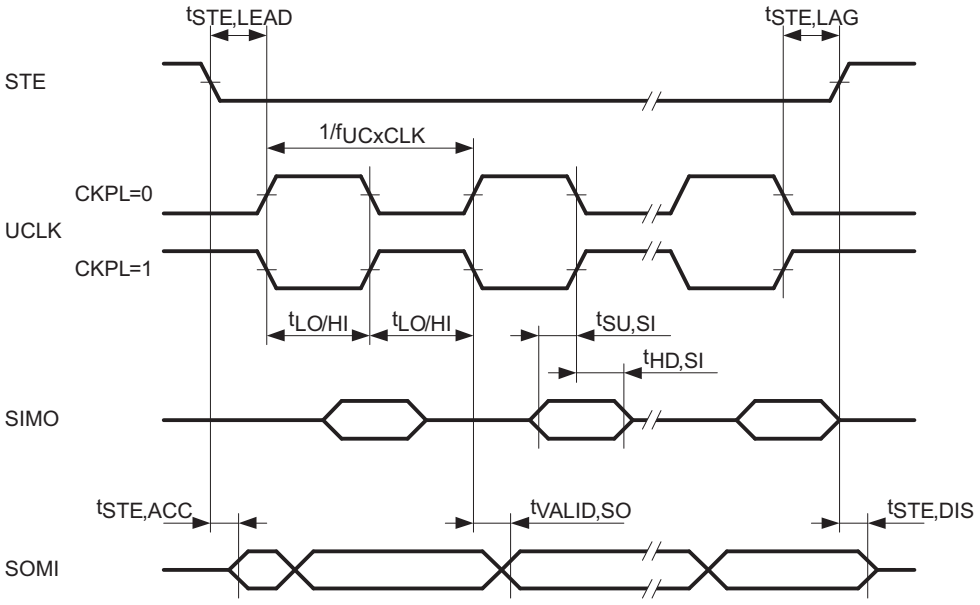


Figure 29. SPI Slave Mode, CKPH = 0

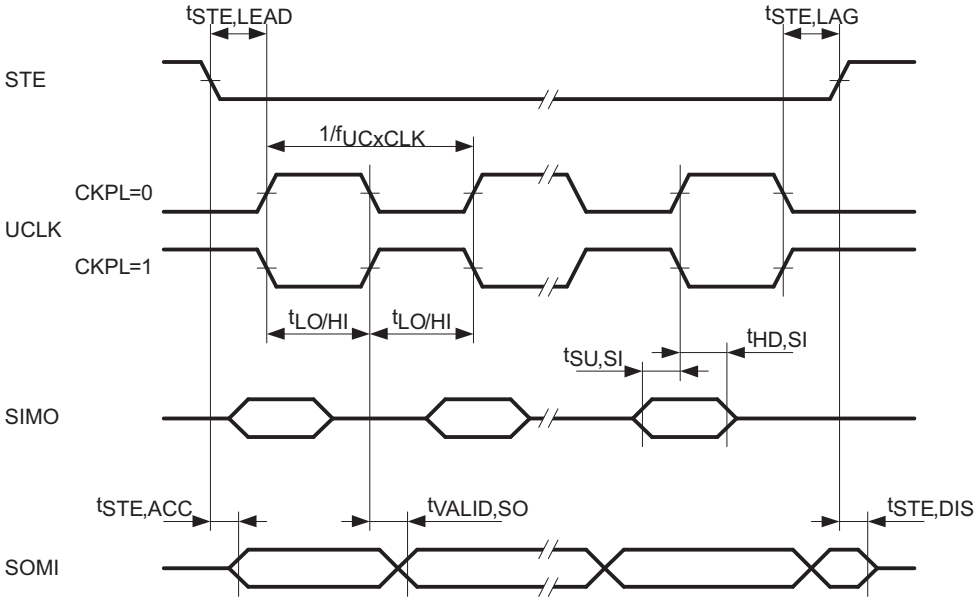


Figure 30. SPI Slave Mode, CKPH = 1

USCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 31)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V/3 V	4			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V/3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V/3 V	4			µs
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

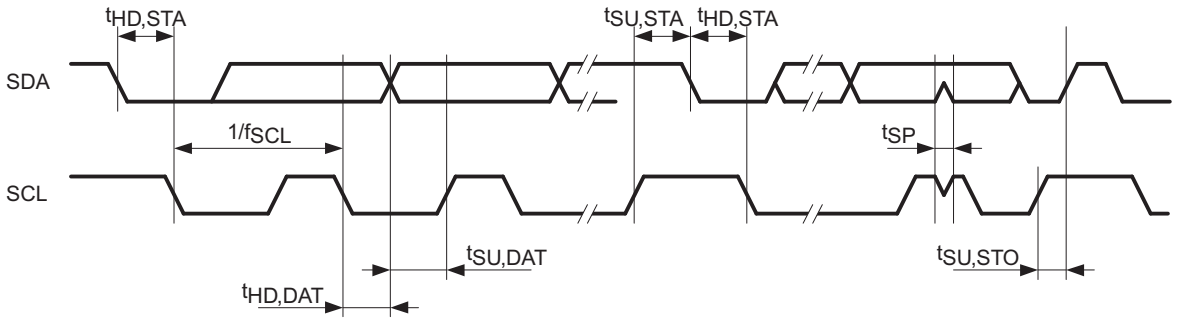


Figure 31. I^2C Mode Timing

Comparator_A+ (1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V/3 V	0		V_{CC} - 1	V
$V_{(Ref025)}$	Voltage at 0.25 V_{CC} node / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	Voltage at 0.5 V_{CC} node / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 36 and Figure 37	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage (2)		2.2 V/3 V	-30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response)}$	Response time (low-to-high and high-to-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0 (3) (see Figure 32 and Figure 33)	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 1 (3) (see Figure 32 and Figure 33)	2.2 V	1.4	1.9	2.8	µs
			3 V	0.9	1.5	2.2	

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
(3) The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step, with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

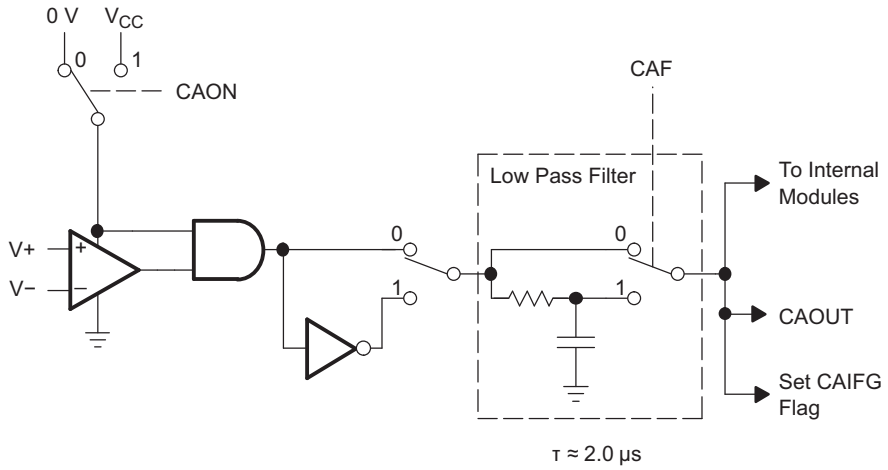


Figure 32. Comparator_A+ Block Diagram

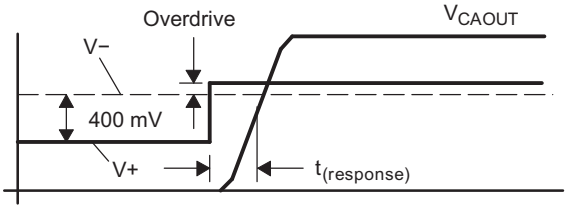


Figure 33. Comparator_A+ Overdrive Definition

Figure 34. Comparator_A+ Short Resistance Test Condition

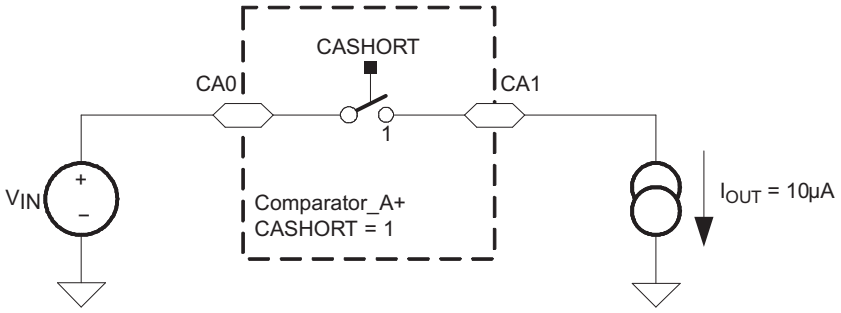


Figure 35. Comparator_A+ Short Resistance Test Condition

Typical Characteristics, Comparator_A+

$V_{(RefVT)}$ vs TEMPERATURE (V_{CC} = 3 V)

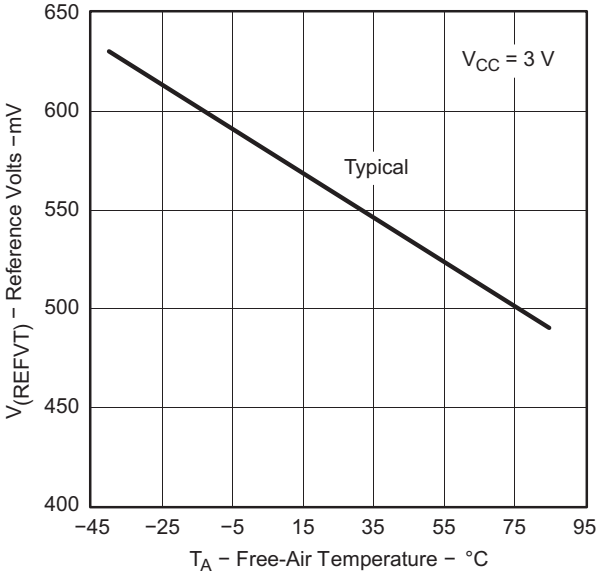


Figure 1. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

Figure 36.

$V_{(RefVT)}$ vs TEMPERATURE (V_{CC} = 2.2 V)

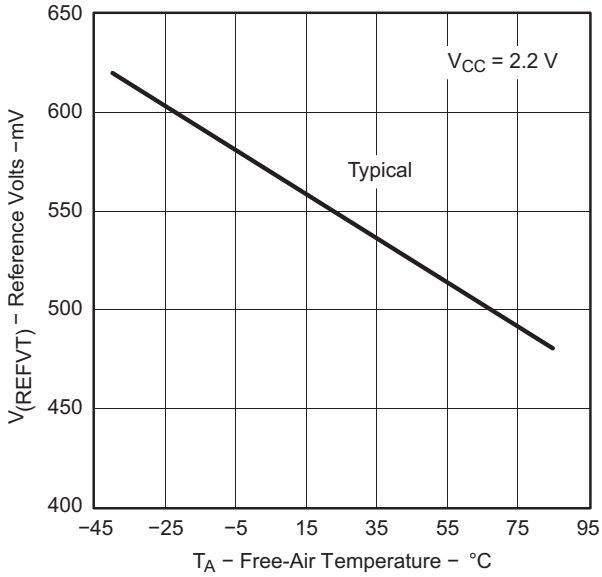


Figure 37.

SHORT RESISTANCE vs V_{IN}/V_{CC}

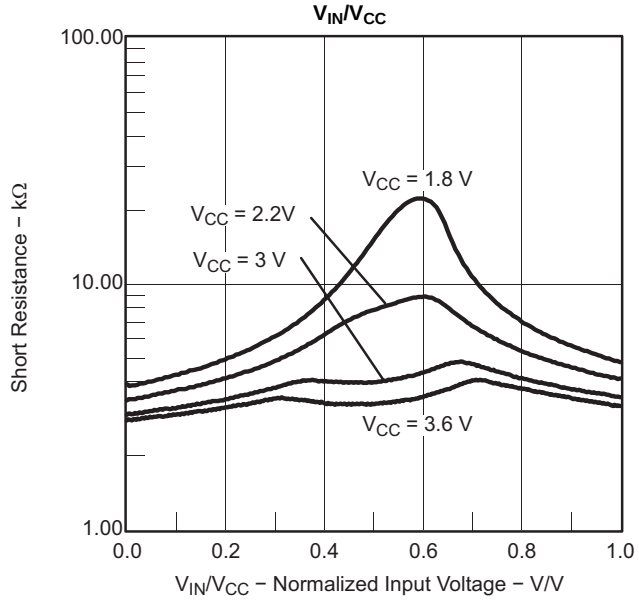


Figure 38.

12-bit ADC, Power Supply and Input Range Conditions(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range(2)	All P6.0/A0 to P6.7/A7 terminals, Analog inputs selected in ADC12MCTLx register, P6Sel.x = 1, 0 ≤ × ≤ 7, $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		0.65	0.8	mA
			3 V		0.8	1	
I_{REF+}	Operating supply current into AV_{CC} terminal(4)	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.7	mA
		$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.7	mA
			3 V		0.5	0.7	
C_I	Input capacitance(5)	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
R_I	Input MUX ON resistance(5)	0 V ≤ V_{Ax} ≤ V_{AVCC}	3 V			2000	Ω

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables settling of the built-in reference before starting an A/D conversion.
(5) Not production tested, limits verified by design.

12-Bit ADC, External Reference(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (2)		1.4	V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (3)		0	1.2	V
(V_{eREF+} – V_{REF-}/V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (4)		1.4	V_{AVCC}	V
I_{VeREF+}	Static leakage current	0 V ≤ V_{eREF+} ≤ V_{AVCC}	2.2 V/3 V		±1	µA
$I_{VREF-/VeREF-}$	Static leakage current	0 V ≤ V_{eREF-} ≤ V_{AVCC}	2.2 V/3 V		±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

12-Bit ADC, Built-In Reference

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	NOM	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	-40°C to 85°C	3 V	2.4	2.5	2.6	V
			105°C		2.37	2.5	2.64	
		REF2_5V = 0 for 1.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	-40°C to 85°C	2.2 V/3 V	1.44	1.5	1.56	
			105°C		1.42	1.5	1.57	
$AV_{CC(min)}$	AV_{CC} minimum voltage, positive built-in reference active	REF2_5V = 0, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min			2.2			V
		REF2_5V = 1, -0.5 mA ≤ I_{VREF+} ≤ I_{VREF+}min			2.8			
		REF2_5V = 1, -1 mA ≤ I_{VREF+} ≤ I_{VREF+}min			2.9			
I_{VREF+}	Load current out of V_{REF+} terminal			2.2 V	0.01		-0.5	mA
				3 V	0.01		-1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal (1)	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ≈ 0.75 V, REF2_5V = 0		2.2 V			±2	LSB
				3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ≈ 1.25 V, REF2_5V = 1		3 V			±2	LSB
$I_{DL(VREF)+}$	Load current regulation, V_{REF+} terminal (2)	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, ax ≈ 0.5 × V_{REF+}, Error of conversion result ≤ 1 LSB		3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (3)	REFON = 1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max		2.2 V/3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference (2)	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA		2.2 V/3 V			±100	ppm/°C
t_{REFON}	Settle time of internal reference voltage (see Figure 39) (4) (2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V		2.2 V			17	ms

(1) Not production tested, limits characterized.
(2) Not production tested, limits verified by design.
(3) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.
(4) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

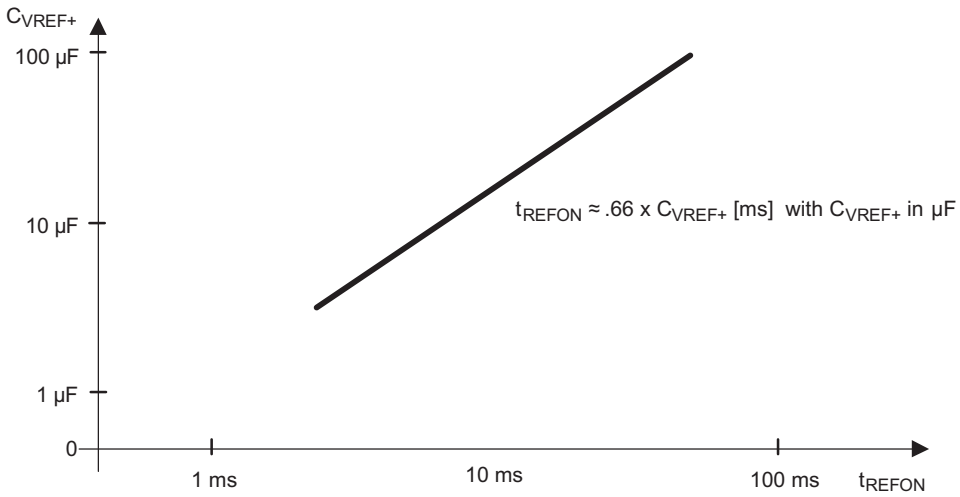


Figure 39. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

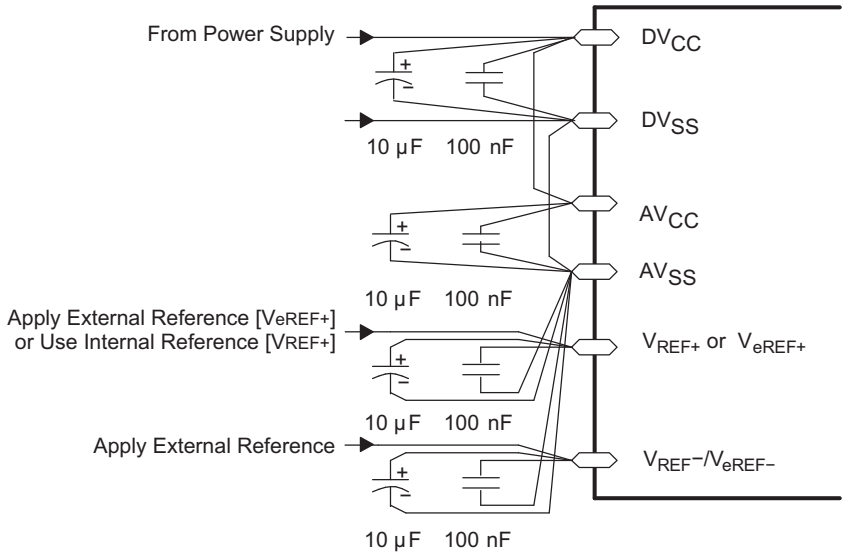


Figure 40. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

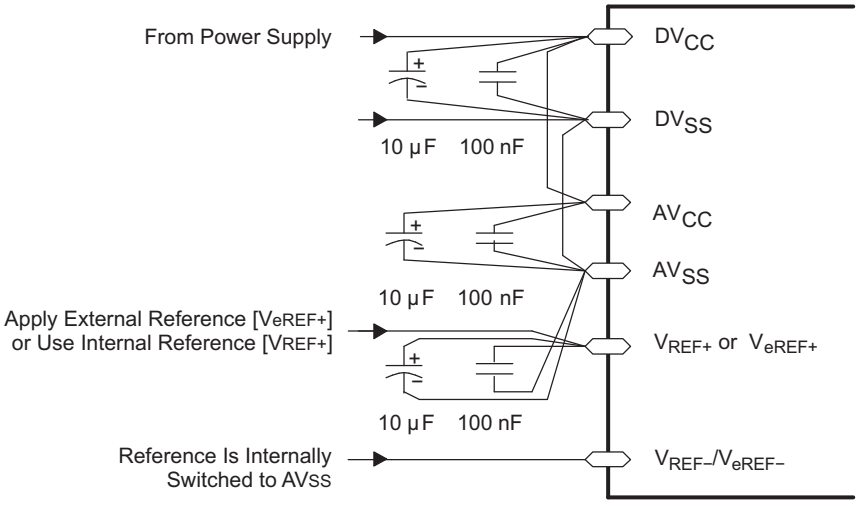


Figure 41. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} = AV_{SS}, Internally Connected

12-Bit ADC, Timing Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2 V/3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V/3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V/3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			13 × ADC12DIV × $1/f_{ADC12CLK}$		µs
$t_{ADC12ON}$	Turn-on settling time of the ADC (1)	See (2)				100	ns
t_{Sample}	Sampling time (1)	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (3)	3 V	1220			ns
			2.2 V	1400			

(1) Limits verified by design
(2) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

12-Bit ADC, Linearity Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < (V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ V_{AVCC}				±1.7	
E_D	Differential linearity error	(V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E_O	Offset error	(V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), Internal impedance of source RS < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (1)	REFON = 0, INCH = 0Ah, ADC12ON = 1, T_A = 25°C	2.2 V		40	120	µA
			3V		60	160	
V_{SENSOR} (2) (3)		ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986		mV
			3V		986		
TC_{SENSOR} (3)		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55 ± 3%	mV/°C
			3V		3.55	3.55 ± 3%	
$t_{SENSOR(sample)}$ (3)	Sample time required if channel 10 is selected (4)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3V	30			
I_{VMID}	Current into divider at channel 11 (5)	ADC12ON = 1, INCH = 0Bh	2.2 V			NA	µA
			3V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 × V_{AVCC}	2.2 V		1.1	1.1 ± 0.04	V
			3V		1.5	1.5 ± 0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (6)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
(2) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(3) Limits characterized
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
(5) No additional current is needed. The V_{MID} is used during sampling.
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$, no additional on time is needed.

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC\ (PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time(1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block,\ 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block,\ 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block,\ End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the flash controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See (1)	2.2 V	0		5	MHz
			3 V	0		10	
$R_{Internal}$	Internal pulldown resistance on TEST	See (2)	2.2 V/3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
(2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

JTAG Fuse(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

Port P1 Pin Schematic: P1.0 to P1.7, Input/Output With Schmitt Trigger

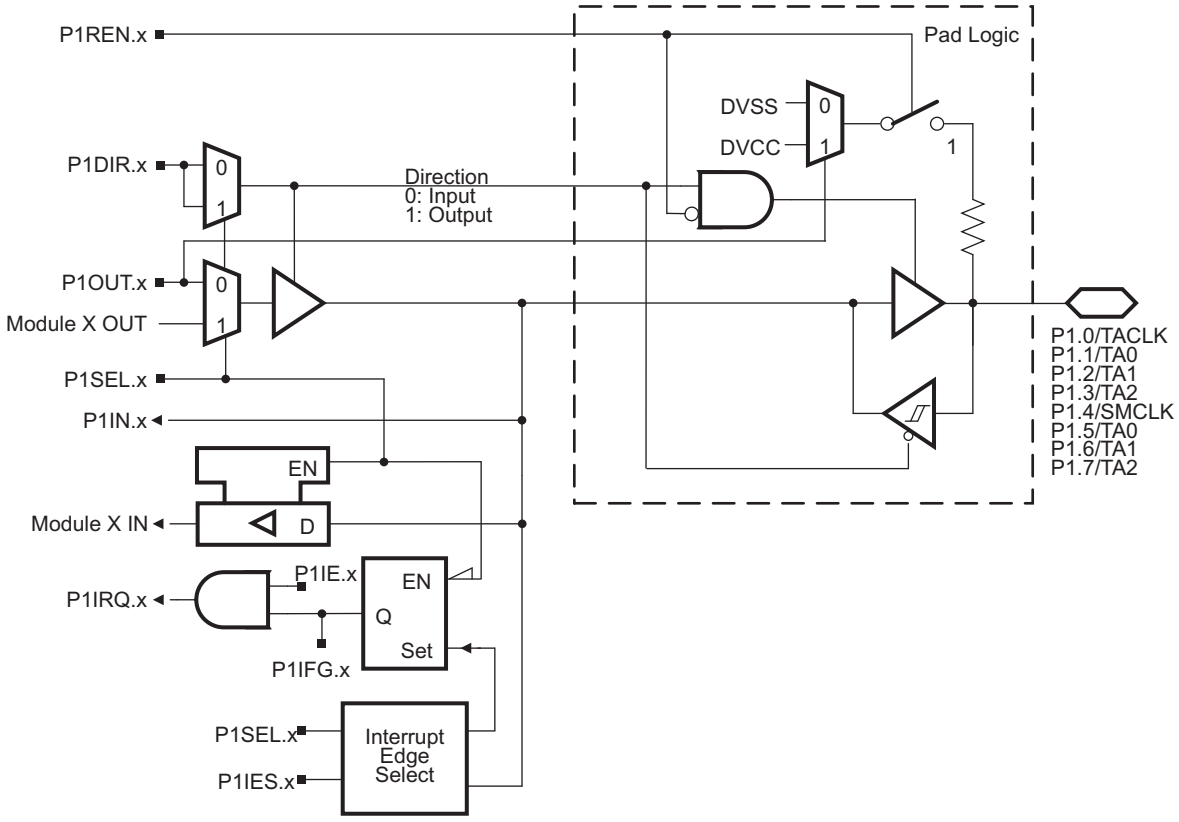


Table 20. Port P1.0 to P1.7 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		CAOUT	1	1
P1.1/TA0	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P1.4/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.5/TA0	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.6/TA1	6	P1.6 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.7/TA2	7	P1.7 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1

Port P2 Pin Schematic: P2.0 to P2.4, P2.6, and P2.7, Input/Output With Schmitt Trigger

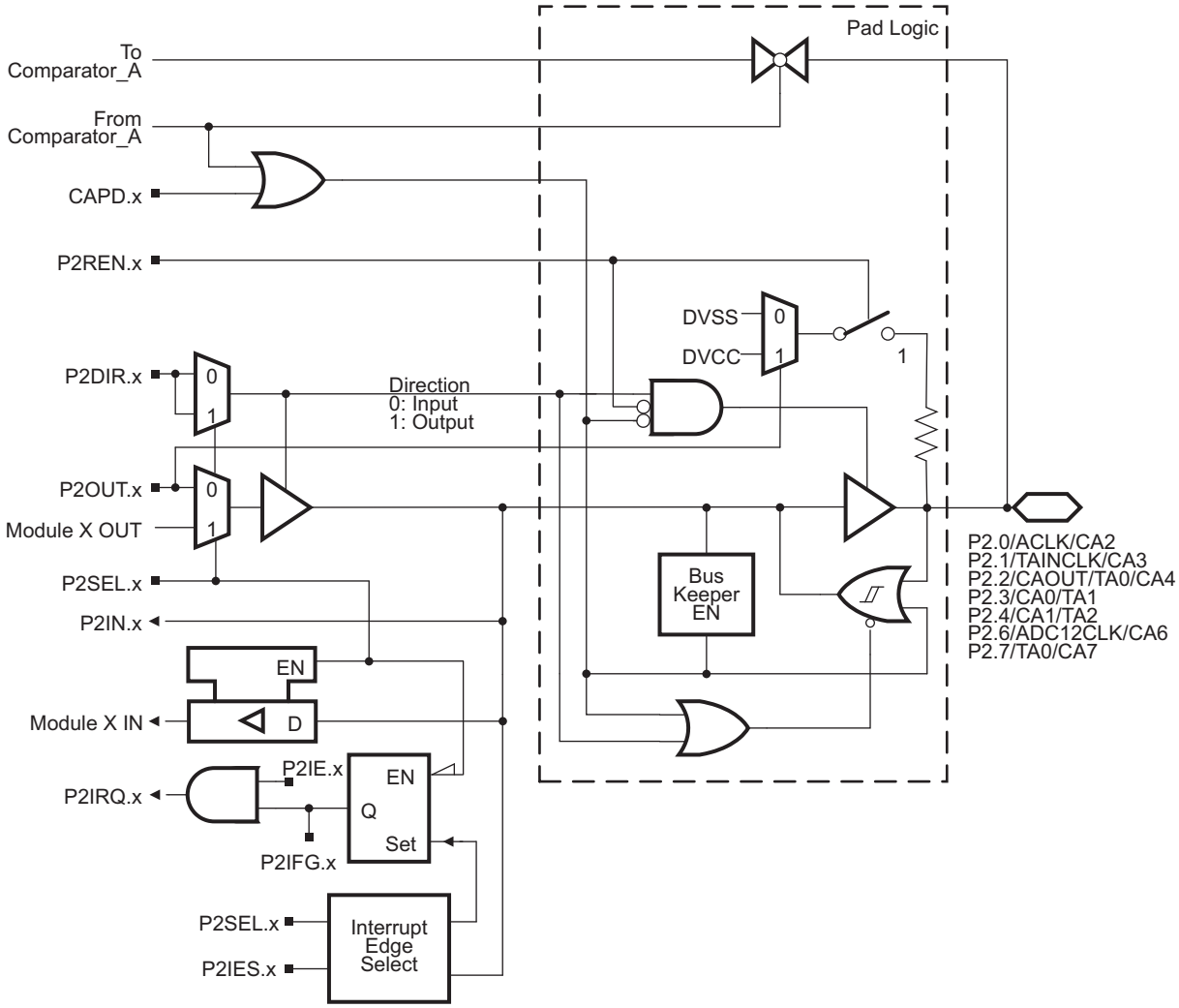


Table 21. Port P2.0 to P2.4, P2.6, and P2.7 Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)		
			CAPD.x	P2DIR.x	P2SEL.x
P2.0/ACLK/CA2	0	P2.0 (I/O)	0	I: 0; O: 1	0
		ACLK	0	1	1
		CA2	1	X	X
P2.1/TAINCLK/CA3	1	P2.1 (I/O)	0	I: 0; O: 1	0
		Timer_A3.INCLK	0	0	1
		DV_{SS}	0	1	1
		CA3	1	X	X
P2.2/CAOUT/TA0/CA4	2	P2.2 (I/O)	0	I: 0; O: 1	0
		CAOUT	0	1	1
		TA0	0	0	1
		CA4	1	X	X
P2.3/CA0/TA1	3	P2.3 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA1	0	1	1
		CA0	1	X	X
P2.4/CA1/TA2	4	P2.4 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA2	0	1	X
		CA1	1	X	1
P2.6/ADC12CLK(2)/CA6	6	P2.6 (I/O)	0	I: 0; O: 1	0
		ADC12CLK(2)	0	1	1
		CA6	1	X	X
P2.7/TA0/CA7	7	P2.7 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA0	0	1	1
		CA7	1	X	X

(1) X = Don't care
(2) MSP430F24x and MSP430F23x devices only

Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger

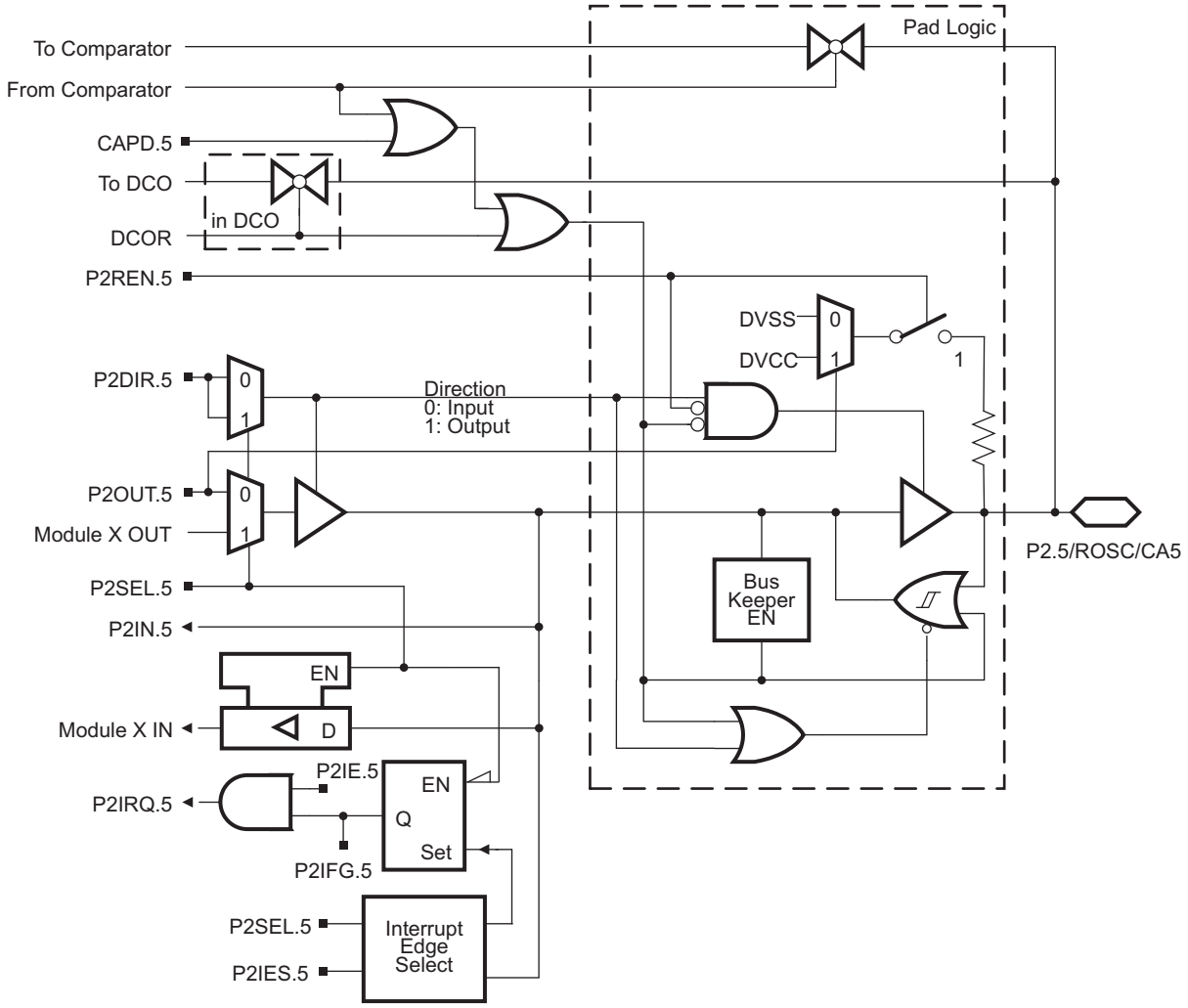


Table 22. Port P2.5 Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD	DCOR	P2DIR.5	P2SEL.5
P2.5/R_{OSC}/CA5	5	P2.5 (I/O)	0	0	I: 0; O: 1	0
		R_{OSC}	0	1	X	X
		DV_{SS}	0	0	1	1
		CA5	1 or selected	0	X	X

(1) X = Don't care

Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger

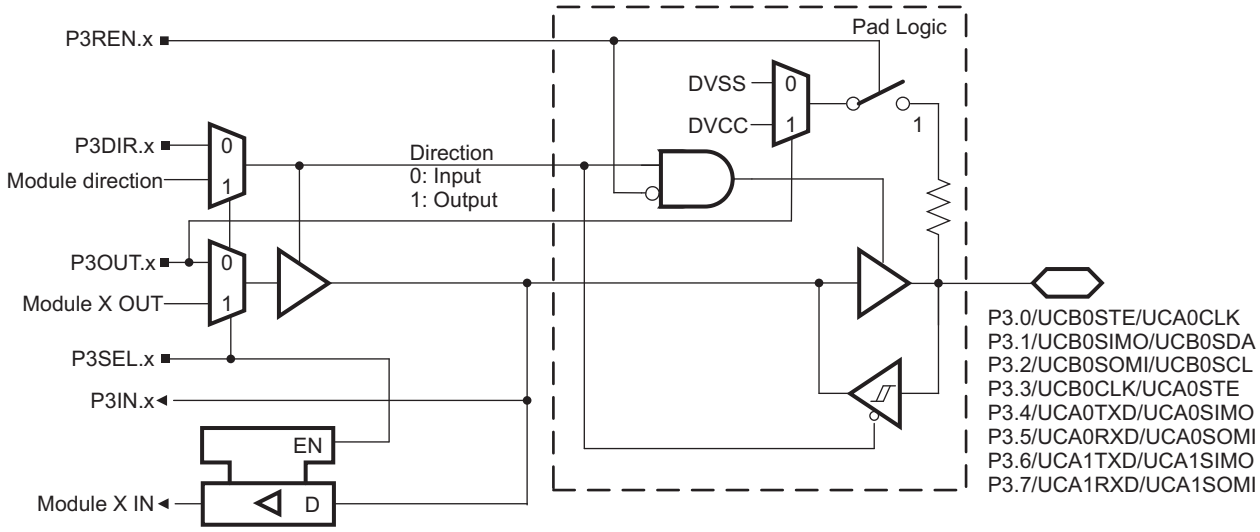


Table 23. Port P3.0 to P3.7 Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK[2][3]	X	1
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA[2][4]	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL[2][4]	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE[2]	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO[2]	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI[2]	X	1
P3.6/UCA1TXD[5]/UCA1SIMO[5]	6	P3.6 (I/O)	I: 0; O: 1	0
		UCA1TXD[5]/UCA1SIMO[5][2]	X	1
P3.7/UCA1RXD[5]/UCA1SOMI[5]	7	P3.7 (I/O)	I: 0; O: 1	0
		UCA1RXD[5]/UCA1SOMI[5][2]	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI A/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) MSP430F24x and MSP430F24x1 devices only

Port P4 Pin Schematic: P4.0 to P4.7, Input/Output With Schmitt Trigger

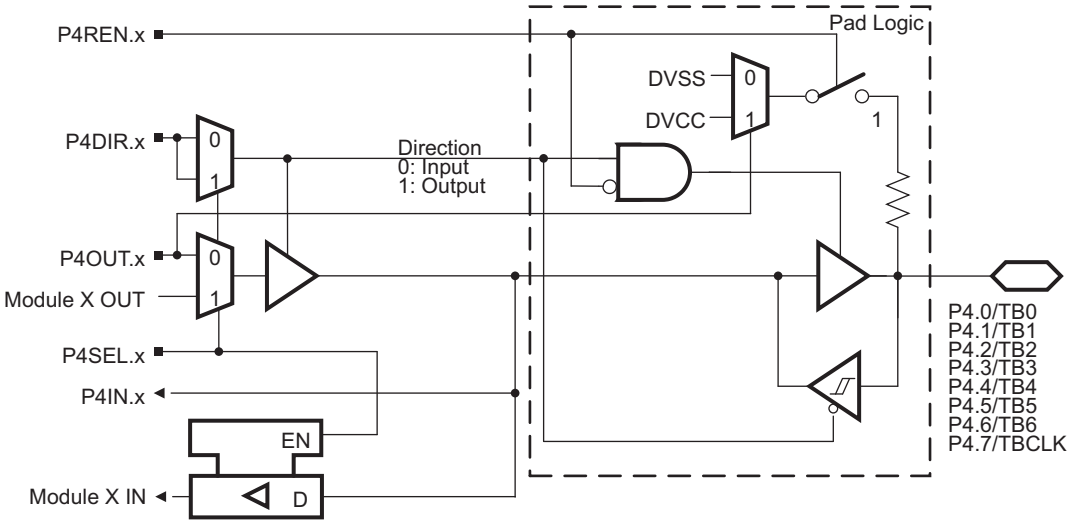


Table 24. Port P4.0 to P4.7 Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0	1	1
P4.1/TB1	1	P4.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1	1	1
P4.2/TB2	2	P4.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB2	1	1
P4.3/TB3(1)	3	P4.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B(1)	0	1
		Timer_B7.TB3(1)	1	1
P4.4/TB4(1)	4	P4.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B(1)	0	1
		Timer_B7.TB4(1)	1	1
P4.5/TB5(1)	5	P4.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B(1)	0	1
		Timer_B7.TB5(1)	1	1
P4.6/TB6(1)	6	P4.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B(1)	0	1
		Timer_B7.TB6(1)	1	1
P4.7/TBCLK	7	P4.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	0	1

(1) MSP430F24x and MSP430F24x1 devices only

Port P5 Pin Schematic: P5.0 to P5.3, Input/Output With Schmitt Trigger

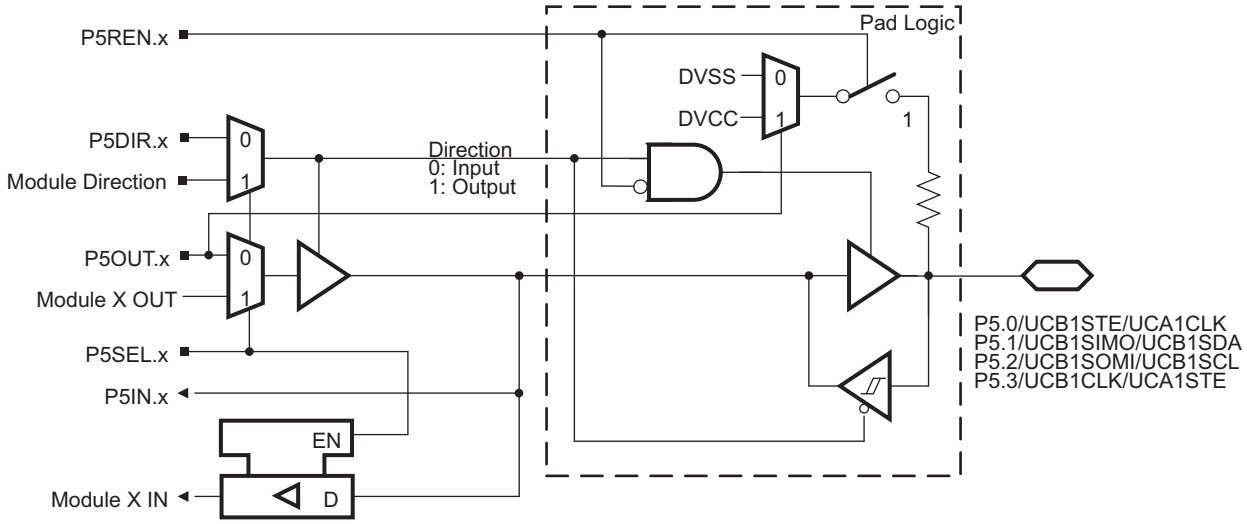


Table 25. Port P5.0 to P5.3 Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.0/UCB1STE(2)/UCA1CLK(2)	0	P5.0 (I/O)	I: 0; O: 1	0
		UCB1STE(2)/UCA1CLK(2)(3)(4)	X	1
P5.1/UCB1SIMO(2)/UCB1SDA(2)	1	P5.1 (I/O)	I: 0; O: 1	0
		UCB1SIMO(2)/UCB1SDA(2)(3)(5)	X	1
P5.2/UCB1SOMI(2)/UCB1SCL(2)	2	P5.2 (I/O)	I: 0; O: 1	0
		UCB1SOMI(2)/UCB1SCL(2)(3)(5)	X	1
P5.3/UCB1CLK(2)/UCA1STE(2)	3	P5.3 (I/O)	I: 0; O: 1	0
		UCB1CLK(2)/UCA1STE(2)(3)	X	1

(1) X = Don't care
(2) MSP430F24x and MSP430F24x1 devices only
(3) The pin direction is controlled by the USCI module.
(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI A/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) If I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P5 Pin Schematic: P5.4 to P5.7, Input/Output With Schmitt Trigger

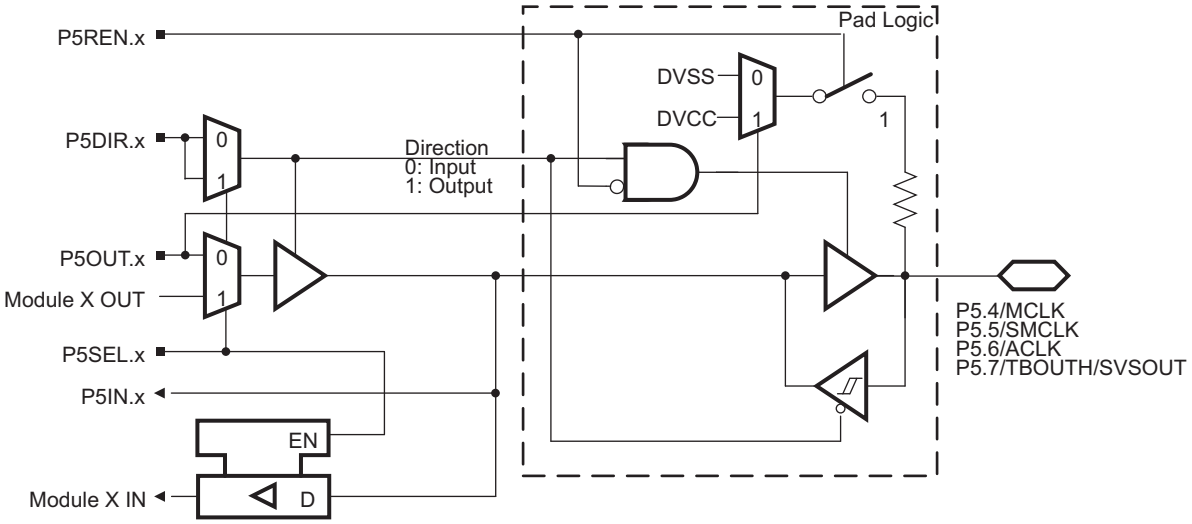


Table 26. Port P5.4 to P5.7 Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.4/MCLK	4	P5.4 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P5.5/SMCLK	5	P5.5 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P5.6/ACLK	6	P5.6 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P5.7/TBOUTH/SVSOUT	7	P5.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBOUTH	0	1
		SVSOUT	1	1

Port P6 Pin Schematic: P6.0 to P6.6, Input/Output With Schmitt Trigger

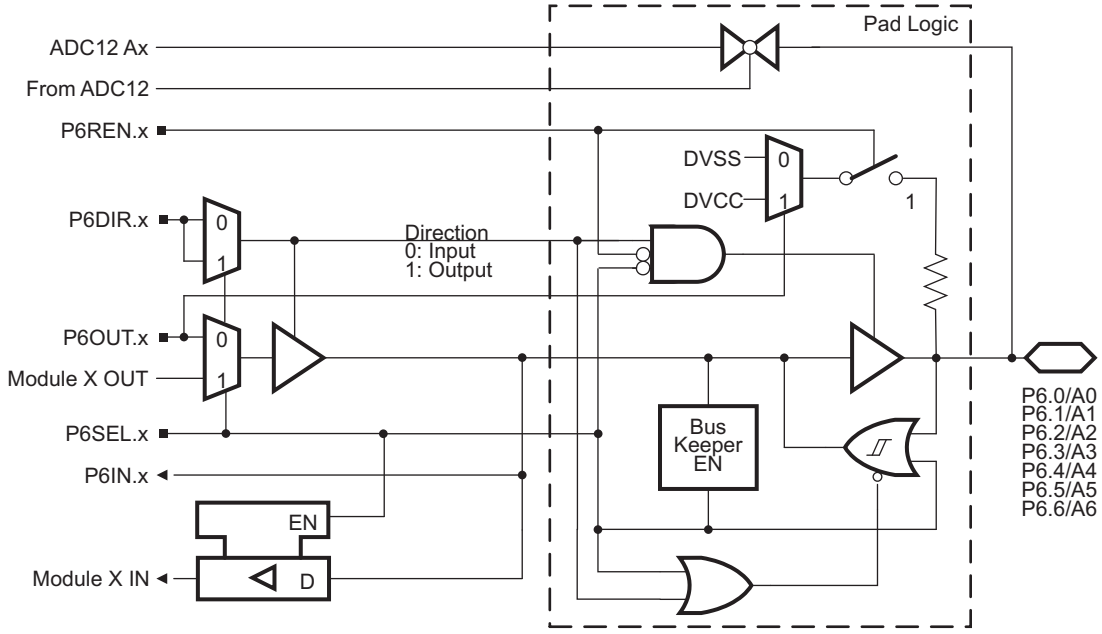


Table 27. Port P6.0 to P6.6 Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P6DIR.x	P6SEL.x
P6.0/A0(2)	0	P5.0 (I/O)	I: 0; O: 1	0
		A0(2)	X	1
P6.1/A1(2)	1	P5.1 (I/O)	I: 0; O: 1	0
		A1(2)	X	1
P6.2/A2(2)	2	P5.2 (I/O)	I: 0; O: 1	0
		A2(2)	X	1
P6.3/A3(2)	3	P5.3 (I/O)	I: 0; O: 1	0
		A3(2)	X	1
P6.4/A4(2)	4	P5.4 (I/O)	I: 0; O: 1	0
		A4(2)	X	1
P6.5/A5(2)	5	P5.5 (I/O)	I: 0; O: 1	0
		A5(2)	X	1
P6.6/A6(2)	6	P6.6 (I/O)	I: 0; O: 1	0
		A6(2)	X	1

(1) X = Don't care
(2) MSP430F24x and MSP430F23x devices only

Port P6 Pin Schematic: P6.7, Input/Output With Schmitt Trigger

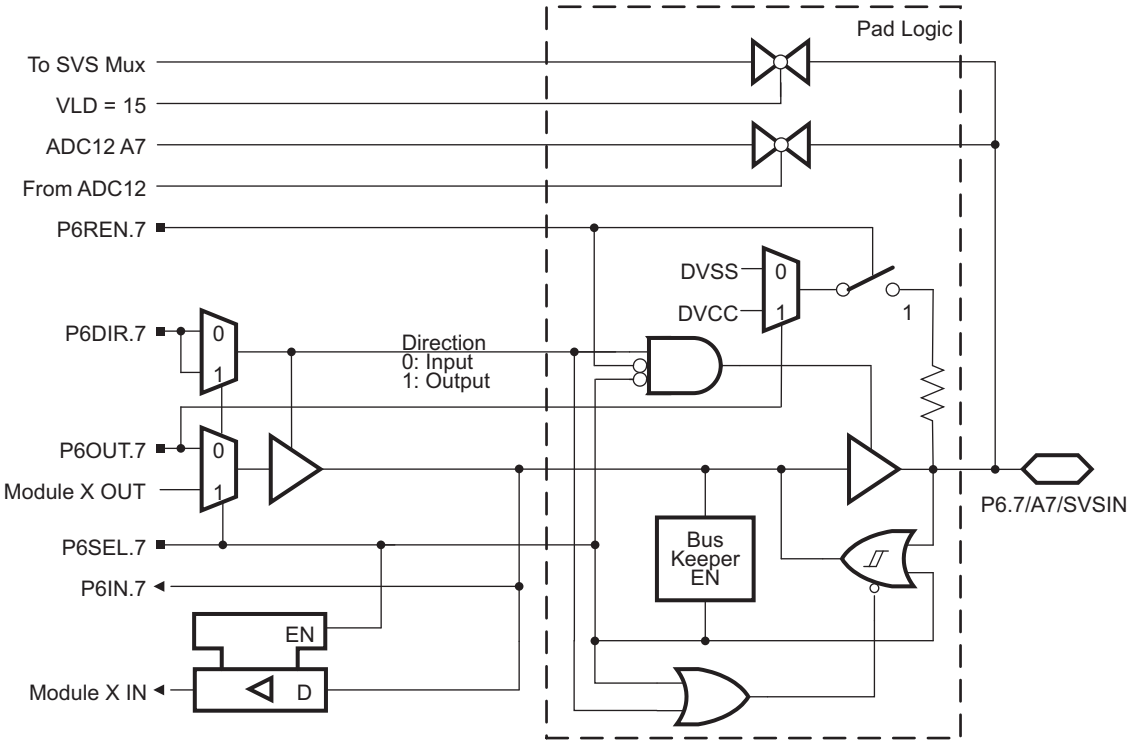
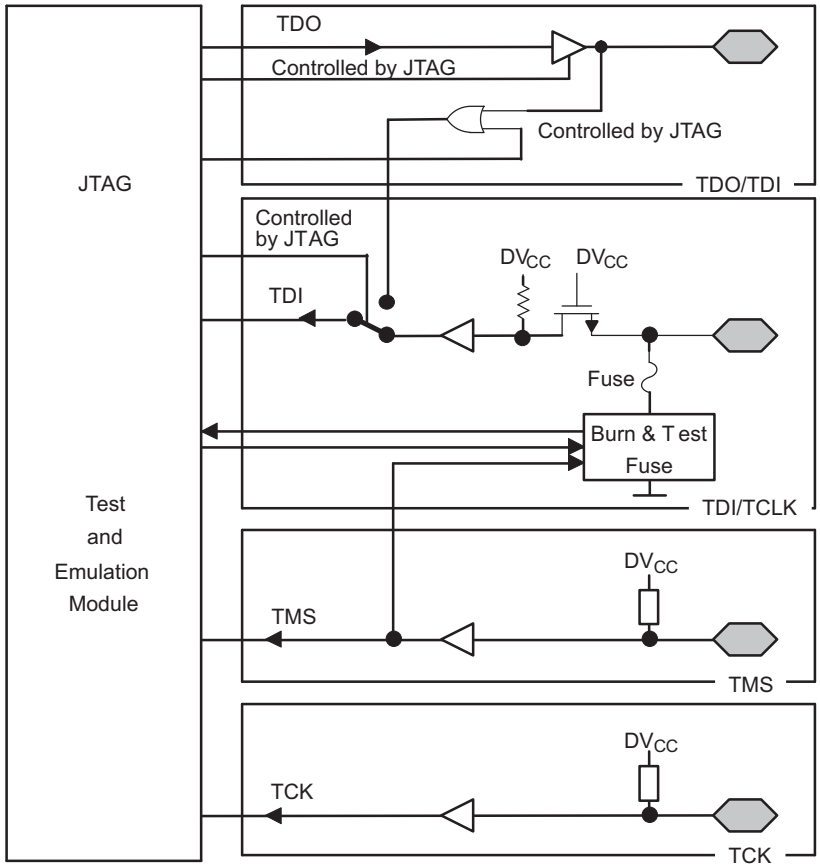


Table 28. Port P6.7 Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P6DIR.x	P6SEL.x	INCHy
P6.7/A7/SVSIN	7	P6.7 (I/O)	I: 0; O: 1	0	0
		DV_{SS}	1	1	0
		A7[2]	X	X	1 (y = 7)
		SVSIN (VLD = 15)	X	X	1

(1) X = Don't care
(2) MSP430F24x and MSP430F23x devices only

JTAG Pins (TMS, TCK, TDI/TCLK, TDO/TDI), Input/Output With Schmitt Trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 42). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

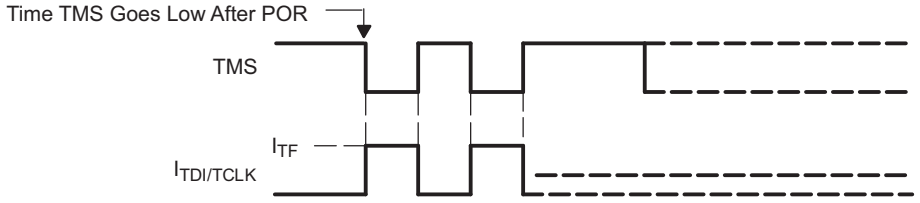


Figure 42. Fuse Check Mode Current

NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the Bootstrap Loader section for more information.

REVISION HISTORY

LITERATURE NUMBER	SUMMARY
SLAS547	Product Preview release
SLAS547A	Production Data release
SLAS547B	Corrected terminal names and descriptions for pins 34 and 35 in "Terminal Functions - MSP430F23x" (page 9) Corrected terminal names for pins 13, 14, and 15 in "Terminal Functions - MSP430F24x1" (page 13) Corrected interrupt source and flag entries for USCI_A1/USCI_B1 in "interrupt vector addresses" table (page 17) Changed index values from 1-3 to 0-2 in Figures 23 to 26 (pages 52 and 54) Changed $f_{max,BITCLK}$ and t_τ parameters in "USCI (UART mode)" table (page 56) Corrected "Port P1.0 to P1.7 pin functions" table (page 72) Removed incorrect CAPD.x column in "Port P6.0 to P6.6 pin functions" table (page 80)
SLAS547C	Added Development Tool Support section (page 2) Updated parametric values in "low-power mode supply current into V_{CC} excluding external current" table (page 34)
SLAS547D	Updated notes and $t_{CMErase}$ MIN value "flash memory" table (page 34)
SLAS547E	Changed limits on $t_{d(SVSon)}$ parameter (page 41)
SLAS547F	Changed "Port 6.0 to 6.6 Pin Functions" table (page 77) Changed "Port 6.7 Pin Functions" table (page 78)
SLAS547G	Changed T_{stg}, Programmed device, to -55°C to 150°C in Absolute Maximum Ratings
SLAS547H	Corrected formatting error of T_A column in Active Mode Supply Current (both $I_{AM,1MHz}$ parameters) and in Low-Power-Mode Supply Currents ($I_{LPM0,1MHz}$ and $I_{LPM0,100kHz}$ parameters)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F233TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F233TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F233TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F233TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F233TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F235TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F235TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F235TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F235TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F235TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2410TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2410TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2410TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F2410TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2410TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2471TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2471TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2471TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F2471TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2471TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F247TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F247TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F247TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F247TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F247TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2481TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2481TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2481TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F2481TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2481TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F248TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F248TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F248TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F248TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F248TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2491TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2491TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F2491TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F2491TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F2491TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F249TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F249TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F249TRGC	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	
MSP430F249TRGCR	ACTIVE	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F249TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F249 :

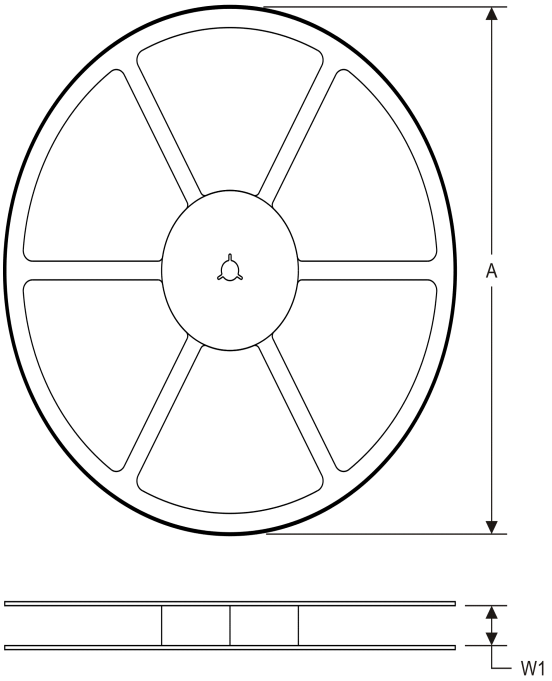
- Enhanced Product: MSP430F249-EP

NOTE: Qualified Version Definitions:

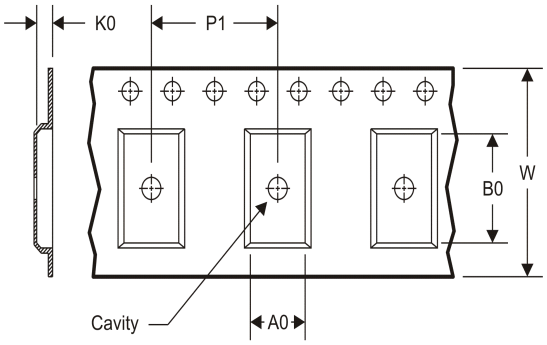
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



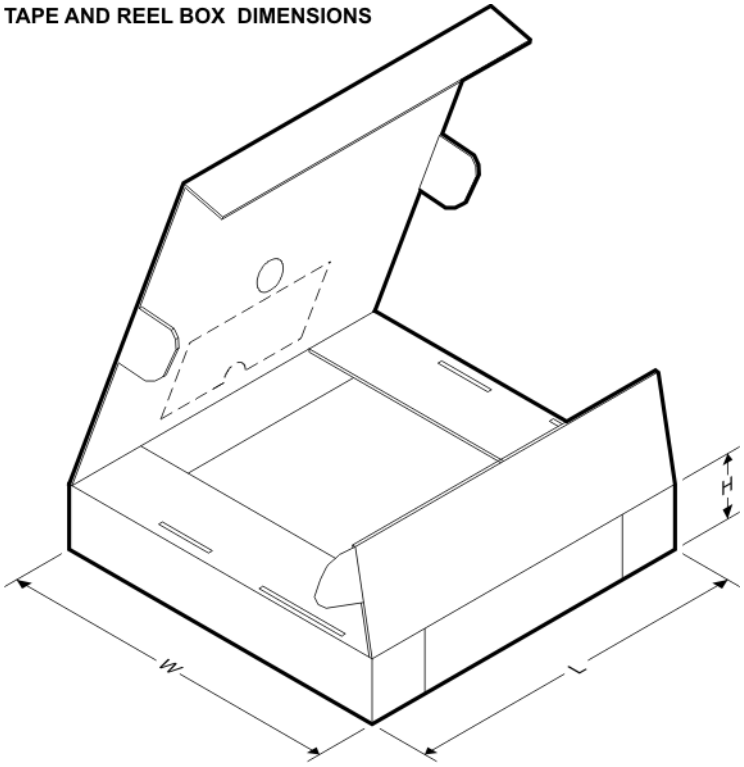
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F233TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F233TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F235TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F235TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F2410TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F2410TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2471TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2471TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F247TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F247TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2481TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2481TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F248TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F248TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2491TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F2491TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F249TPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F249TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

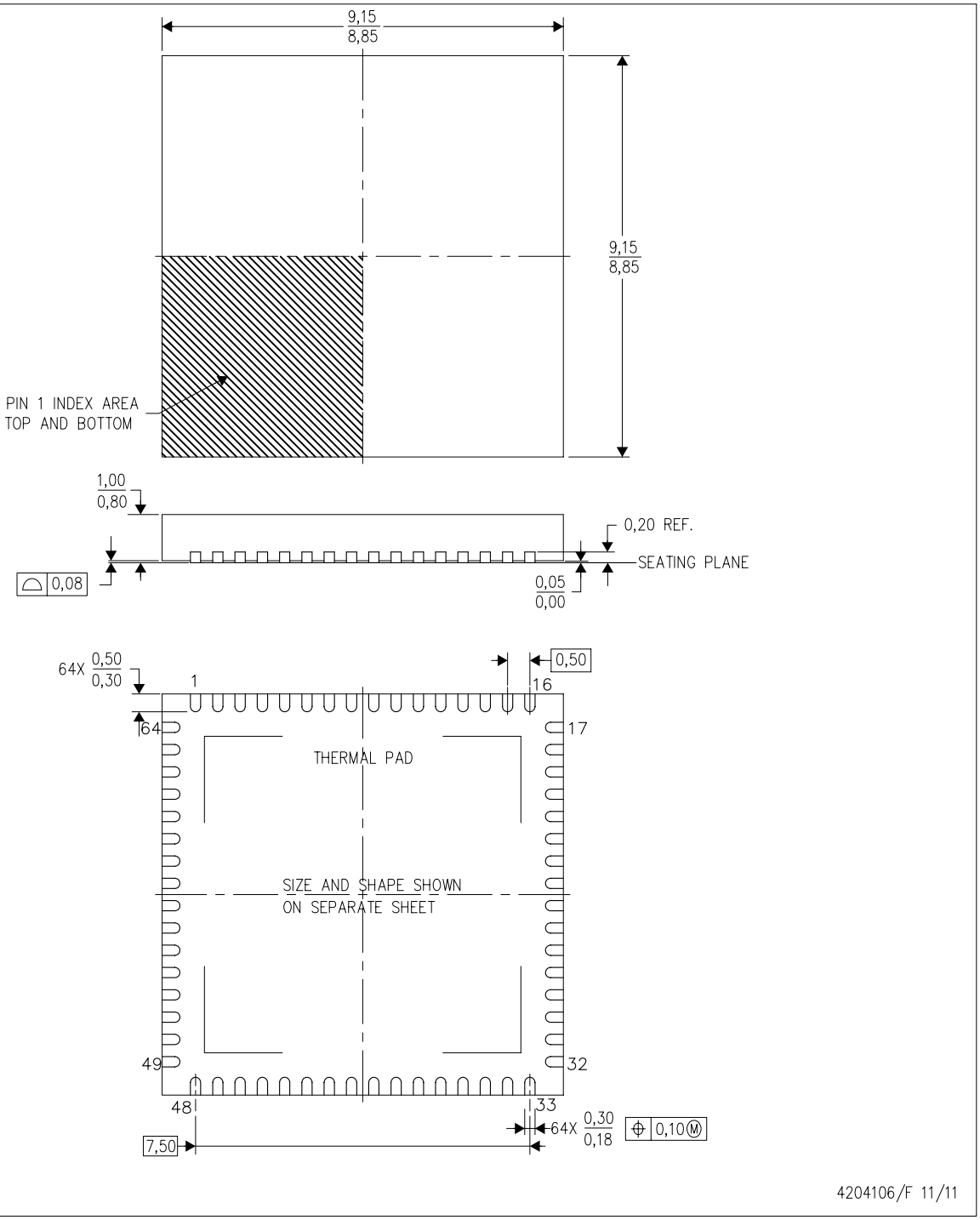
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F233TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F233TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F235TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F235TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2410TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2410TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F2471TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F2471TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F247TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F247TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F2481TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F2481TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F248TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F248TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F2491TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2491TPMR	LQFP	PM	64	1000	346.0	346.0	41.0
MSP430F249TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F249TPMR	LQFP	PM	64	1000	346.0	346.0	41.0

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

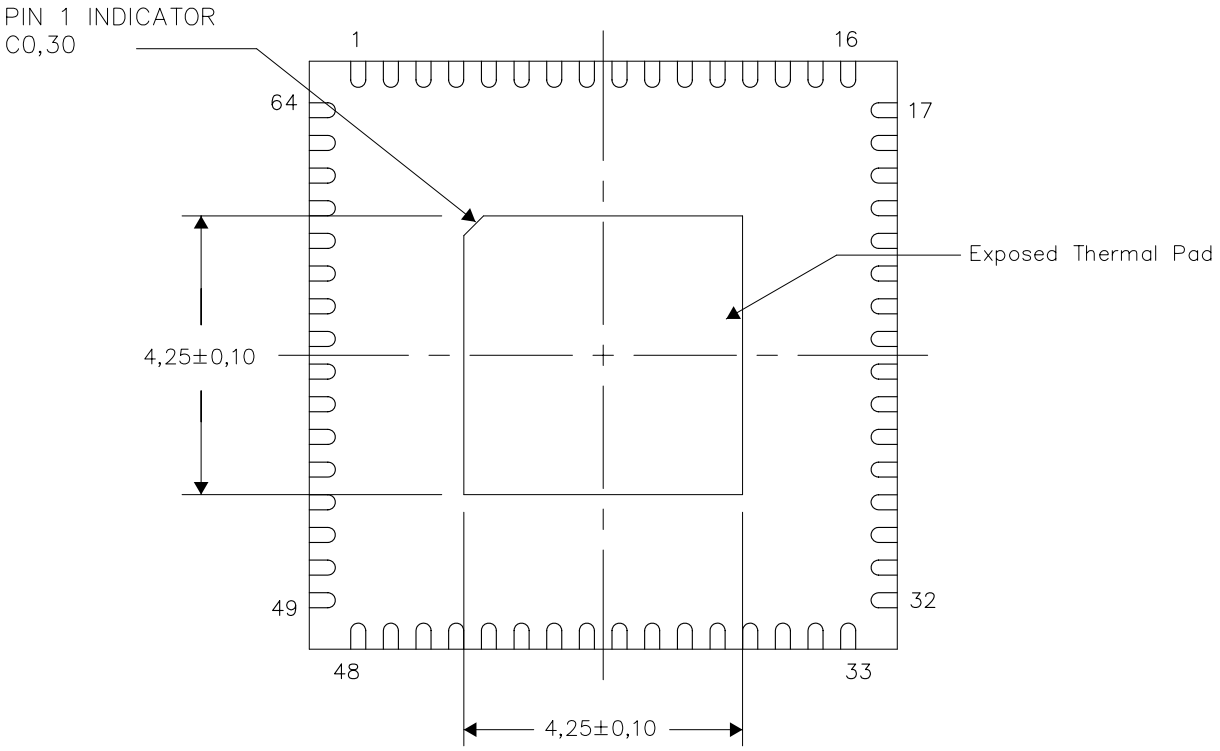
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



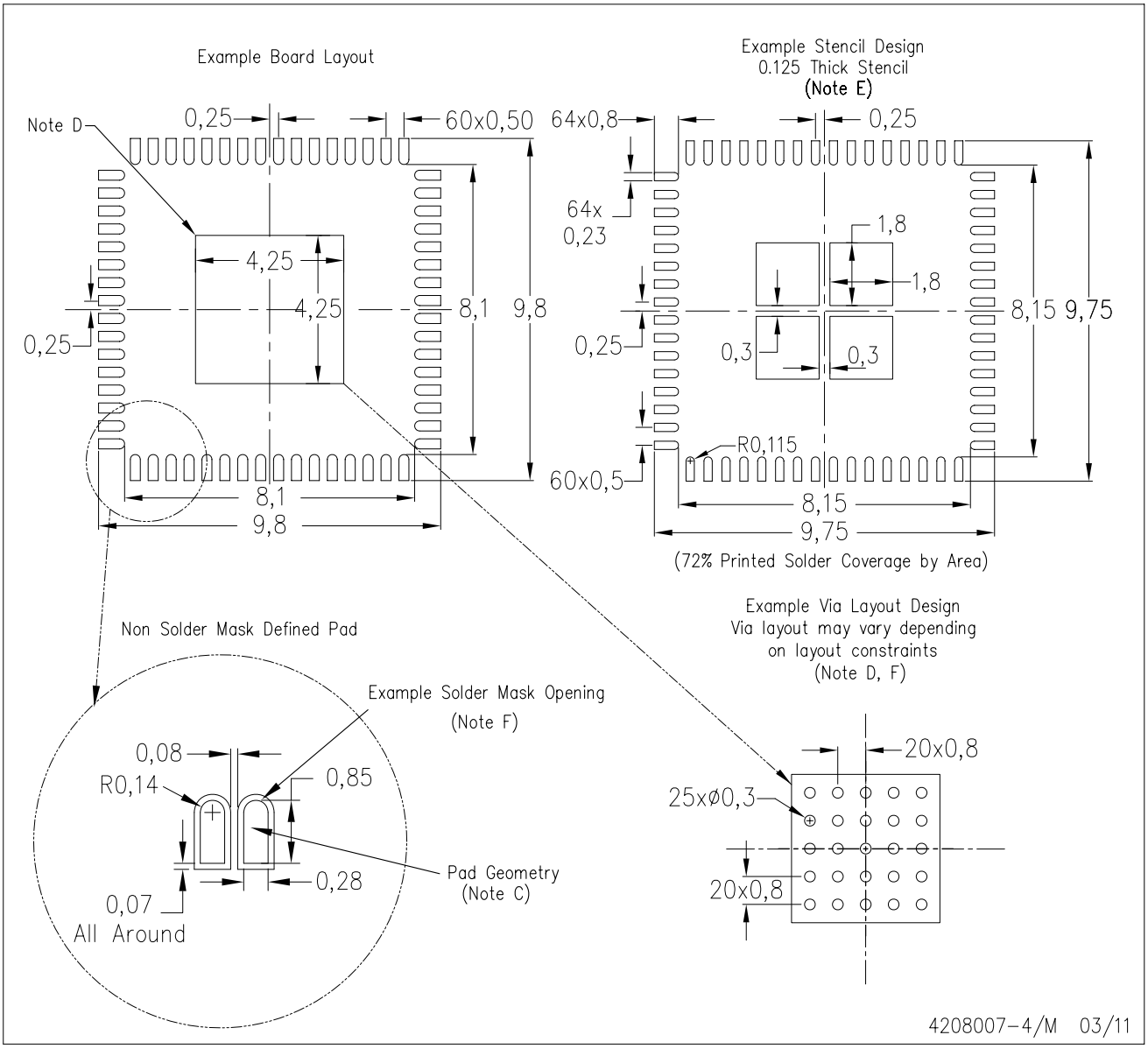
Bottom View

Exposed Thermal Pad Dimensions

4206192–3/P 01/12

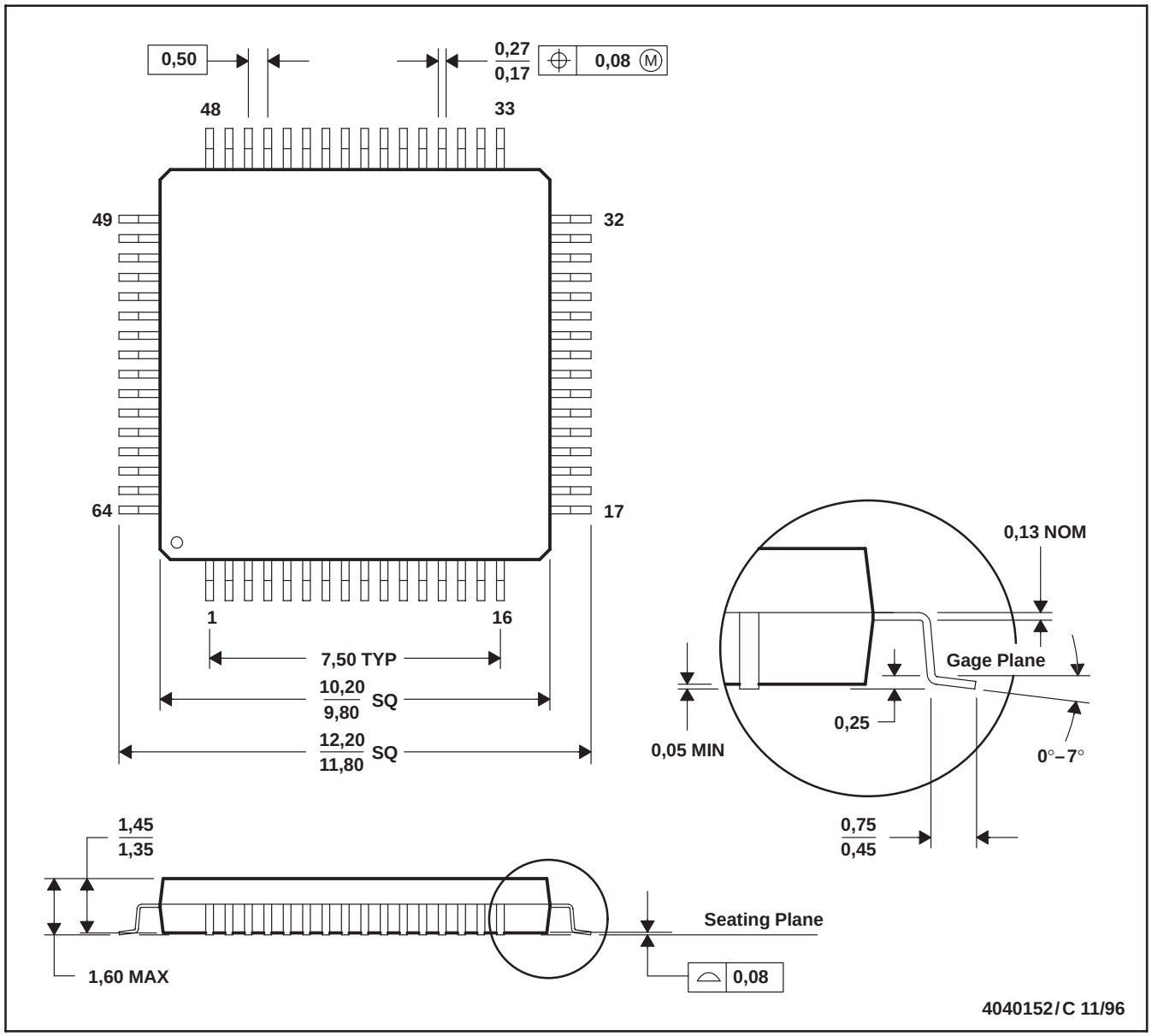
NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



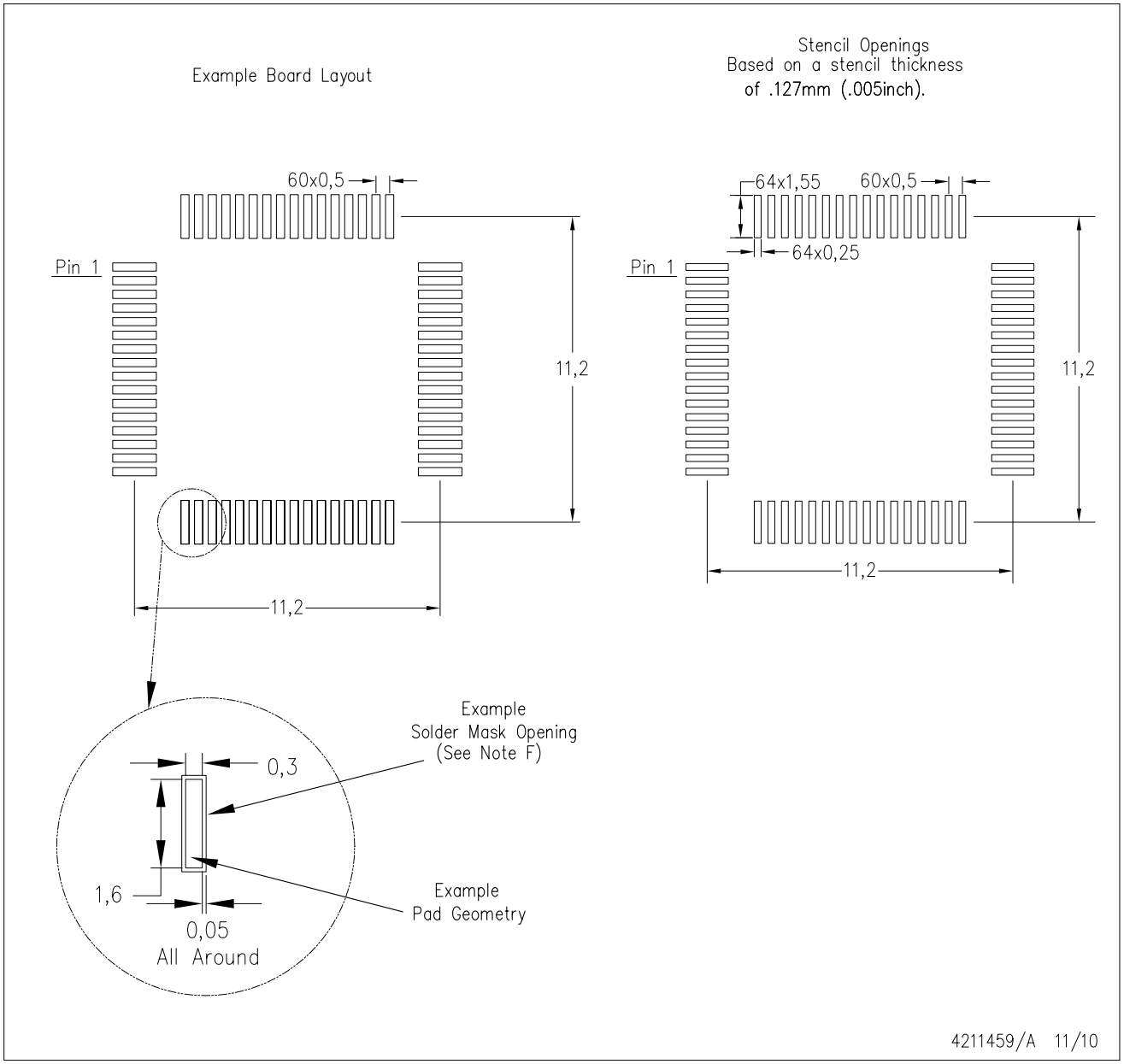
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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