

## 200-mA, Low- $I_Q$ , Low-Dropout Regulator for Portable Devices

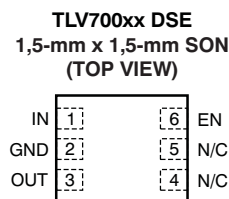
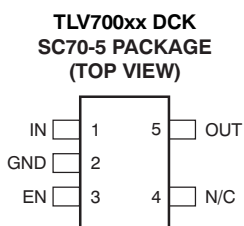
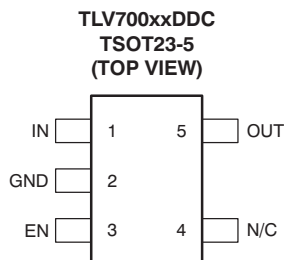
### FEATURES

- **Very Low Dropout:**
  - 43 mV at  $I_{OUT} = 50$  mA,  $V_{OUT} = 2.8$  V
  - 85 mV at  $I_{OUT} = 100$  mA,  $V_{OUT} = 2.8$  V
  - 175 mV at  $I_{OUT} = 200$  mA,  $V_{OUT} = 2.35$  V
- **2% Accuracy**
- **Low  $I_Q$ : 31  $\mu$ A**
- **Available in Fixed-Output Voltages from 1.2 V to 4.8 V**
- **High PSRR: 68 dB at 1 kHz**
- **Stable with Effective Capacitance of 0.1  $\mu$ F<sup>(1)</sup>**
- **Thermal Shutdown and Overcurrent Protection**
- **Available in 1,5-mm  $\times$  1,5-mm SON-6, SOT23-5, and SC-70 Packages**

<sup>(1)</sup> See the [Input and Output Capacitor Requirements](#) in the [Application Information](#) section.

### APPLICATIONS

- **Wireless Handsets**
- **Smart Phones, PDAs**
- **MP3 Players**
- **ZigBee<sup>®</sup> Networks**
- **Bluetooth<sup>®</sup> Devices**
- **Li-Ion Operated Handheld Products**
- **WLAN and Other PC Add-on Cards**

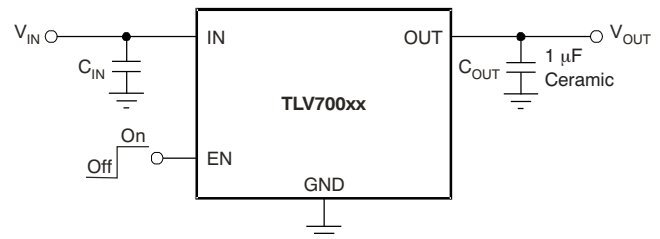


### DESCRIPTION

The TLV700xx series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1  $\mu$ F. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV700xx series of LDOs are available in 1,5-mm  $\times$  1,5-mm SON-6, TSOT23-5, and SC-70 packages.



**Typical Application Circuit (Fixed-Voltage Versions)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Bluetooth is a registered trademark of Bluetooth SIG.  
ZigBee is a registered trademark of the ZigBee Alliance.  
All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub> <sup>(2)</sup>
TLV700xx yyy z	<b>XX</b> is nominal output voltage (for example, 28 = 2.8 V). <b>YYY</b> is the package designator. <b>Z</b> is tape and reel quantity (R = 3000, T = 250).

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).
- (2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

At T<sub>J</sub> = –40°C to +125°C (unless otherwise noted). All voltages are with respect to GND.

PARAMETER	TLV700xx	UNIT
Input voltage range, V <sub>IN</sub>	–0.3 to +6.0	V
Enable voltage range, V <sub>EN</sub>	–0.3 to +6.0 <sup>(2)</sup>	V
Output voltage range, V <sub>OUT</sub>	–0.3 to +6.0	V
Maximum output current, I <sub>OUT</sub>	Internally limited	
Output short-circuit duration	Indefinite	
Total continuous power dissipation, P <sub>DISS</sub>	See <a href="#">Dissipation Ratings Table</a>	
ESD rating	Human body model (HBM)	2 kV
	Charged device model (CDM)	500 V
Operating junction temperature range, T <sub>J</sub>	–55 to +150	°C
Storage temperature range, T <sub>STG</sub>	–55 to +150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) V<sub>EN</sub> absolute maximum rating is V<sub>IN</sub> + 0.3 V or 6.0 V, whichever is less.

### DISSIPATION RATINGS

BOARD	PACKAGE	R <sub>θJC</sub>	R <sub>θJA</sub>	DERATING FACTOR ABOVE T <sub>A</sub> = +25°C	T <sub>A</sub> < +25°C	T <sub>A</sub> = +70°C	T <sub>A</sub> = +85°C
Low-K <sup>(1)</sup>	DCK	165°C/W	395°C/W	2.5 mW/°C	250 mW	140 mW	100 mW
High-K <sup>(2)</sup>	DCK	165°C/W	315°C/W	3.2 mW/°C	320 mW	175 mW	130 mW
High-K <sup>(2)</sup>	DSE	67°C/W	180°C/W	4.55 mW/°C	555 mW	305 mW	222 mW
Low-K <sup>(1)</sup>	DDC	90°C/W	280°C/W	3.6 mW/°C	360 mW	200 mW	145 mW
High-K <sup>(2)</sup>	DDC	90°C/W	200°C/W	5.0 mW/°C	500 mW	275 mW	200 mW

- (1) The JEDEC low-K (1s) board used to derive this data was a 3-inch × 3-inch, two-layer board with 2-ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

## ELECTRICAL CHARACTERISTICS

At  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$  or  $2.0\text{ V}$  (whichever is greater);  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = 0.9\text{ V}$ ,  $C_{OUT} = 1.0\text{ }\mu\text{F}$ , and  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range		2.0		5.5	V
$V_{OUT}$	DC output accuracy	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	-2		+2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$		1	15	mV
$V_{DO}$	Dropout voltage <sup>(1)</sup>	$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 50\text{ mA}$ , $V_{OUT} = 2.8\text{ V}$		43		mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 100\text{ mA}$ , $V_{OUT} = 2.8\text{ V}$		85		mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 200\text{ mA}$ , $V_{OUT} = 2.35\text{ V}$		175	250	mV
$I_{CL}$	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	220		860	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 0\text{ mA}$		31	55	$\mu\text{A}$
		$I_{OUT} = 200\text{ mA}$ , $V_{IN} = V_{OUT} + 0.5\text{ V}$		270		$\mu\text{A}$
$I_{SHDN}$	Ground pin current (shutdown)	$V_{EN} \leq 0.4\text{ V}$ , $V_{IN} = 2.0\text{ V}$		400		nA
		$V_{EN} \leq 0.4\text{ V}$ , $2.0\text{ V} \leq V_{IN} \leq 4.5\text{ V}$		1	2	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$V_{IN} = 2.3\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $f = 1\text{ kHz}$		68		dB
$V_N$	Output noise voltage	BW = 100 Hz to 100 kHz, $V_{IN} = 2.3\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 10\text{ mA}$		48		$\mu\text{V}_{RMS}$
$t_{STR}$	Startup time <sup>(2)</sup>	$C_{OUT} = 1.0\text{ }\mu\text{F}$ , $I_{OUT} = 200\text{ mA}$		100		$\mu\text{s}$
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		$V_{IN}$	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
$I_{EN}$	Enable pin current	$V_{IN} = V_{EN} = 5.5\text{ V}$		0.04	0.5	$\mu\text{A}$
UVLO	Undervoltage lockout	$V_{IN}$ rising		1.9		V
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		+160		$^\circ\text{C}$
		Reset, temperature decreasing		+140		$^\circ\text{C}$
$T_J$	Operating junction temperature		-40		+125	$^\circ\text{C}$

(1)  $V_{DO}$  is measured for devices with  $V_{OUT(NOM)} \geq 2.35\text{ V}$ .

(2) Startup time = time from EN assertion to  $0.98 \times V_{OUT(NOM)}$ .

### FUNCTIONAL BLOCK DIAGRAM

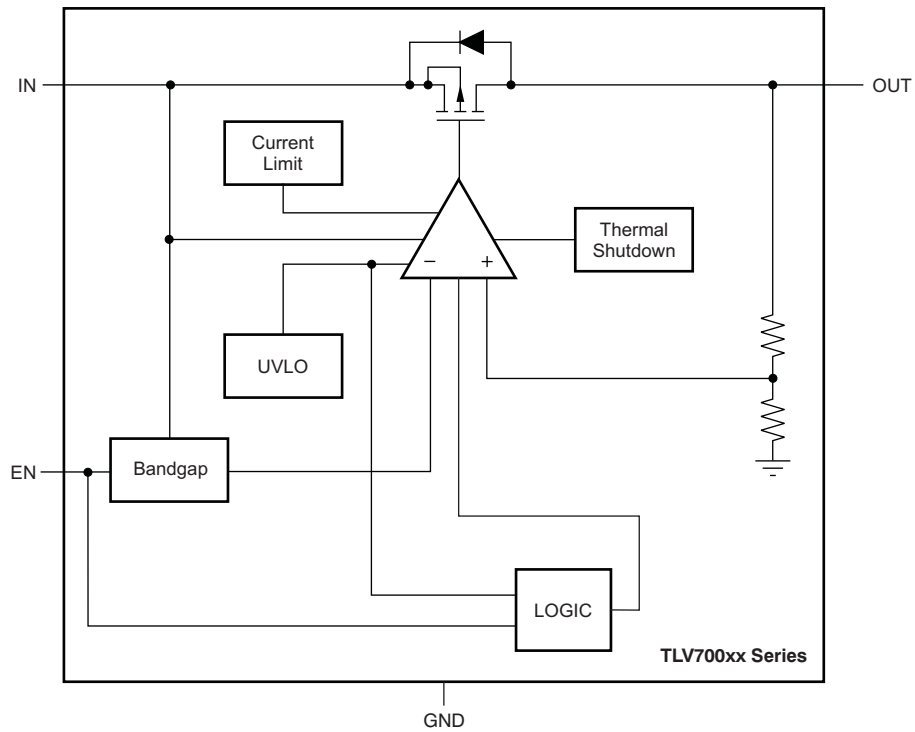
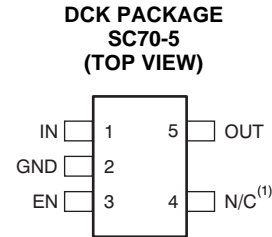
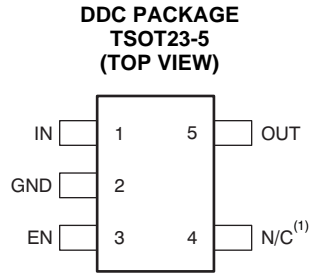
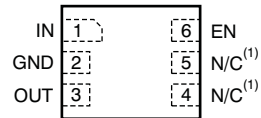


Figure 1. TLV700xx

## PIN CONFIGURATIONS



**DSE PACKAGE  
SON-6  
(TOP VIEW)**



(1) No connection.

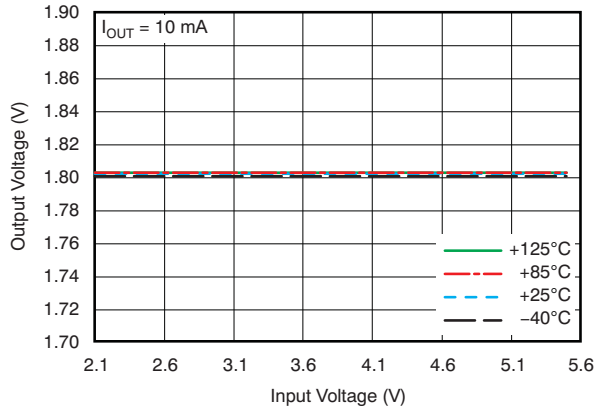
## PIN DESCRIPTIONS

NAME	SON-6 DSE	SC70-5 DCK	TSOT23-5 DDC	DESCRIPTION
IN	1	1	1	Input pin. A small 1- $\mu$ F ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See <a href="#">Input and Output Capacitor Requirements</a> in the <i>Application Information</i> section for more details.
GND	2	2	2	Ground pin
EN	6	3	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 $\mu$ A, nominal.
NC	4, 5	4	4	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	3	5	5	Regulated output voltage pin. A small 1- $\mu$ F ceramic capacitor is needed from this pin to ground to assure stability. See <a href="#">Input and Output Capacitor Requirements</a> in the <i>Application Information</i> section for more details.

### TYPICAL CHARACTERISTICS

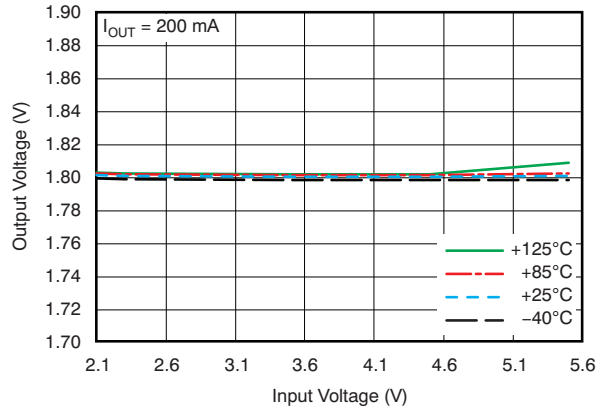
Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.0\text{ V}$ , whichever is greater;  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$ .

**TLV70018  
LINE REGULATION**



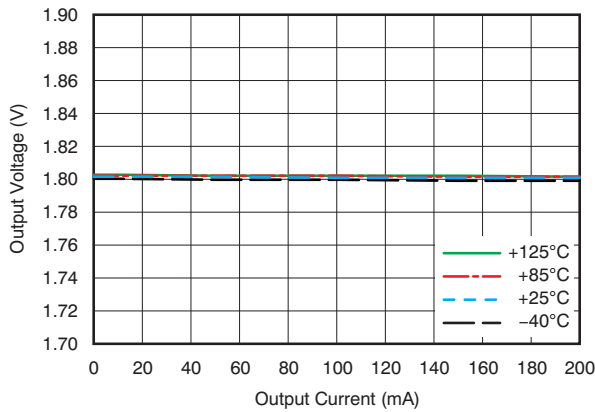
**Figure 2.**

**TLV70018  
LINE REGULATION**



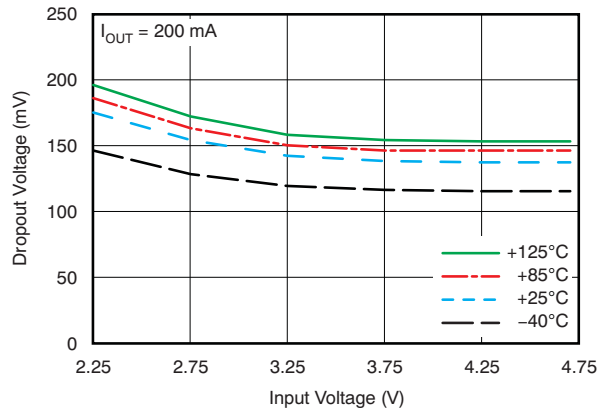
**Figure 3.**

**TLV70018  
LOAD REGULATION**



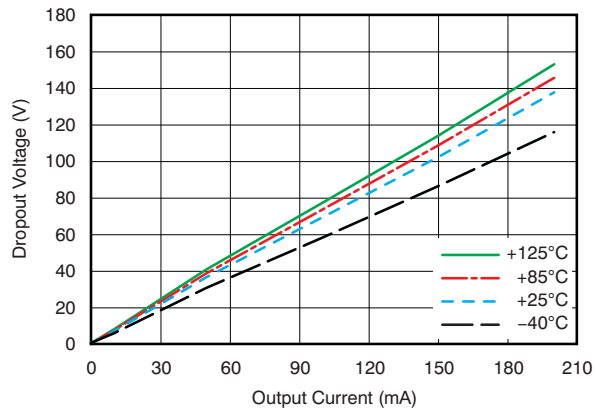
**Figure 4.**

**DROPOUT VOLTAGE  
vs INPUT VOLTAGE**



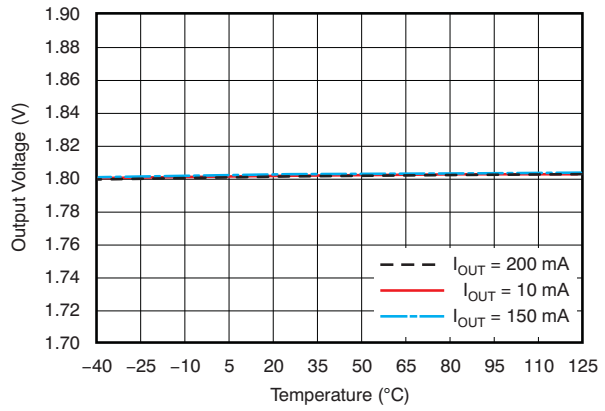
**Figure 5.**

**DROPOUT VOLTAGE vs OUTPUT CURRENT  
 $V_{OUT} = 4.8\text{ V}$**



**Figure 6.**

**TLV70018  
OUTPUT VOLTAGE vs TEMPERATURE**



**Figure 7.**

**TYPICAL CHARACTERISTICS (continued)**

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.0\text{ V}$ , whichever is greater;  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

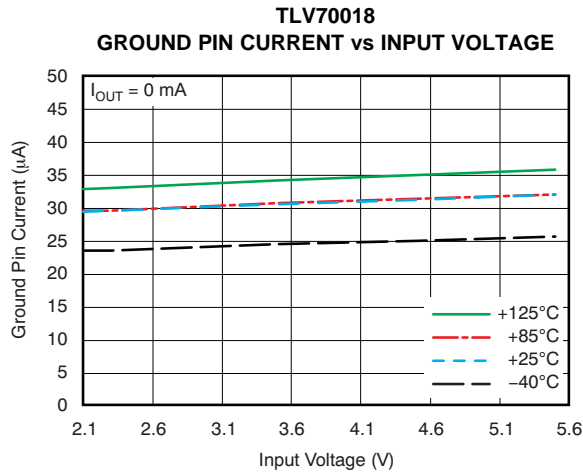


Figure 8.

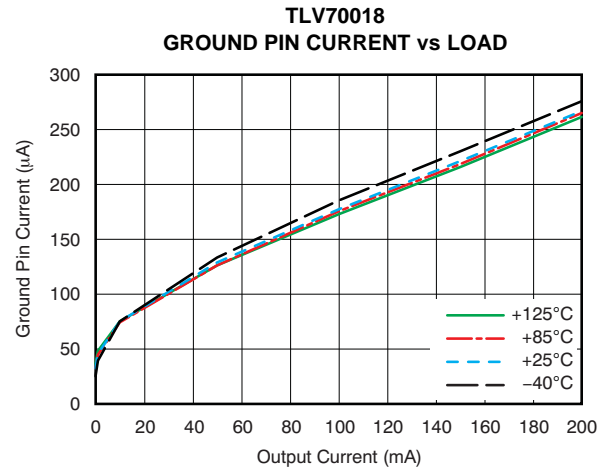


Figure 9.

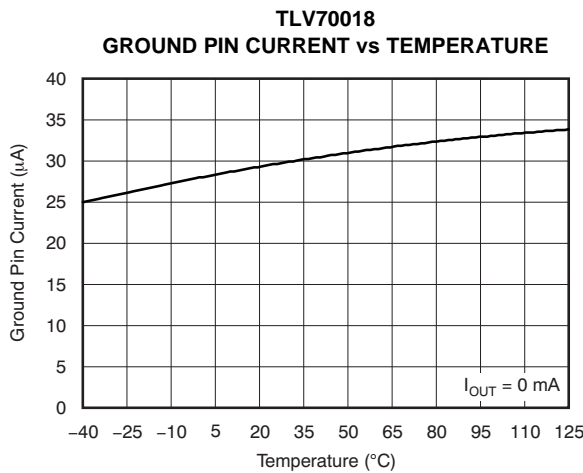


Figure 10.

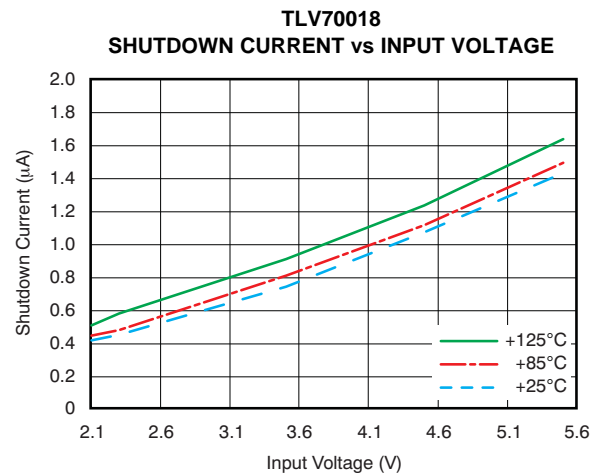


Figure 11.

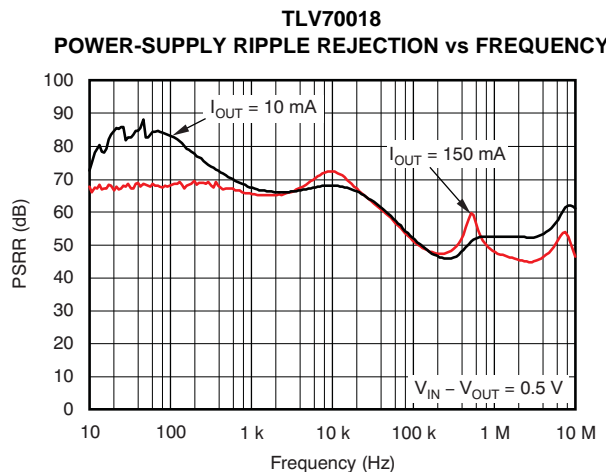


Figure 12.

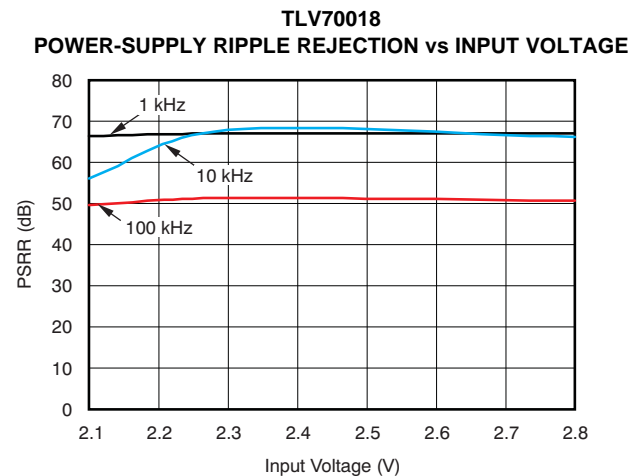


Figure 13.

**TYPICAL CHARACTERISTICS (continued)**

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.0\text{ V}$ , whichever is greater;  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

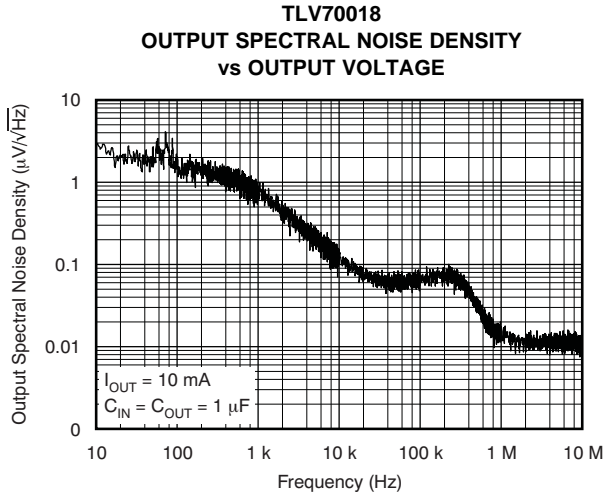


Figure 14.

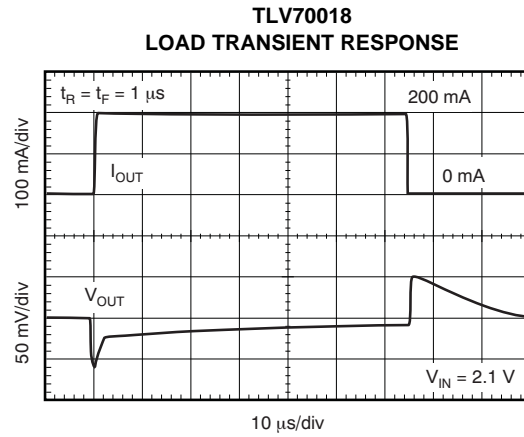


Figure 15.

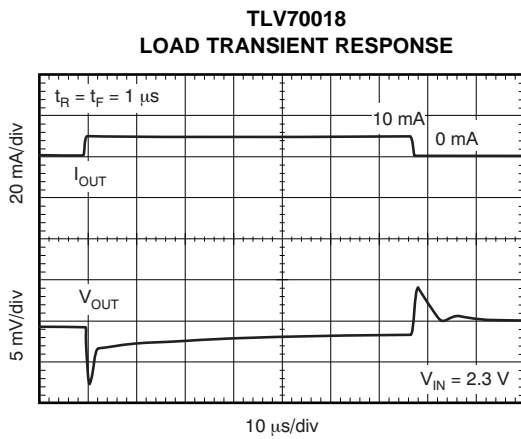


Figure 16.

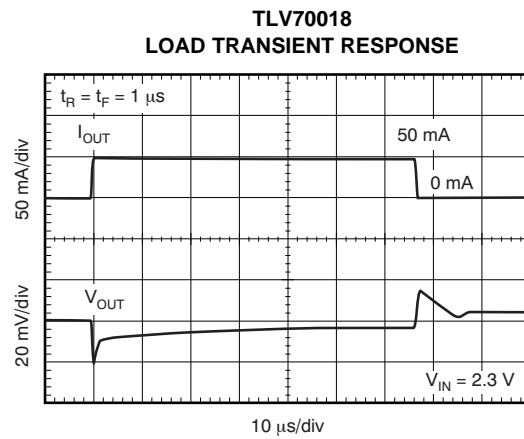


Figure 17.

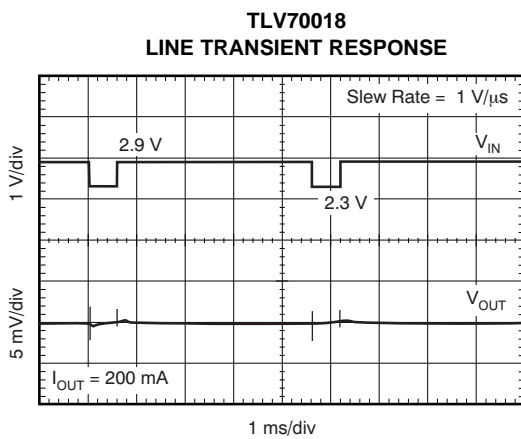


Figure 18.

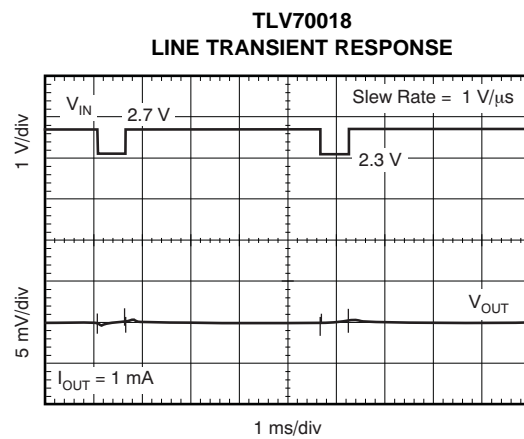
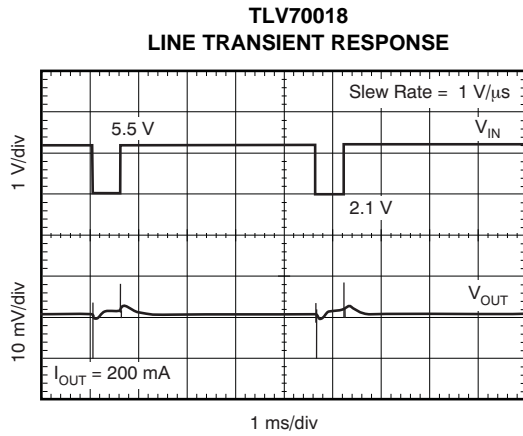


Figure 19.

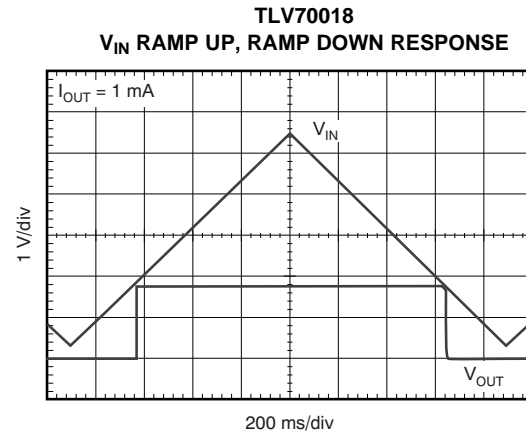


**TYPICAL CHARACTERISTICS (continued)**

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.0\text{ V}$ , whichever is greater;  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\ \mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .



**Figure 20.**



**Figure 21.**

## APPLICATION INFORMATION

The TLV700xx belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little ( $V_{IN} - V_{OUT}$ ) headroom, make this family of devices ideal for RF portable applications. This family of regulators offers current limit and thermal protection, and is specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Input and Output Capacitor Requirements

1.0- $\mu\text{F}$  X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV700xx is designed to be stable with an *effective capacitance* of 0.1  $\mu\text{F}$  or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1  $\mu\text{F}$ . This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1- $\mu\text{F}$  effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Note that using a 0.1- $\mu\text{F}$  rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1  $\mu\text{F}$ . Maximum ESR should be less than 200 m $\Omega$ .

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- $\mu\text{F}$  to 1.0- $\mu\text{F}$ , low ESR capacitor across the IN pin and GND in of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2  $\Omega$ , a 0.1- $\mu\text{F}$  input capacitor may be necessary to ensure stability.

### Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

### Internal Current Limit

The TLV700xx internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is  $V_{OUT} = I_{LIMIT} \times R_{LOAD}$ . The PMOS pass transistor dissipates  $(V_{IN} - V_{OUT}) \times I_{LIMIT}$  until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the [Thermal Information](#) section for more details.

The PMOS pass element in the TLV700xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

### Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9V. This relatively lower value of voltage required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO Logic 1 voltage level is lower than traditional microcontrollers. The device is turned OFF when the EN pin is held at less than 0.4V. When shutdown capability is not required, EN can be connected to the IN pin.

## Dropout Voltage

The TLV700xx uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as  $(V_{IN} - V_{OUT})$  approaches dropout. This effect is shown in [Figure 13](#) in the [Typical Characteristics](#) section.

## Transient Response

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

## Undervoltage Lockout (UVLO)

The TLV700xx uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

## Thermal Information

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV700xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV700xx into thermal shutdown degrades device reliability.

## Power Dissipation

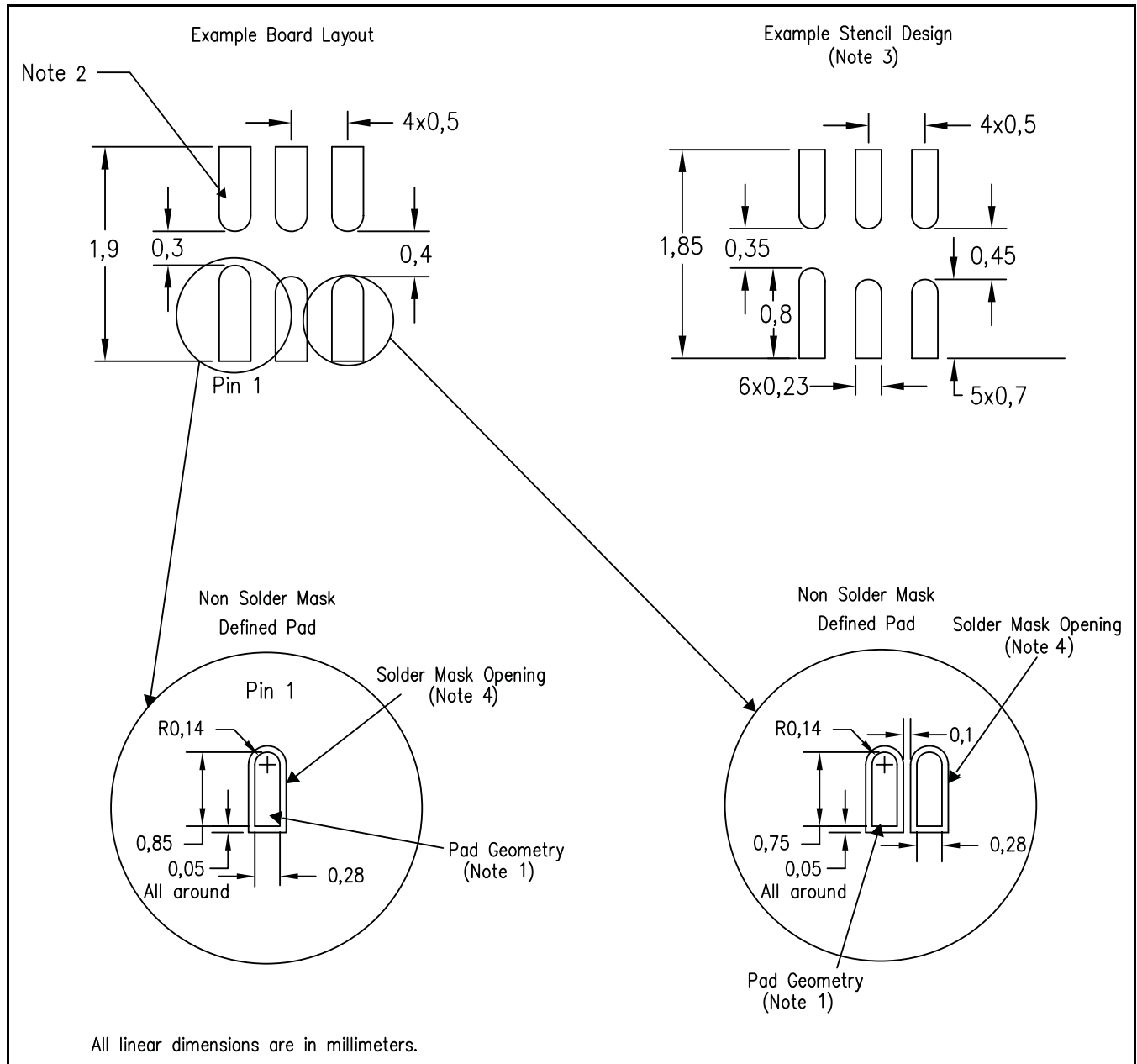
The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in the [Dissipation Ratings](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 1](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

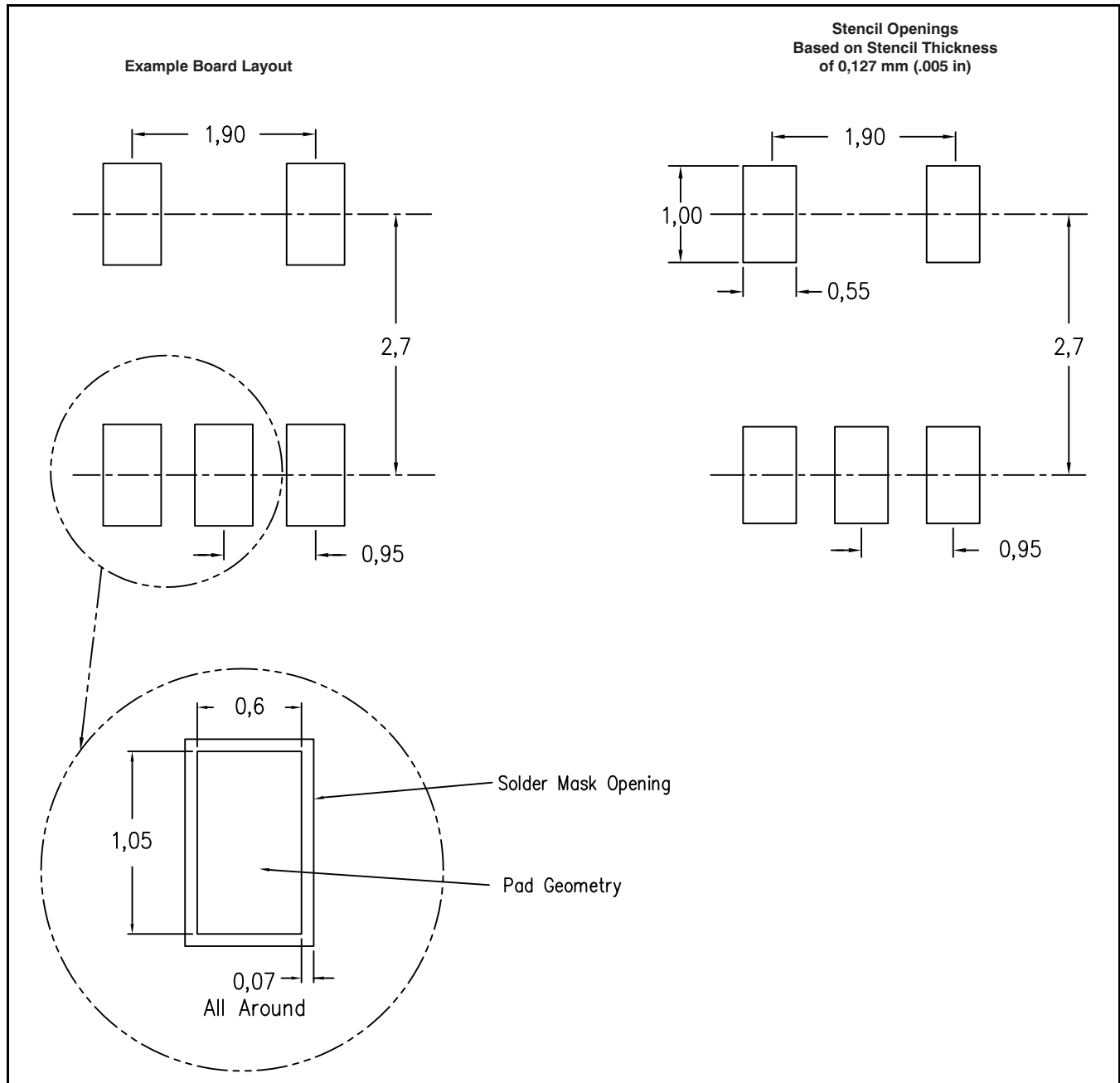
## Package Mounting

Solder pad footprint recommendations for the TLV700xx are available from the Texas Instruments web site at [www.ti.com](http://www.ti.com). The recommended land patterns for the DSE, DDC, and DCK packages are shown in [Figure 22](#), [Figure 23](#), and [Figure 24](#), respectively. [Figure 25](#), [Figure 26](#), and [Figure 27](#) show the mechanical package dimensions for the DSE, DDC, and DCK packages, respectively.



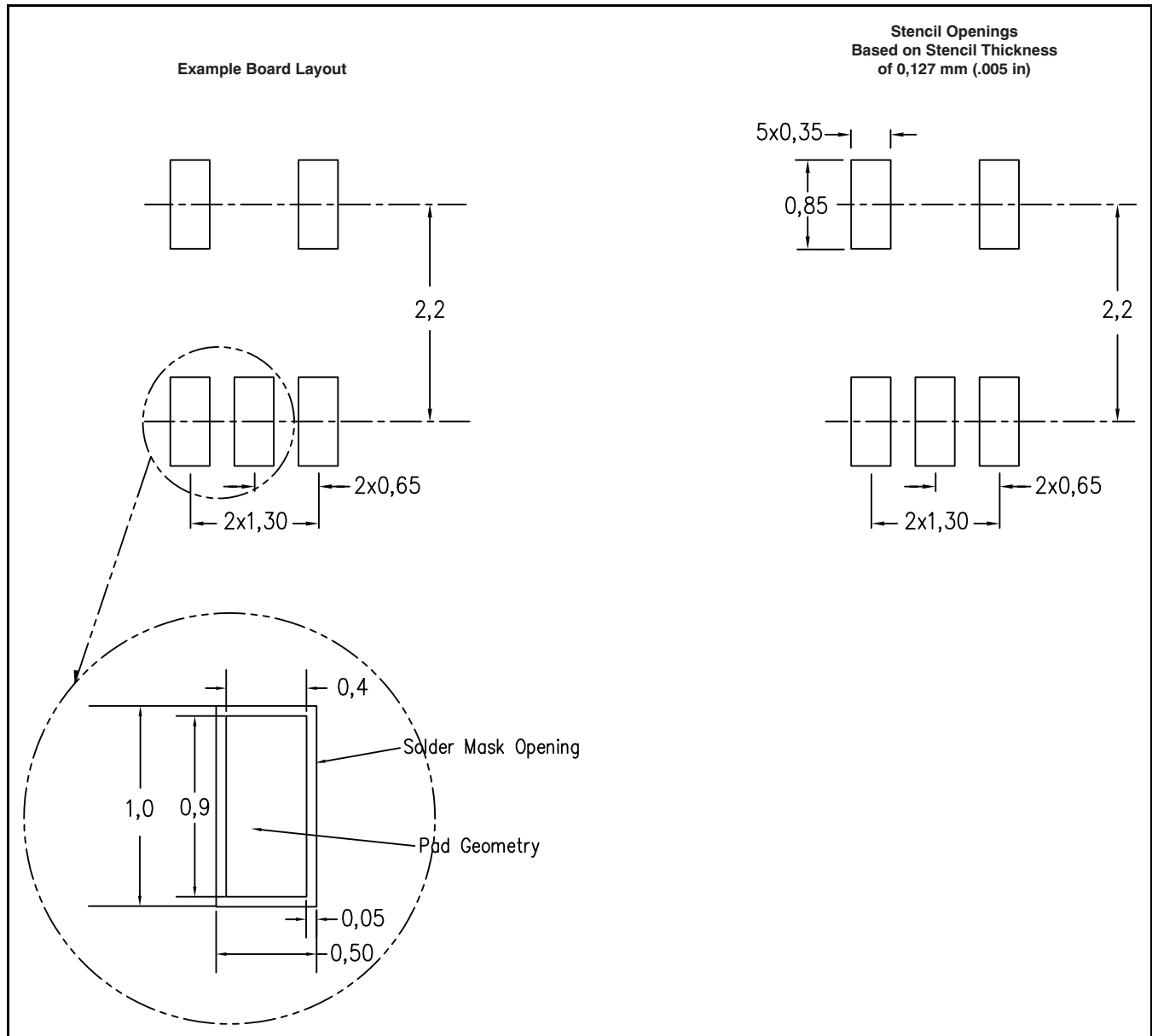
- (1) Publication IPC-7351 is recommended for alternate designs.
- (2) For more information, refer to TI application notes [SCBA017](#) and [SLUA271](#) (*Quad Flatpack No-Lead Logic Packages* and *QFN/SOIC PCB Attachment*, respectively) for specific thermal information, via requirements, and additional recommendations for board layout. These documents are available at the Texas Instruments web site (<http://www.ti.com>) by searching for the literature number.
- (3) Laser-cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for stencil design considerations.
- (4) Customers should contact their board fabrication site for minimum solder mask tolerances between signal pads.

**Figure 22. Recommended Land Pattern for DSE Package**



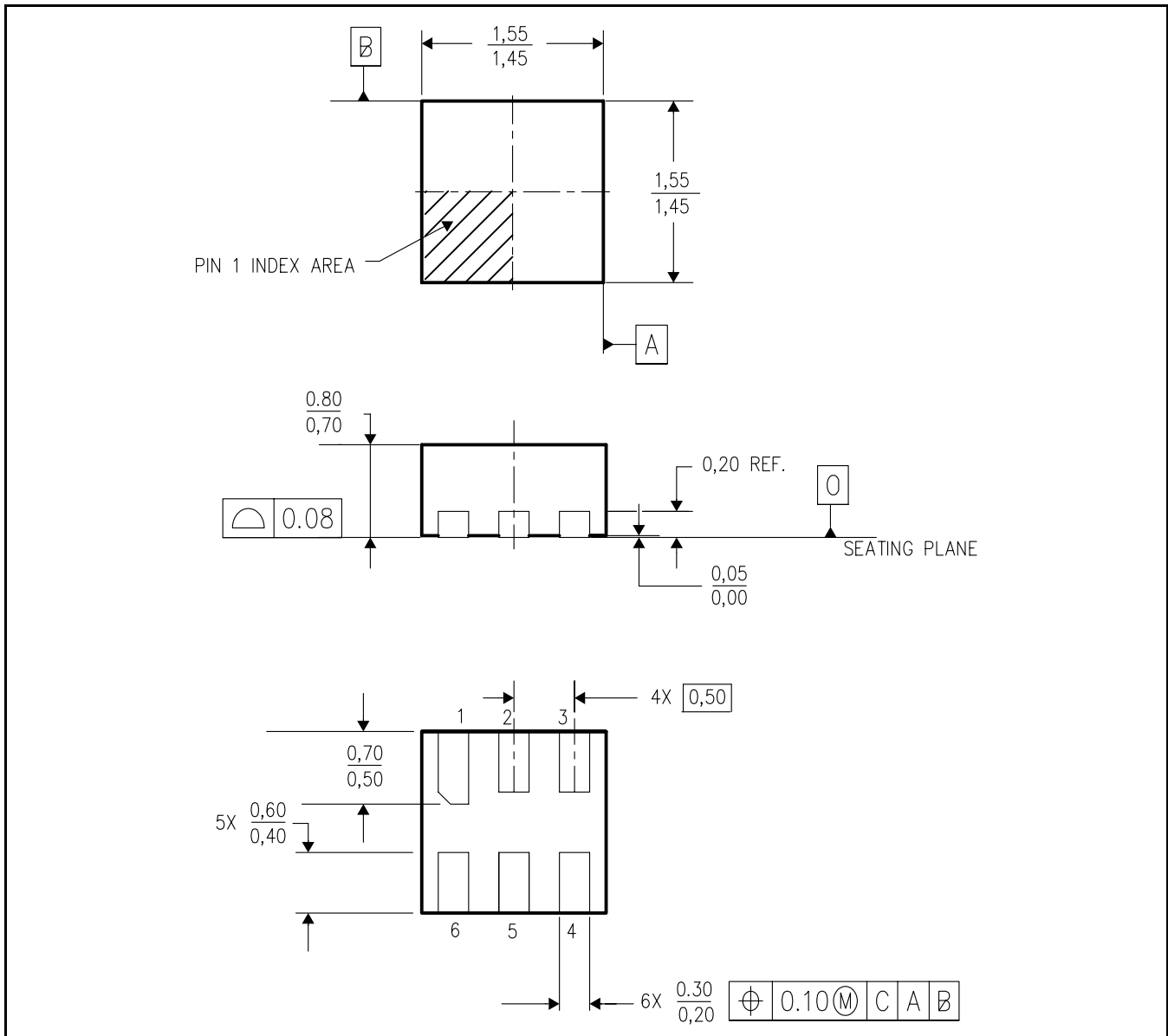
- (1) All linear dimensions are in millimeters.
- (2) Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- (3) Publication IPC-7351 is recommended for alternate designs.
- (4) Laser-cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric load solder paste. Refer to IPC-7525 for other stencil recommendations.

**Figure 23. Recommended Land Pattern for DDC Package**



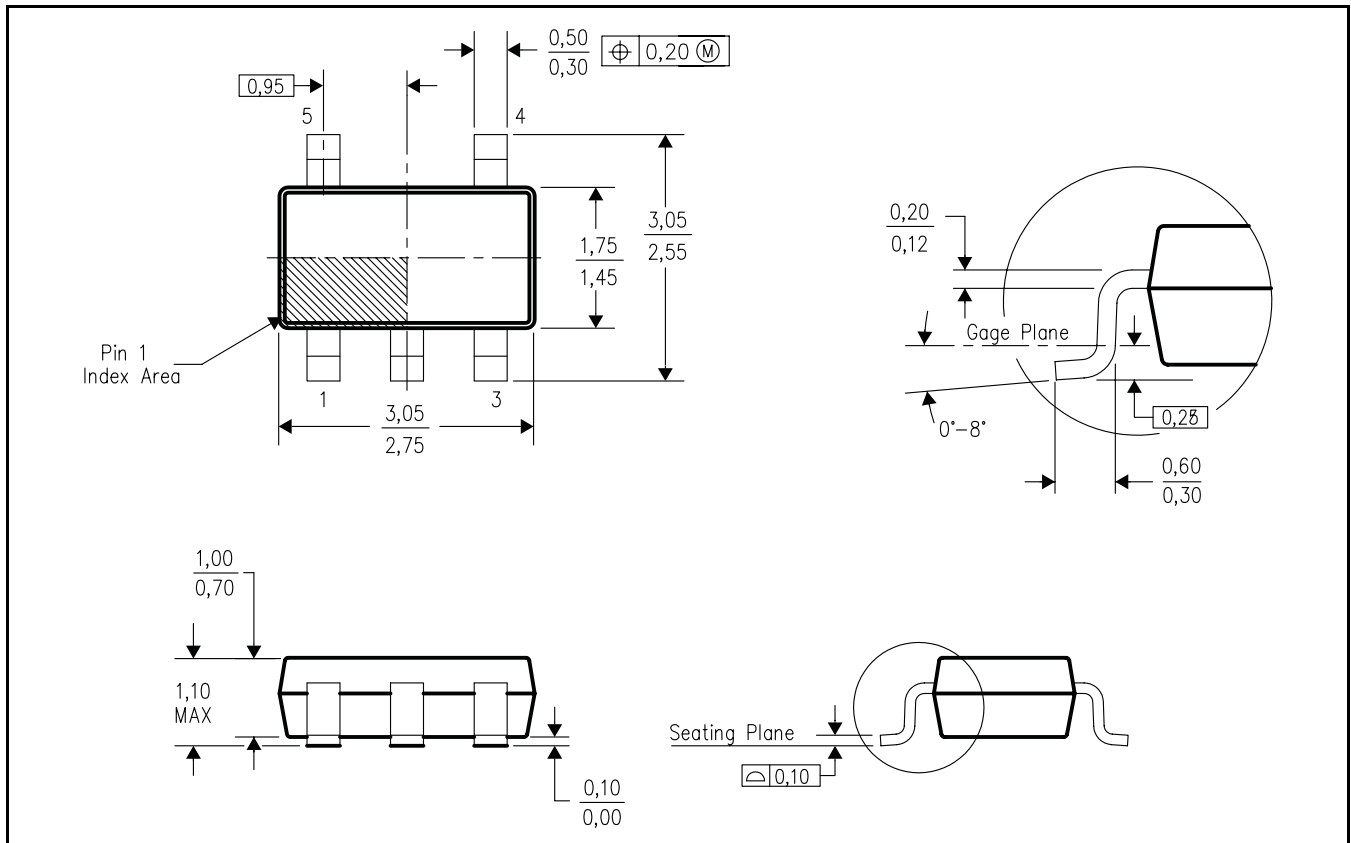
- (1) All linear dimensions are in millimeters.
- (2) Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- (3) Publication IPC-7351 is recommended for alternate designs.
- (4) Laser-cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric load solder paste. Refer to IPC-7525 for other stencil recommendations.

**Figure 24. Recommended Land Pattern for DCK Package**



- (1) All linear dimensions are in millimeters.
- (2) Small outline no-lead (SON) package configuration.

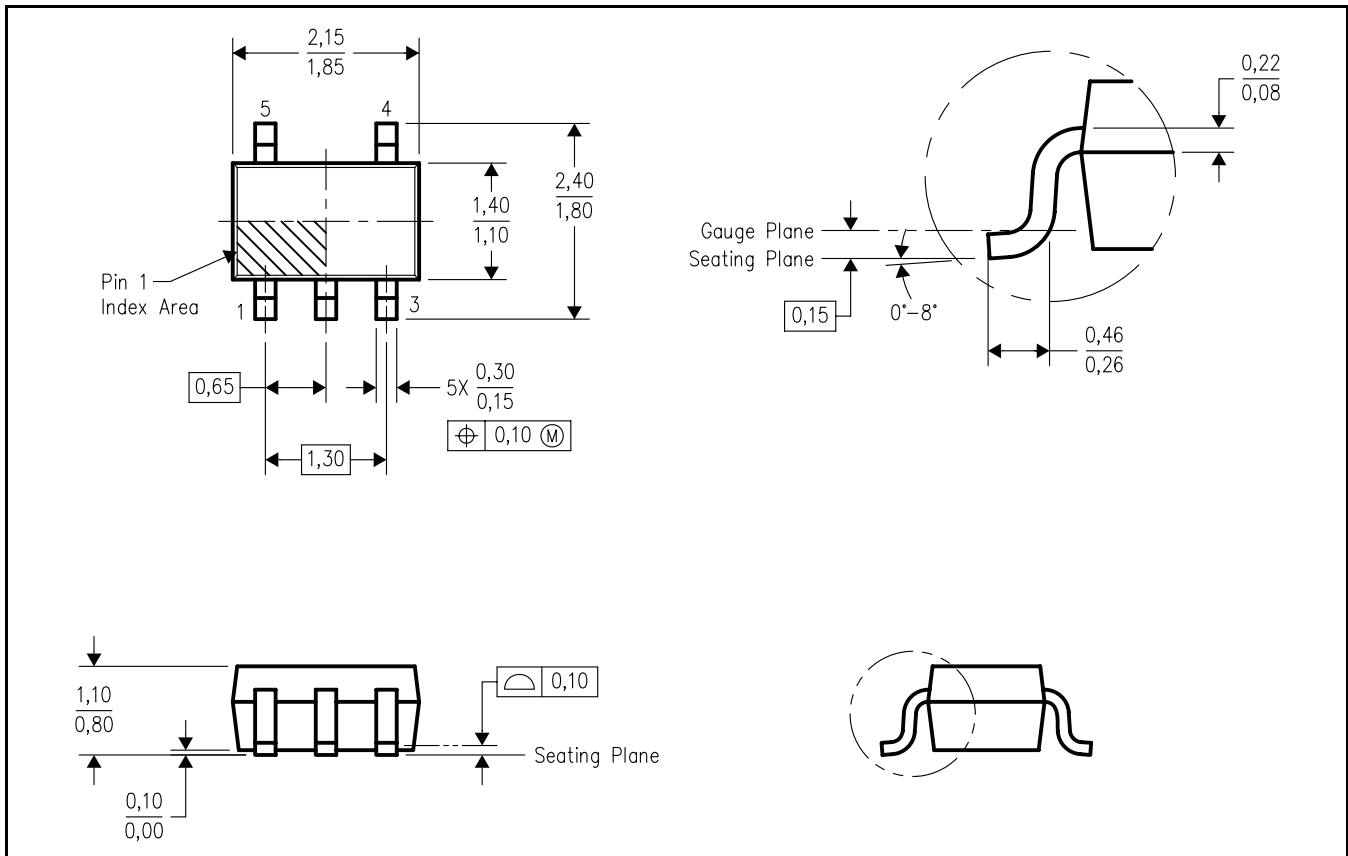
**Figure 25. DSE Package Dimensions**



- (1) All linear dimensions are in millimeters.
- (2) Body dimensions do not include mold flash or protrusion.
- (3) Falls within JEDEC MO-193 variation AB (pin 5).

**Figure 26. DDC Package Dimensions**





- (1) All linear dimensions are in millimeters.
- (2) Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0,15 per side.
- (3) Falls within JEDEC MO-203 variation AA.

**Figure 27. DCK Package Dimensions**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December, 2010) to Revision C	Page
• Added footnote 2 to <i>Absolute Maximum Ratings</i> table .....	2
• Changed <i>output current limit</i> typical and maximum specifications .....	3
• Deleted previous Figure 12, <i>Current Limit vs Input Voltage</i> typical characteristic .....	7

Changes from Revision A (April, 2010) to Revision B	Page
• Removed TLV701xx device references throughout document .....	1
• Changed minimum output voltage available from 0.7 V to 1.2 V .....	1
• Added footnote (1) .....	1
• Changed footnote 2 for <i>Ordering Information</i> table to reflect minimum output voltage of 1.2 V .....	2
• Deleted $V_{OUT} < 1\text{ V}$ specification .....	3
• Deleted <i>Active pulldown resistance</i> parameter .....	3
• Removed TLV701xx block diagram .....	4
• Changed <a href="#">Figure 5</a> title .....	6
• Changed <a href="#">Figure 6</a> title .....	6
• Updated <i>Application Information</i> section to reflect minimum output voltage availability of 1.2 V .....	10
• Deleted references to TLV701xx throughout <i>Application Information</i> .....	10
• Revised <a href="#">Shutdown</a> section .....	10

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TLV70012DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70012DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70012DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70012DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70012DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70012DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70013DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70013DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70015DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70015DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70015DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70015DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70015DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70015DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70018DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70018DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70018DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TLV70018DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70018DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70018DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70025DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70025DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70025DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70025DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70025DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70025DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70028DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70028DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70028DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70028DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70028DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70028DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70029DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70029DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70030DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TLV70030DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70030DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70030DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70030DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70030DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70033DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70033DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70033DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70033DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLV70033DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70033DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70036DDCR	PREVIEW	SOT	DDC	5	3000	TBD	Call TI	Call TI	
TLV70036DDCT	PREVIEW	SOT	DDC	5	250	TBD	Call TI	Call TI	
TLV70036DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70036DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

---

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV70018, TLV70025, TLV70033 :**

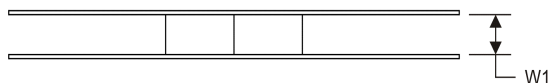
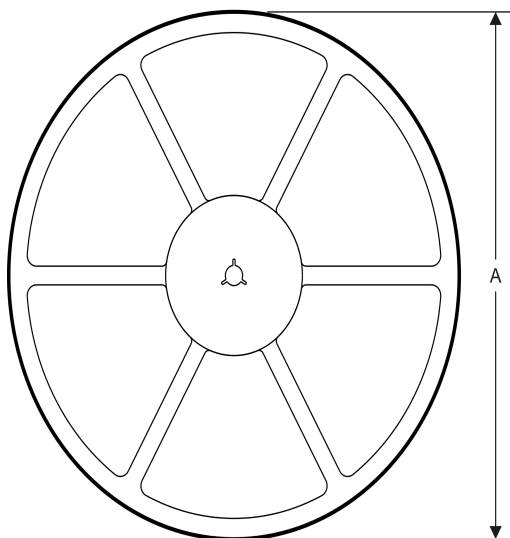
- Automotive: [TLV70018-Q1](#), [TLV70025-Q1](#), [TLV70033-Q1](#)

NOTE: Qualified Version Definitions:

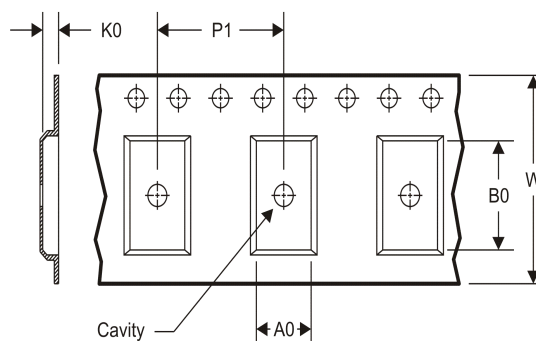
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70012DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70012DCKT	SC70	DCK	5	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70012DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70012DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70012DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70012DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70012DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70012DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70013DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70013DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70015DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70015DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70015DCKT	SC70	DCK	5	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70015DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70015DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70015DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70015DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70015DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70015DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70015DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70015DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70015DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70018DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70018DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70018DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70018DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70018DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70018DCKT	SC70	DCK	5	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70018DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70018DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70018DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70018DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70018DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70018DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70018DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70018DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70025DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70025DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70025DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70025DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70025DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70025DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70025DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70025DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70025DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70028DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70028DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70028DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70028DCKT	SC70	DCK	5	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70028DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70028DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70028DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70028DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70028DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70028DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70028DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70028DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70029DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70029DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70029DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70029DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70030DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70030DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70030DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70030DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70030DCKT	SC70	DCK	5	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70030DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70030DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70030DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70030DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70030DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70030DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70030DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70030DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70030DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70033DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70033DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70033DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70033DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70033DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70033DCKT	SC70	DCK	5	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TLV70033DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70033DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TLV70033DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70033DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70033DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70033DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70036DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70036DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70012DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TLV70012DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TLV70012DDCR	SOT	DDC	5	3000	406.0	348.0	63.0
TLV70012DDCT	SOT	DDC	5	250	202.0	201.0	28.0
TLV70012DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV70012DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70012DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70012DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70013DDCR	SOT	DDC	5	3000	202.0	201.0	28.0
TLV70013DDCT	SOT	DDC	5	250	202.0	201.0	28.0
TLV70015DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TLV70015DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
TLV70015DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TLV70015DCKT	SC70	DCK	5	250	203.0	203.0	35.0
TLV70015DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70015DDCR	SOT	DDC	5	3000	406.0	348.0	63.0
TLV70015DDCT	SOT	DDC	5	250	406.0	348.0	63.0
TLV70015DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70015DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70015DSER	WSON	DSE	6	3000	203.0	203.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70015DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70015DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70018DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TLV70018DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV70018DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
TLV70018DCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV70018DCKT	SC70	DCK	5	250	203.0	203.0	35.0
TLV70018DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TLV70018DDCR	SOT	DDC	5	3000	406.0	348.0	63.0
TLV70018DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70018DDCT	SOT	DDC	5	250	406.0	348.0	63.0
TLV70018DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70018DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV70018DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70018DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70018DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70025DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
TLV70025DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV70025DCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV70025DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70025DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70025DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV70025DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70025DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70025DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70028DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TLV70028DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
TLV70028DCKT	SC70	DCK	5	250	203.0	203.0	35.0
TLV70028DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TLV70028DDCR	SOT	DDC	5	3000	406.0	348.0	63.0
TLV70028DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70028DDCT	SOT	DDC	5	250	406.0	348.0	63.0
TLV70028DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70028DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70028DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV70028DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70028DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70029DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV70029DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70029DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70029DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70030DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV70030DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TLV70030DCKR	SC70	DCK	5	3000	203.0	203.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70030DCKT	SC70	DCK	5	250	203.0	203.0	35.0
TLV70030DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TLV70030DCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV70030DDCR	SOT	DDC	5	3000	406.0	348.0	63.0
TLV70030DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70030DDCT	SOT	DDC	5	250	406.0	348.0	63.0
TLV70030DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70030DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV70030DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70030DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70030DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70033DCKR	SC70	DCK	5	3000	203.0	203.0	35.0
TLV70033DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TLV70033DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV70033DCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV70033DCKT	SC70	DCK	5	250	203.0	203.0	35.0
TLV70033DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TLV70033DDCR	SOT	DDC	5	3000	406.0	348.0	63.0
TLV70033DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70033DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70033DDCT	SOT	DDC	5	250	406.0	348.0	63.0
TLV70033DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70033DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV70033DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70033DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV70036DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV70036DSET	WSON	DSE	6	250	202.0	201.0	28.0

DCK (R-PDSO-G5)

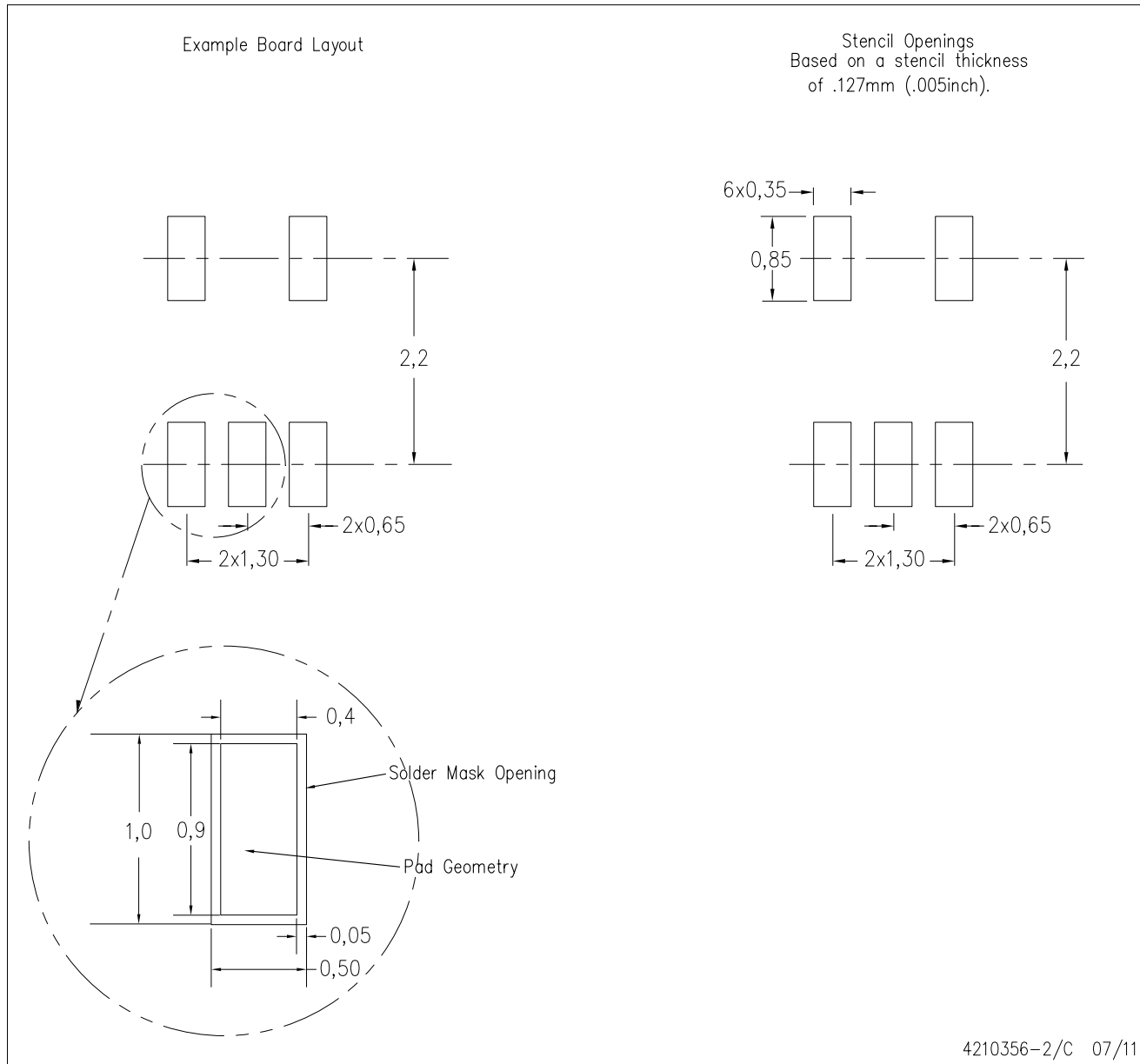
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

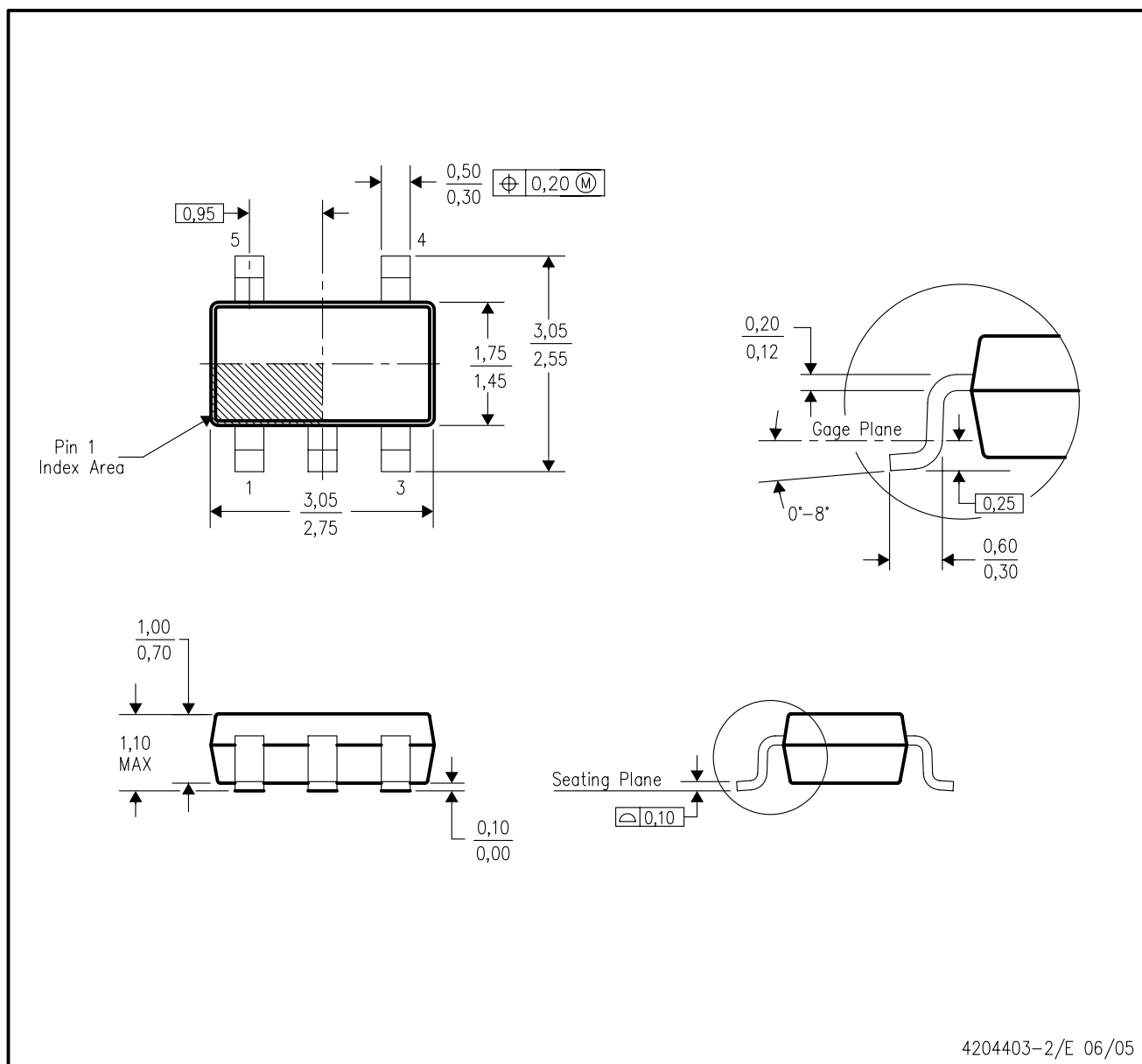
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DDC (R-PDSO-G5)

PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-193 variation AB (5 pin).

DSE (S-PDSO-N6)

PLASTIC SMALL OUTLINE



4207810/A 03/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - D. This package is lead-free.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Mobile Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2012, Texas Instruments Incorporated