# 16-Channel Wideband Video Multiplexers

## FEATURES

- Crosstalk: –100 dB @ 5 MHz
- 300 MHz Bandwidth
- Low Input and Output Capacitance
- Low Power: 75 μW
- Low $r_{DS(on)}$: 50 Ω
- On-Board Address Latches
- Disable Output

## BENEFITS

- High Video Quality
- Reduced Insertion Loss
- Reduced Input Buffer Requirements
- Minimizes Power Consumption
- Simplifies Bus Interface

## APPLICATIONS

- Video Switching/Routing
- High Speed Data Routing
- RF Signal Multiplexing
- Precision Data Acquisition
- Crosspoint Arrays
- FLIR Systems

## DESCRIPTION

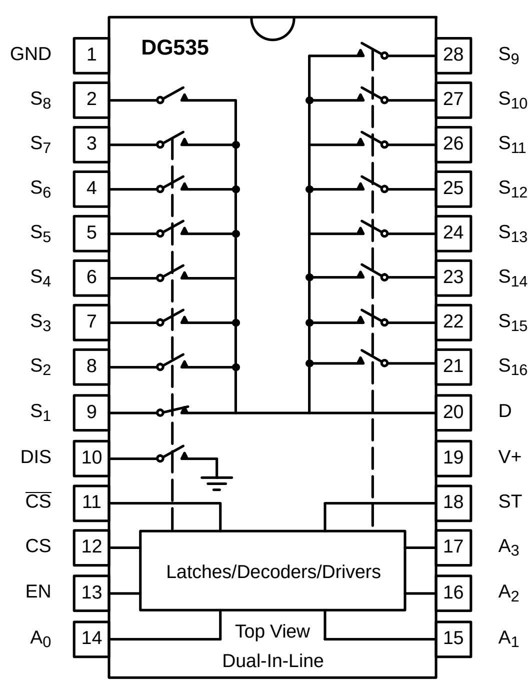
The DG535/536 are 16-channel multiplexers designed for routing one of 16 wideband analog or digital input signals to a single output. They feature low input and output capacitance, low on-resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "off" isolation. In the on state, the switches pass signals in either direction, allowing them to be used as multiplexers or as demultiplexers.

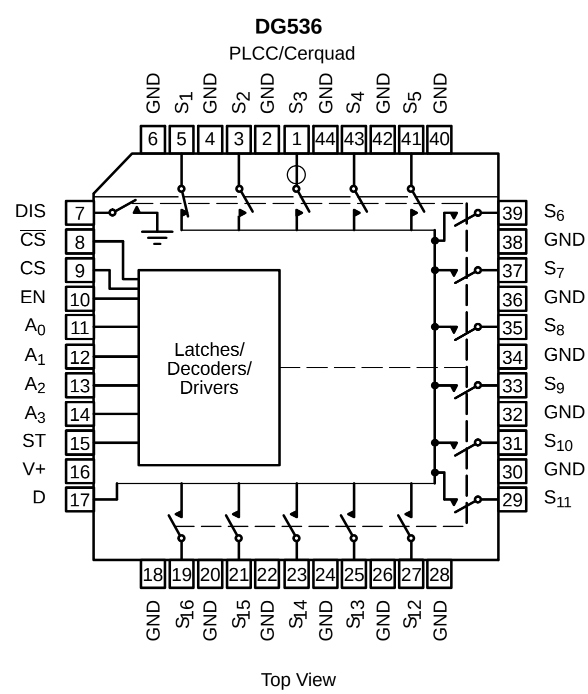
On-chip address latches and decode logic simplify microprocessor interface. Chip Select and Enable inputs simplify addressing in large matrices. Single-supply operation and a low 75-μW power consumption vastly reduces power supply requirements.

Theses devices are built on a proprietary D/CMOS process which creates low-capacitance DMOS FETs and high-speed, low-power CMOS logic on the same substrate.

For more information please refer to Vishay Siliconix Application Note AN501 (FaxBack document number 70608).

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



## TRUTH TABLES AND ORDERING INFORMATION

| ORDERING INFORMATION | | |
|---|---|---|
| **Temperature Range** | **Package** | **Part Number** |
| –40 to 85°C | 28-Pin Plastic DIP | DG535DJ |
| | 44-Pin PLCC | DG536DN |
| –55 to 125°C | 28-Pin Sidebraze | DG535AP |
| | | DG535AP/883 |
| | 44-Pin Cerquad | DG536AM/883 |

| TRUTH TABLE | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **EN** | **CS** | **$\overline{CS}$** | **ST[a]** | **$A_3$** | **$A_2$** | **$A_1$** | **$A_0$** | **Channel Selected** | **Disable[b]** |
| 0 | X | X | 1 | X | X | X | X | None | High Z |
| X | 0 | X | | | | | | | |
| X | X | 1 | | | | | | | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $S_1$ | Low Z |
| | | | | 0 | 0 | 0 | 1 | $S_2$ | |
| | | | | 0 | 0 | 1 | 0 | $S_3$ | |
| | | | | 0 | 0 | 1 | 1 | $S_4$ | |
| | | | | 0 | 1 | 0 | 0 | $S_5$ | |
| | | | | 0 | 1 | 0 | 1 | $S_6$ | |
| | | | | 0 | 1 | 1 | 0 | $S_7$ | |
| | | | | 0 | 1 | 1 | 1 | $S_8$ | |
| | | | | 1 | 0 | 0 | 0 | $S_9$ | |
| | | | | 1 | 0 | 0 | 1 | $S_{10}$ | |
| | | | | 1 | 0 | 1 | 0 | $S_{11}$ | |
| | | | | 1 | 0 | 1 | 1 | $S_{12}$ | |
| | | | | 1 | 1 | 0 | 0 | $S_{13}$ | |
| | | | | 1 | 1 | 0 | 1 | $S_{14}$ | |
| | | | | 1 | 1 | 1 | 0 | $S_{15}$ | |
| | | | | 1 | 1 | 1 | 1 | $S_{16}$ | |
| X | X | X | 0 | X | X | X | X | Maintains previous switch condition | High Z or Low Z |
| Logic "0" = $V_{AL} \leq 4.5$ V<br>Logic "1" = $V_{AH} \geq 10.5$ V<br>X = Don't Care | | | | | | | | | |

Notes:
a. Strobe input (ST) is level triggered.
b. Low Z, High Z = impedance of Disable Output to GND. Disable output sinks current when any channel is selected.

## ABSOLUTE MAXIMUM RATINGS

V+ to GND . . . . . . . . –0.3 V to +18 V
Digital Inputs . . . . . . . . (GND – 0.3 V) to (V+ plus 2 V ) or 20 mA, whichever occurs first
$V_S$, $V_D$ . . . . . . . . (GND – 0.3 V) to V+ plus 2 V) or 20 mA, whichever occurs first
Current (any terminal) Continuous . . . . . . . . 20 mA
Current (S or D) Pulsed 1 ms 10% duty cycle . . . . . . . . 40 mA
Storage Temperature (A Suffix) . . . . . . . . –65 to 150°C
(D Suffix) . . . . . . . . –65 to 125°C
Power Dissipation (Package)[a]
28-Pin Plastic DIP[b] . . . . . . . . 625 mW
28-Pin Sidebraze[c] . . . . . . . . 1200 mW
44-Pin PLCC[d] . . . . . . . . 450 mW
44-Pin Cerquad[e] . . . . . . . . 825 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 8.6 mW/°C above 75°C.
c. Derate 16 mW/°C above 75°C.
d. Derate 6 mW/°C above 75°C.
e. Derate 11 mW/°C above 75°C.

## SPECIFICATIONS[a]

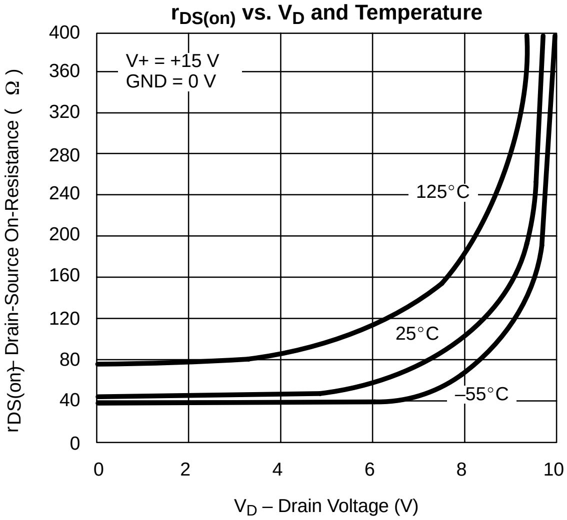
| Parameter | Symbol | Test Conditions Unless Otherwise Specified<br>V+ = 15 V, ST, CS = 10.5 V<br>$\overline{CS}$ = 4.5 V, $V_A$ = 4.5 or 10.5 V[f] | | Temp[b] | Typ[c] | A Suffix –55 to 125°C<br>Min[c] | A Suffix<br>Max[c] | D Suffix –40 to 85°C<br>Min[c] | D Suffix<br>Max[c] | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | | |
| Analog Signal Range[e] | $V_{ANALOG}$ | | | Full | | 0 | 10 | 0 | 10 | V |
| Drain-Source<br>On-Resistance | $r_{DS(on)}$ | $I_S$ = –1 mA, $V_D$ = 3 V<br>EN = 10.5 V<br>Sequence Each Switch On | | Room<br>Full | 55 | | 90<br>120 | | 90<br>120 | Ω |
| Resistance Match | $\Delta r_{DS(on)}$ | | | Room | | | 9 | | 9 | |
| Source Off<br>Leakage Current | $I_{S(off)}$ | $V_S$ = 3 V, $V_D$ = 0 V, EN = 4.5 V | | Room<br>Full | | –10<br>–100 | 10<br>100 | –10<br>–100 | 10<br>100 | nA |
| Drain On<br>Leakage Current | $I_{D(on)}$ | $V_S$ = $V_D$ = 3 V, EN = 10.5 V | | Room<br>Full | | –10<br>–1000 | 10<br>1000 | –10<br>–100 | –10<br>–100 | |
| Disable Output | $R_{DISABLE}$ | $I_{DISABLE}$ = 1 mA, EN = 10.5 V | | Room<br>Full | 100 | | 200<br>250 | | 200<br>250 | Ω |
| **Digital Control** | | | | | | | | | | |
| Input Voltage High | $V_{AIH}$ | | | Full | | 10.5 | | 10.5 | | V |
| Input Voltage Low | $V_{AIL}$ | | | Full | | | 4.5 | | 4.5 | |
| Address Input Current | $I_{AI}$ | $V_A$ = GND or V+ | | Room<br>Full | <0.01 | –1<br>–100 | 1<br>100 | –1<br>–100 | 1<br>100 | µA |
| Address Input<br>Capacitance | $C_A$ | | | Full | 5 | | | | | pF |
| **Dynamic Characteristics** | | | | | | | | | | |
| On State Input<br>Capacitance[e] | $C_{S(on)}$ | $V_D$ = $V_S$ = 3 V | PLCC | Room | 32 | | 45 | | 45 | pF |
| | | | Cerquad | Room | 35 | | | | | |
| | | | DIP | Room | 40 | | 55 | | 55 | |
| Off State Input<br>Capacitance[e] | $C_{S(off)}$ | $V_S$ = 3 V | PLCC | Room | 2 | | 8 | | 8 | |
| | | | Cerquad | Room | 5 | | | | | |
| | | | DIP | Room | 3 | | | | | |
| Off State Output<br>Capacitance[e] | $C_{D(off)}$ | $V_D$ = 3 V | PLCC | Room | 8 | | 20 | | 20 | |
| | | | Cerquad | Room | 12 | | | | | |
| | | | DIP | Room | 9 | | | | | |
| Multiplexer Switching Time | $t_{TRANS}$ | See Figure 4 | | Full | | | 300 | | 300 | ns |
| Break-Before-Make<br>Interval | $t_{OPEN}$ | | | Full | | 25 | | 25 | | |
| EN, CS, $\overline{CS}$, ST, $t_{ON}$ | $t_{ON}$ | See Figure 2 and 3 | | Full | | | 300 | | 300 | |
| EN, CS, $\overline{CS}$, ST, $t_{OFF}$ | $t_{OFF}$ | See Figure 2 | | Full | | | 150 | | 150 | |
| Charge Injection | Q | See Figure 5 | | Room | –35 | | | | | pC |
| Single-Channel Crosstalk | $X_{TALK(SC)}$ | $R_{IN}$ = 75 Ω<br>$R_L$ = 75 Ω<br>f = 5 MHz<br>See Figure 9 | PLCC | Room | –100 | | | | | dB |
| | | | Cerquad | Room | –93 | | | | | |
| | | | DIP | Room | –60 | | | | | |
| Chip Disabled Crosstalk | $X_{TALK(CD)}$ | $R_{IN}$ = $R_L$ = 75 Ω<br>f = 5 MHz<br>EN = 4.5 V<br>See Figure 8 | PLCC | Room | –85 | | | | | |
| | | | Cerquad | Room | –84 | | | | | |
| | | | DIP | Room | –60 | | | | | |

| SPECIFICATIONS[a] | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified<br>V+ = 15 V, ST, CS = 10.5 V<br>$\overline{CS}$ = 4.5 V, $V_A$ = 4.5 or 10.5 V[f] | | Temp[b] | Typ[c] | A Suffix –55 to 125°C<br>Min[c] | A Suffix<br>Max[c] | D Suffix –40 to 85°C<br>Min[c] | D Suffix<br>Max[c] | Unit |
| **Dynamic Characteristics (Cont'd)** | | | | | | | | | | |
| Adjacent Input Crosstalk | $X_{TALK(AI)}$ | $R_{IN}$ = 10 Ω<br>$R_L$ = 10 kΩ<br>f = 5 MHz<br>See Figure 10 | PLCC | Room | –92 | | | | | dB |
| | | | Cerquad | Room | –87 | | | | | |
| | | | DIP | Room | –72 | | | | | |
| All Hostile Crosstalk[e] | $X_{TALK(AH)}$ | $R_{IN}$ = 10 Ω<br>$R_L$ = 10 kΩ<br>f = 5 MHz<br>See Figure 7 | PLCC | Room | –74 | –60 | | –60 | | |
| | | | Cerquad | Room | –74 | | | | | |
| | | | DIP | Room | –60 | | | | | |
| Bandwidth | BW | $R_L$ = 50 Ω, See Figure 6 | | Room | 500 | | | | | MHz |
| **Power Supplies** | | | | | | | | | | |
| Positive Supply Current | I+ | Any One Channgel Selected with All Logic Inputs at GND or V+ | | Room<br>Full | 5 | | 50<br>100 | | 50<br>100 | μA |
| Supply Voltage Range | V+ | | | Full | | 10 | 16.5 | 10 | 16.5 | V |
| **Minimum Input Timing Requirements** | | | | | | | | | | |
| Strobe Pulse Width | $t_{SW}$ | See Figure 1 | | Full | | 200 | | 200 | | ns |
| $A_0$, $A_1$, $A_2$, $A_3$ CS, $\overline{CS}$, EN Data Valid to Strobe | $t_{DW}$ | | | Full | | 100 | | 100 | | |
| $A_0$, $A_1$, $A_2$, $A_3$ CS, $\overline{CS}$, EN Data Valid after Strobe | $t_{WD}$ | | | Full | | 50 | | 50 | | |

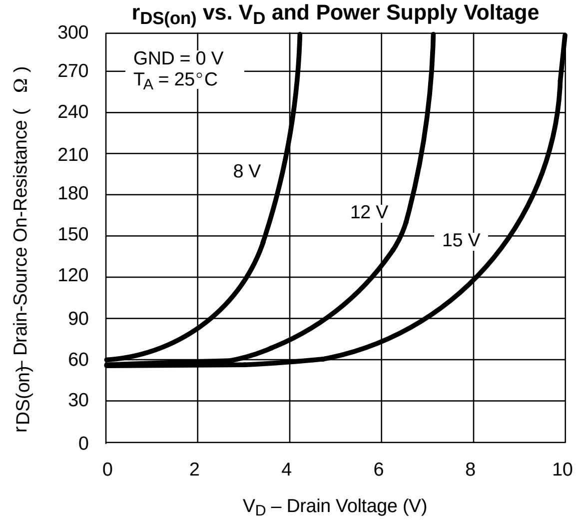
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. $V_A$ = input voltage to perform proper function.

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

$r_{DS(on)}$ vs. $V_D$ and Temperature




$r_{DS(on)}$ vs. $V_D$ and Power Supply Voltage





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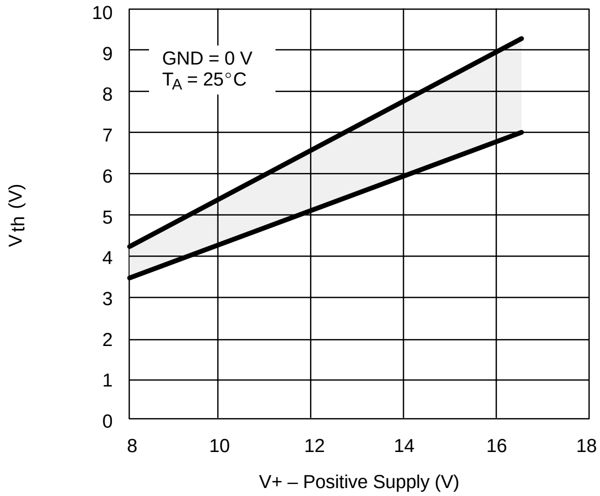
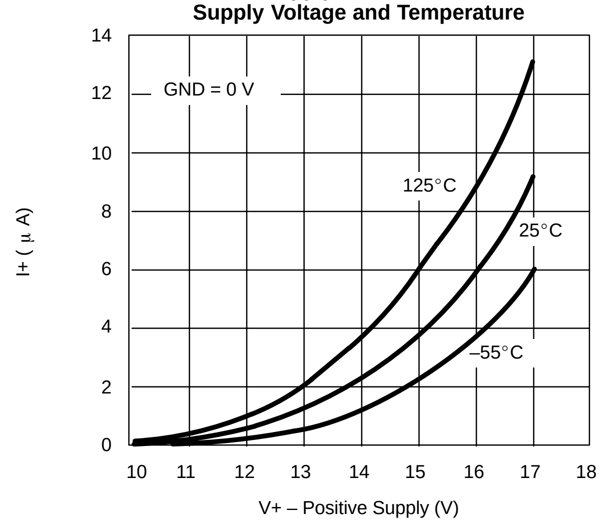
## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

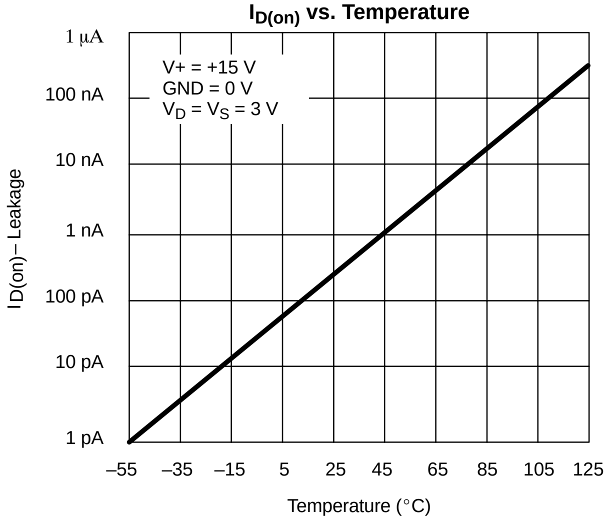
**Logic Input Switching Threshold vs. Supply Voltage (V+)**



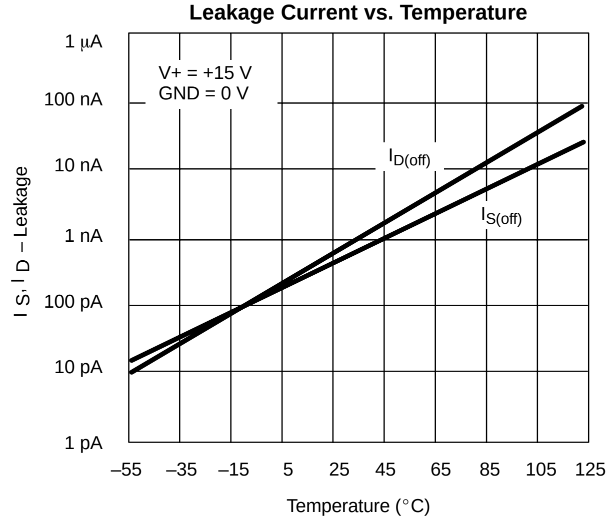

**Supply Current vs. Supply Voltage and Temperature**



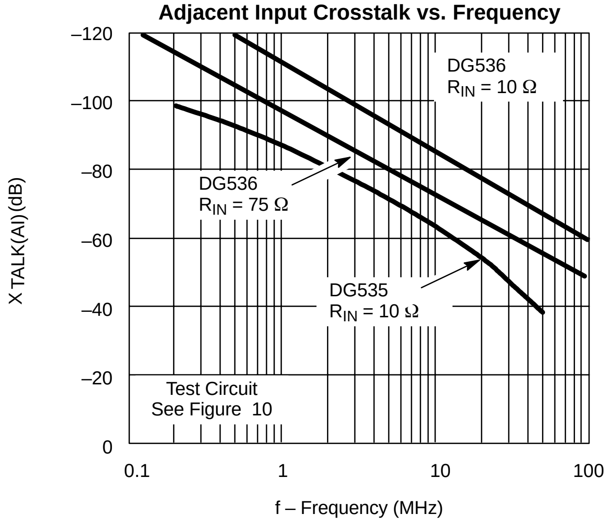

**$I_{D(on)}$ vs. Temperature**



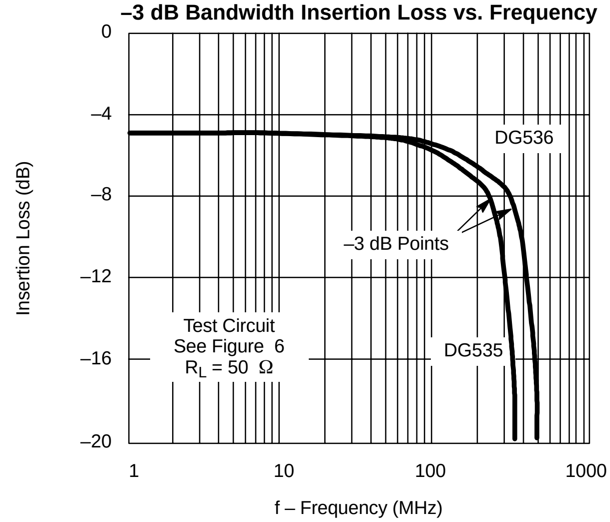

**Leakage Current vs. Temperature**




**Adjacent Input Crosstalk vs. Frequency**

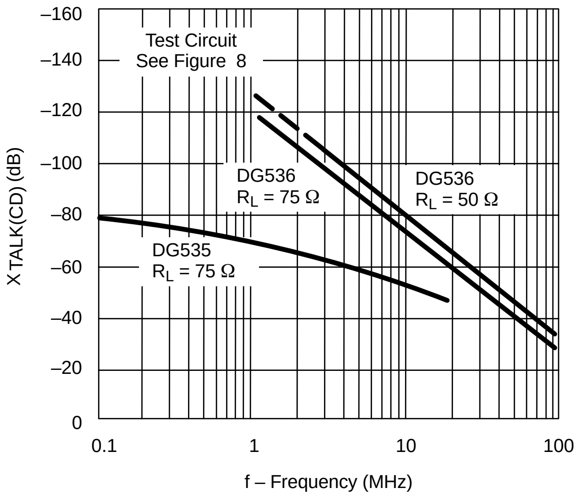



**–3 dB Bandwidth Insertion Loss vs. Frequency**

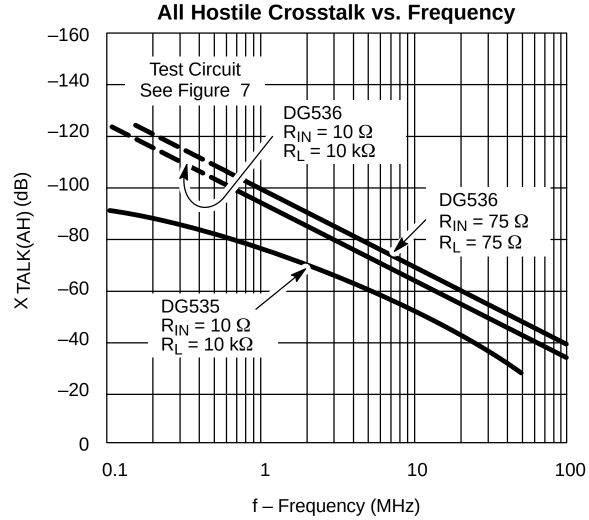


## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

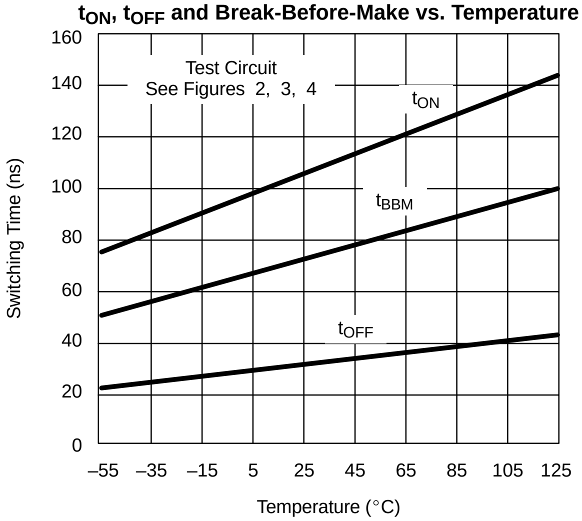
**Chip Disable Crosstalk vs. Frequency**



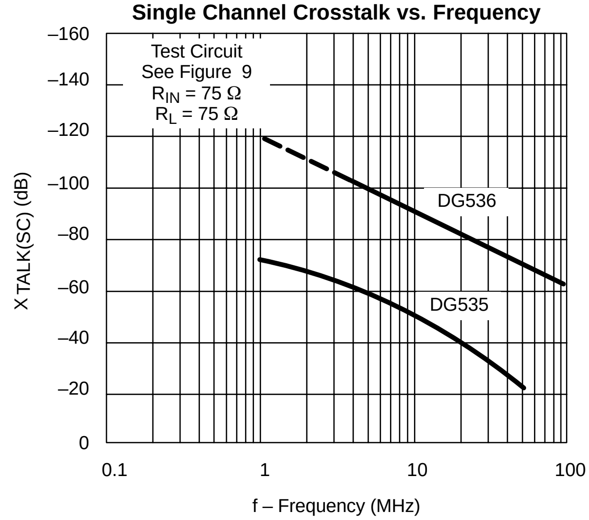

**All Hostile Crosstalk vs. Frequency**




**$t_{ON}$, $t_{OFF}$ and Break-Before-Make vs. Temperature**




**Single Channel Crosstalk vs. Frequency**




## INPUT TIMING REQUIREMENTS

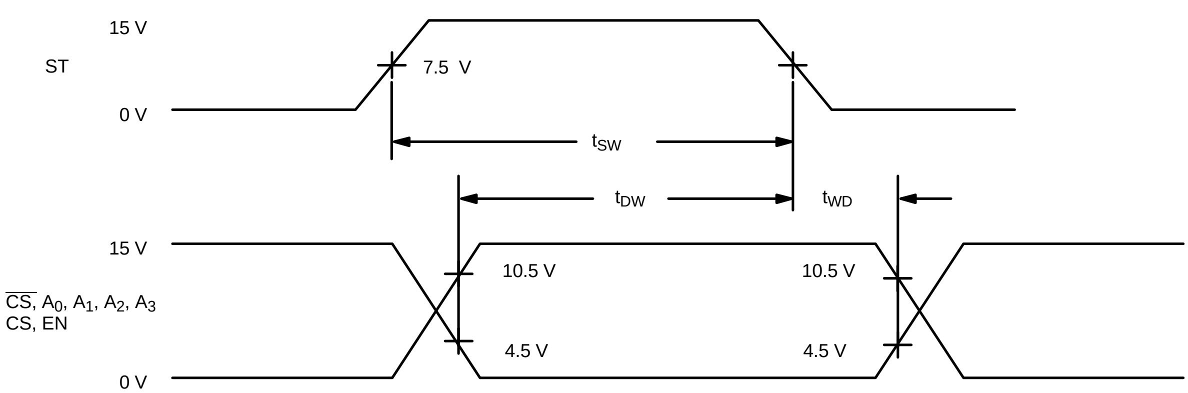



**FIGURE 1.**

## TEST CIRCUITS

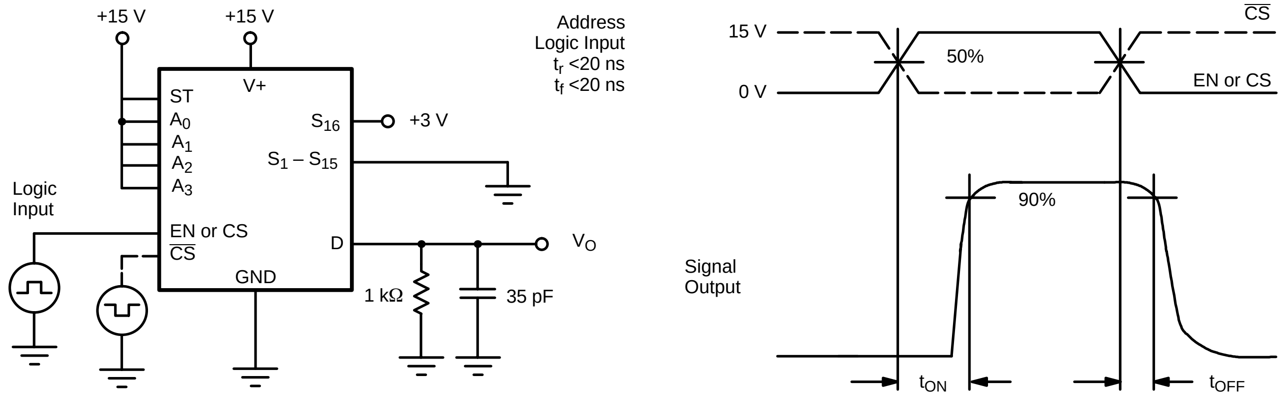



**FIGURE 2.** EN, CS, $\overline{CS}$, Turn On/Off Time

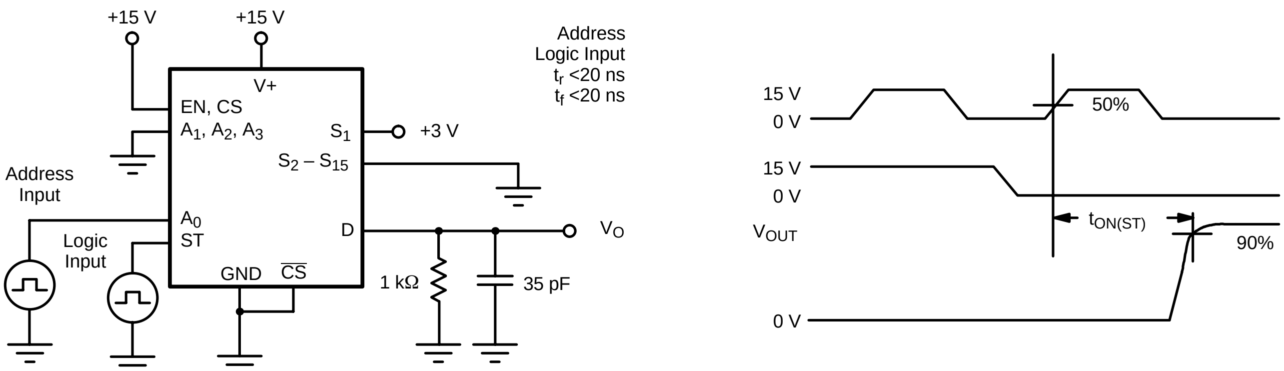



**FIGURE 3.** Strobe ST Turn On Time

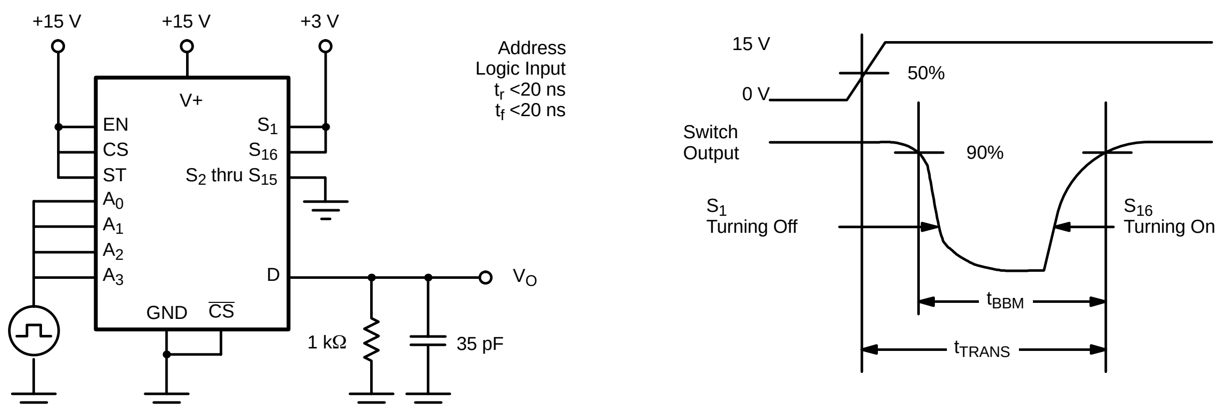
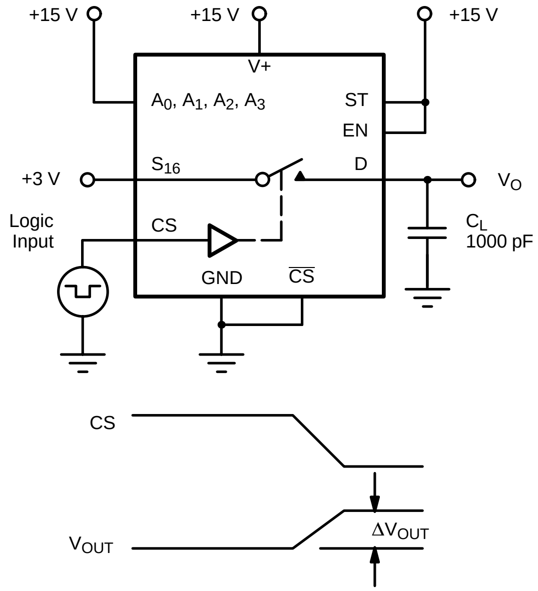



**FIGURE 4.** Transition Time and Break-Before-Make Interval

## TEST CIRCUITS




$\Delta V_{OUT}$ is the measured voltage error due to charge injection.
The charge injection in Coulombs is $Q = C_L \times \Delta V_{OUT}$

**FIGURE 5.** Charge Injection

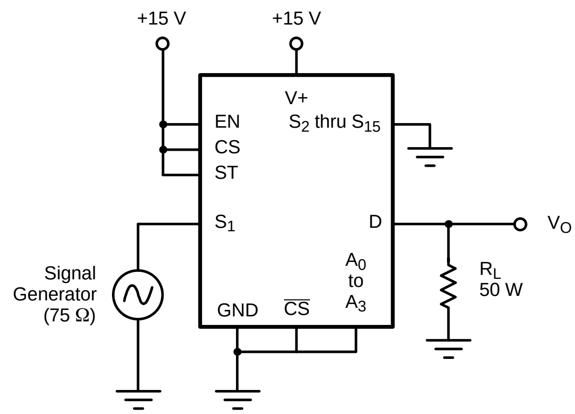



**FIGURE 6.** Bandwidth

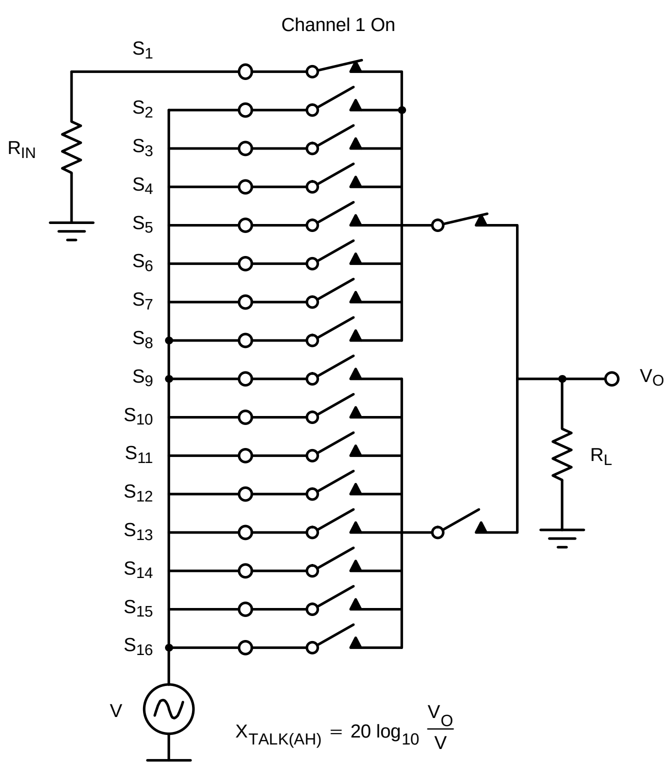



**FIGURE 7.** All Hostile Crosstalk

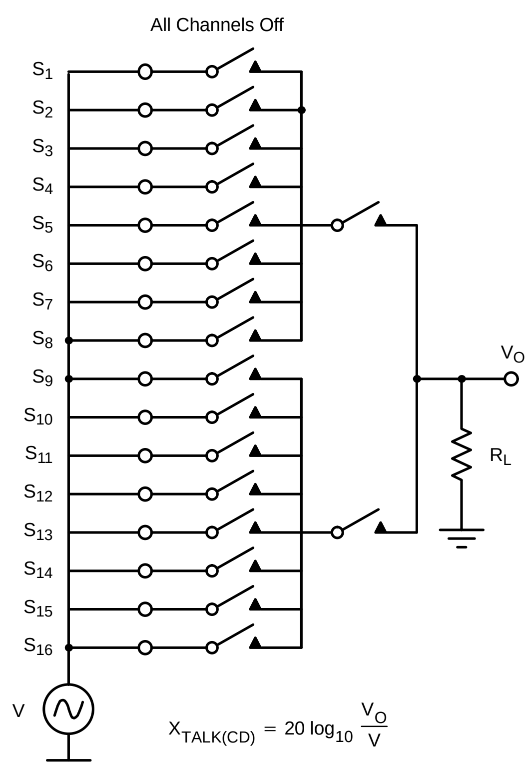



**FIGURE 8.** Chip Disabled Crosstalk



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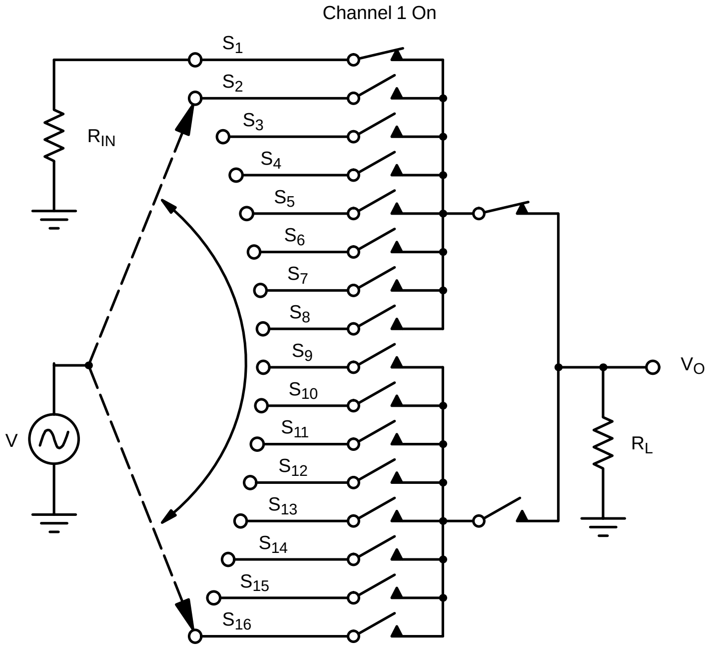
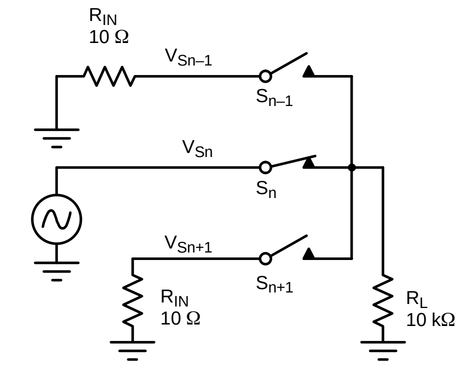
## TEST CIRCUITS




Notes:

1. Any individual channel between $S_2$ and $S_{16}$ can be selected
2. $X_{TALK(SC)} = 20 \log_{10} \frac{V_O}{V}$ is scanned sequentially from $S_2$ to $S_{16}$

**FIGURE 9.** Single Channel Crosstalk




$$X_{TALK(AI)} = 20 \log_{10} \frac{V_{Sn-1}}{V_{Sn}} \text{ or } 20 \log_{10} \frac{V_{Sn+1}}{V_{Sn}}$$

**FIGURE 10.** Adjacent Input Crosstalk

| PIN DESCRIPTION | |
|---|---|
| **Symbol** | **Description** |
| $S_1$ thru $S_{16}$ | Analog inputs/outputs |
| D | Multiplexer output/demultiplexer input |
| DIS | Open drain low impedance to analog ground when any channel is selected |
| $\overline{CS}$, CS, EN | Logic inputs to selected desired multiplexer(s) when using several multiplexers in a system |
| $A_0$ thru $A_3$ | Binary address inputs to determine which channel is selected |
| ST | Strobe input that latches $A_0$, $A_1$, $A_2$, $A_3$, $\overline{CS}$, CS, EN |
| V+ | Positive supply voltage input |
| GND | Analog signal ground and most negative potential<br>**All ground pins should be connected externally to ensure dynamic performance** |

## DETAILED DESCRIPTION

The DG535/536 are 16-channel single-ended multiplexers with on-chip address logic and control latches.

The multiplexer connects one of sixteen inputs ($S_1$, $S_2$ through $S_{16}$) to a common output (D) under the control of a 4-bit binary address ($A_0$ to $A_3$). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of three independent logic inputs (EN, CS and $\overline{CS}$) are provided on chip. These inputs are gated together (see Figure 11) and only when EN = CS = 1 and $\overline{CS}$ = 0 can an output switch be selected. This necessary logic condition is then latched-in when Strobe (ST) goes low.

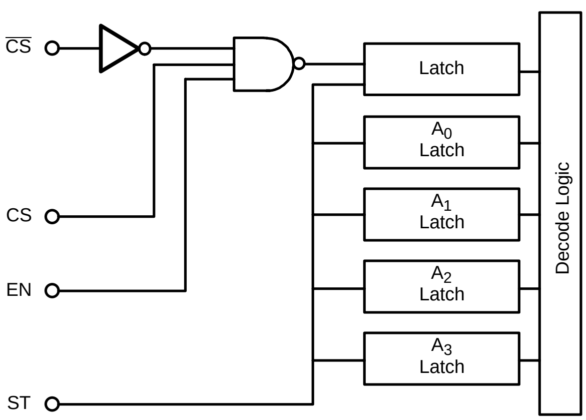



**FIGURE 11.** $\overline{CS}$, CS, EN, ST Control Logic

Break-before-make switching prevents momentary shorting when changing from one input to another.

The devices feature a two-level switch arrangement whereby two banks of eight switches (first level) are connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 12).

With this method $SW_2$ operates out of phase with $SW_1$ and $SW_3$. In the on condition $SW_1$ and $SW_3$ are closed with $SW_2$ open whereas in the off condition $SW_1$ and $SW_3$ are open and $SW_2$ closed. In the off condition the input to $SW_3$ is effectively the isolation leakage of $SW_1$ working into the on-resistance of $SW_2$ (typically 200 Ω).

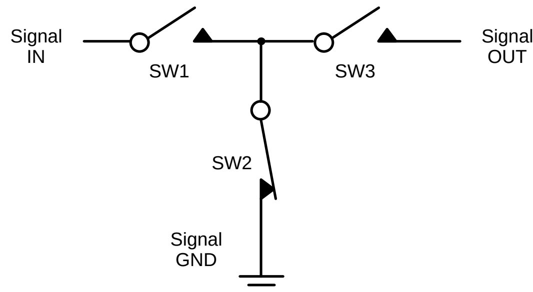



**FIGURE 12.** "T" Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535/536 have extensive applications where any high frequency video or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using n-channel DMOS FETs for the "T" and series switches.

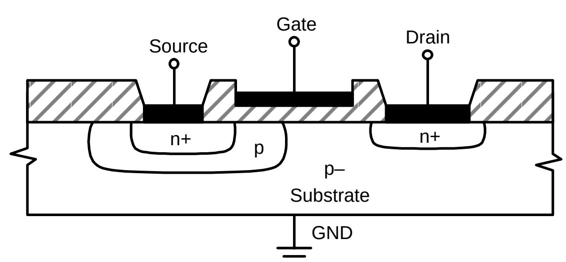



**FIGURE 13.** Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 13 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e., 20 mA).

## DETAILED DESCRIPTION

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS drain terminal (see Figure 13) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown.

The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

### DC Biasing

To avoid negative overvoltage conditions and subsequent distortion of ac analog signals, dc biasing may be necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to ±200 mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 14.

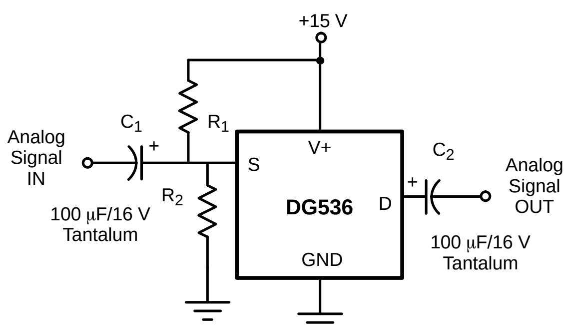



**FIGURE 14.** Simp
le Bias Circuit

$R_1$ and $R_2$ are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor $C_1$ blocks the dc bias voltage from being coupled back to the analog signal source and $C_2$ blocks the dc bias from the output signal. Both $C_1$ and $C_2$ should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies. Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method is to offset the supply voltages (see Figure 15).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

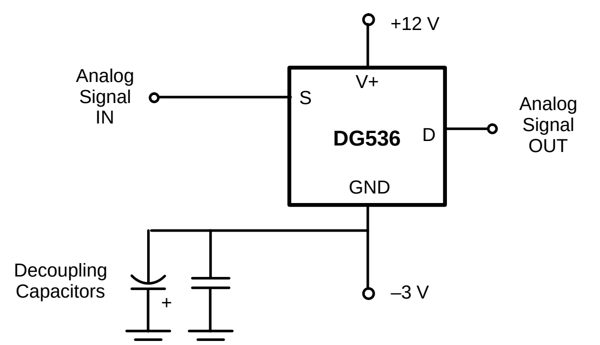



**FIGURE 15.** DG536 with
Offset Supply

TTL to CMOS level shifting is easily obtained by using a MC14504B.

### Circuit Layout

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG536. Stray capacitances on the PC board and/or connecting leads will considerably degrade the ac performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.