

HD6350/HD6850 Series

ACIA (Asynchronous Communications Interface Adapter)

The HD6350/HD6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the HMCS6800 Micro-processing Unit.

The bus interface of the HD6350/HD6850 includes select, enable, read/writer, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface with proper formatting and error checking.

The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided.

FEATURES

- Serial/Parallel Conversion of Data
- Seven and Eight-bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Peripheral/Modem Control Functions (Clear to Send CTS, Request to Send RTS, Data Carrier Detect DCD)
- Optional $\div 1$, $\div 16$, and $\div 64$ Clock Modes
- One-or Two-Stop Bit Operation
- Double Buffered

— HD6350 —

- Low-Power, High-Speed, High-Density CMOS
- Compatible with NMOS ACIA (HD6850)
- Wide Range Operating Voltage ($V_{CC} = 5V \pm 10\%$)
- Up to 1Mbps Transmission

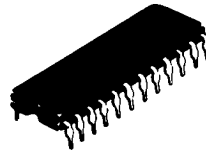
— HD6850 —

- Compatible with MC6850 and MC68A50
- Up to 500Kbps Transmission

■ TYPE OF PRODUCTS

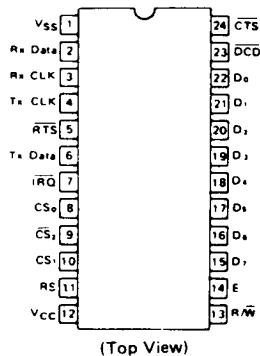
Type	Process	Clock Frequency	Package
HD6350P	CMOS	1.0MHz	DP-24
HD63A50P		1.5MHz	
HD63B50P		2.0MHz	
HD6350FP	CMOS	1.0MHz	FP-24D
HD63A50FP		1.5MHz	
HD63A50FP		2.0MHz	
HD6850	NMOS	1.0MHz	DC-24
HD68A50		1.5MHz	
HD6850P	NMOS	1.0MHz	DP-24
HD68A50P		1.5MHz	

HD6350P, HD6850P



(DP-24)

■ PIN ARRANGEMENT



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Only Function and summary are introduced regarding to this products. Please refer to the user's manual in details.

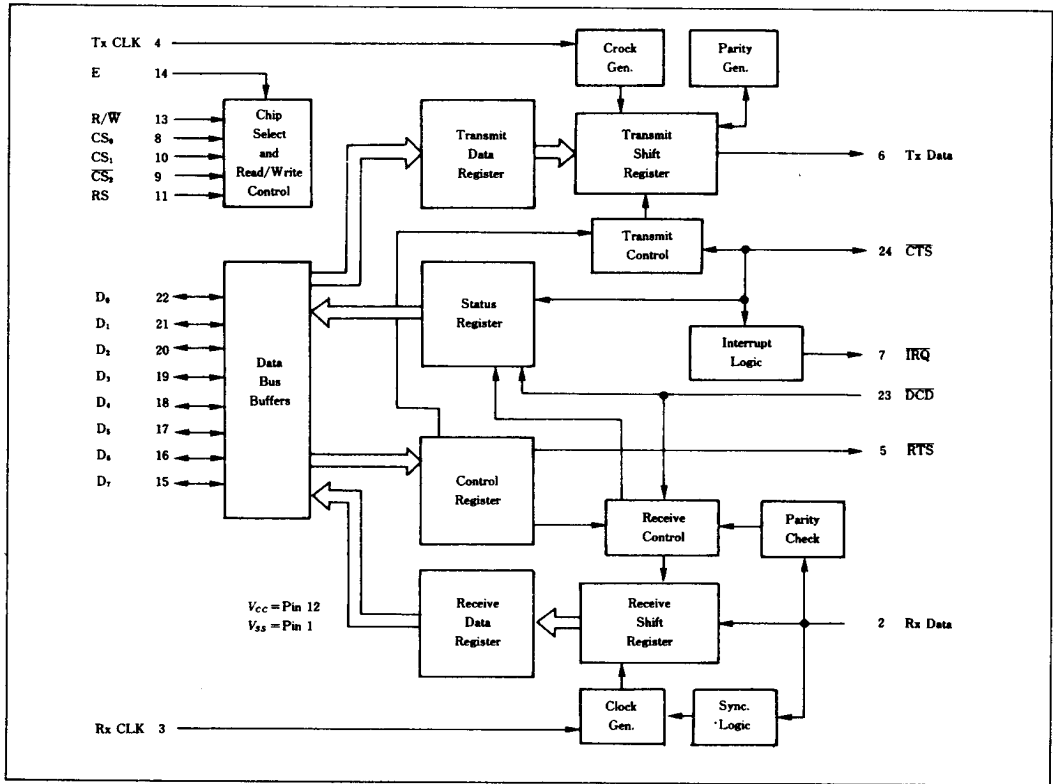
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■ BLOCK DIAGRAM



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