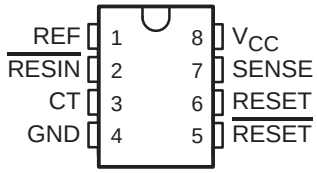
SLVS028F – APRIL 1983 – REVISED NOVEMBER 2000

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Wide Supply-Voltage Range**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

D OR P PACKAGE
(TOP VIEW)



description

The TL77xxA family of integrated-circuit supply-voltage supervisors is specifically designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

During power down and when SENSE is below V_{IT-}, the outputs remain active until V_{CC} falls below 2 V. After this, the outputs are undefined.

An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL77xxAC series is characterized for operation from 0°C to 70°C. The TL77xxAI series is characterized for operation from –40°C to 85°C.

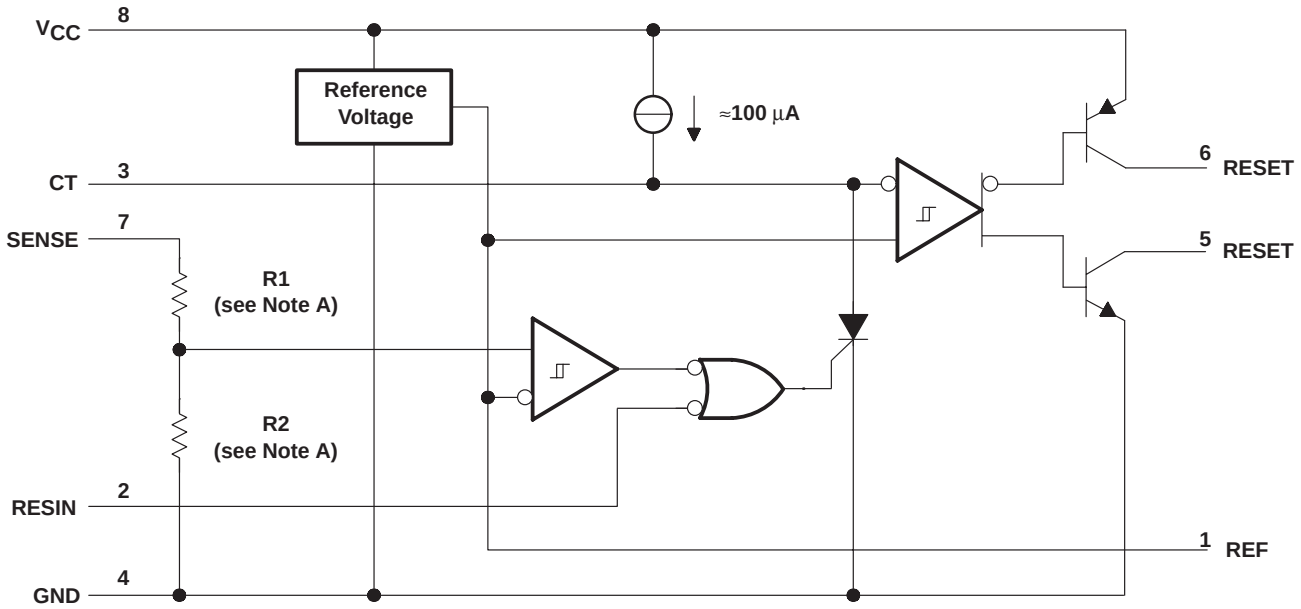
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TL7702ACD TL7705ACD TL7709ACD TL7712ACD TL7715ACD	TL7702ACP TL7705ACP TL7709ACP TL7712ACP TL7715ACP
–40°C to 85°C	TL7702AID TL7705AID TL7709AID TL7712AID TL7715AID	TL7702AIP TL7705AIP TL7709AIP TL7712AIP TL7715AIP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL7702ACDR).

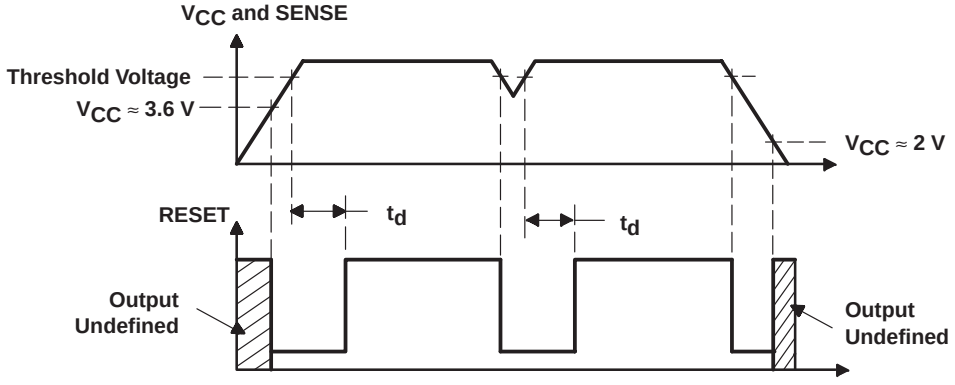
functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



NOTES: A. TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ
B. Resistor values shown are nominal.

timing diagram



TL7702A, TL7705A, TL7709A, TL7712A, TL7715A
SUPPLY-VOLTAGE SUPERVISORS

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MIN

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA	V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A	T_A = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_{hys}	Hysteresis, SENSE ($V_{IT+} – V_{IT-}$)	TL7702A	T_A = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 2.4 V to V_{CC}			20	µA
			V_I = 0.4 V			–100	
		SENSE TL7702A	$V_{ref} < V_I < V_{CC} – 1.5$ V		0.5	2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0			–50	µA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

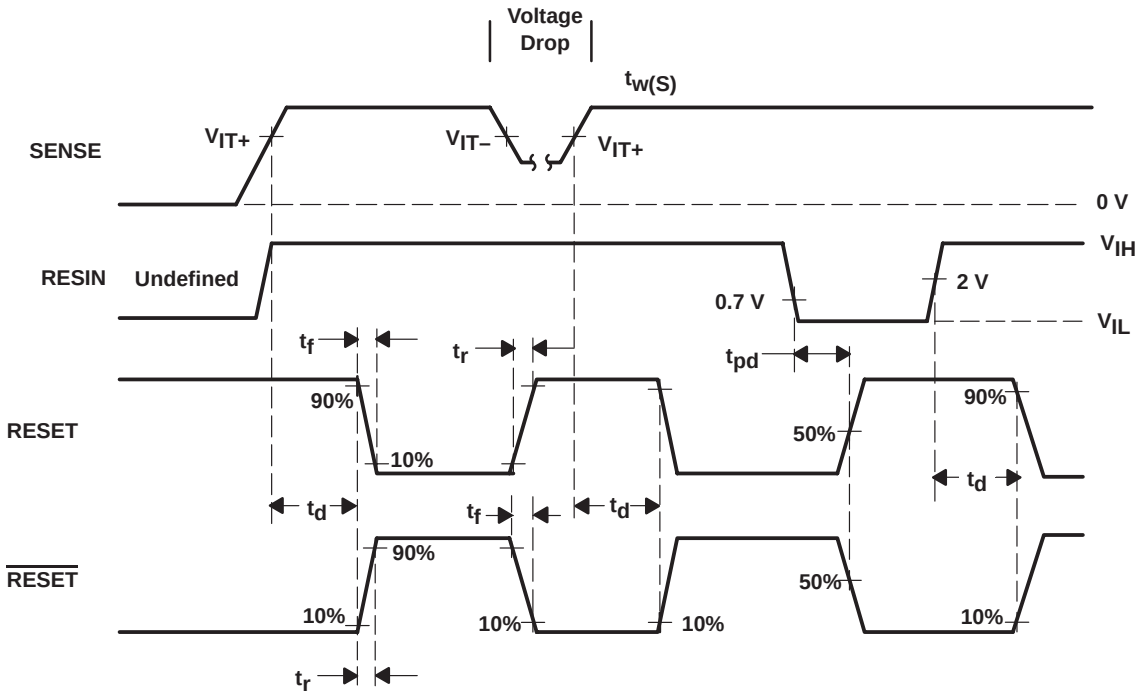
† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡		TL77xxAC TL77xxAI			UNIT
					MIN	TYP	MAX	
	Output pulse duration		C_T = 0.1 µF		0.65	1.2	2.6	msec
	Input pulse duration at $\overline{\text{RESIN}}$				0.4			µs
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs		$V_{IH} = V_{IT-}$ +200 mV,	$V_{IL} = V_{IT-}$ –200 mV	2			µs
t_{pd}	Propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$		V_{CC} = 5 V				1	µs
t_r	Rise time	RESET	V_{CC} = 5 V,	See Note 5			0.2	µs
		$\overline{\text{RESET}}$					3.5	
t_f	Fall time	RESET	V_{CC} = 5 V,	See Note 5			3.5	µs
		$\overline{\text{RESET}}$					0.2	

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.
NOTE 5: The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS†

ASSERTION TIME vs LOAD RESISTANCE

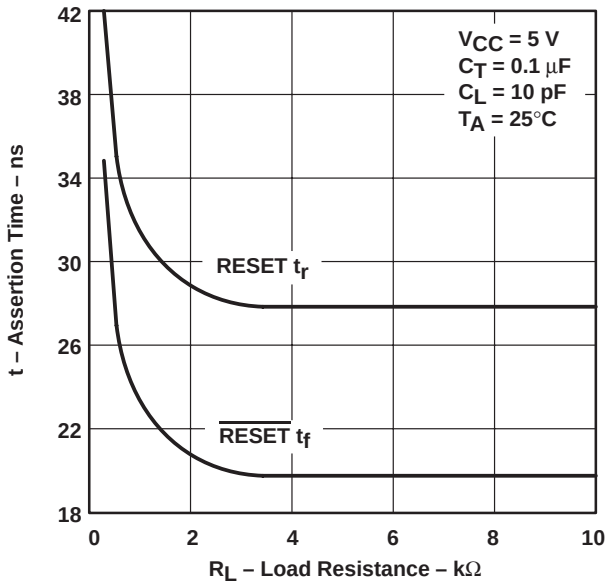


Figure 2

DEASSERTION TIME vs LOAD RESISTANCE

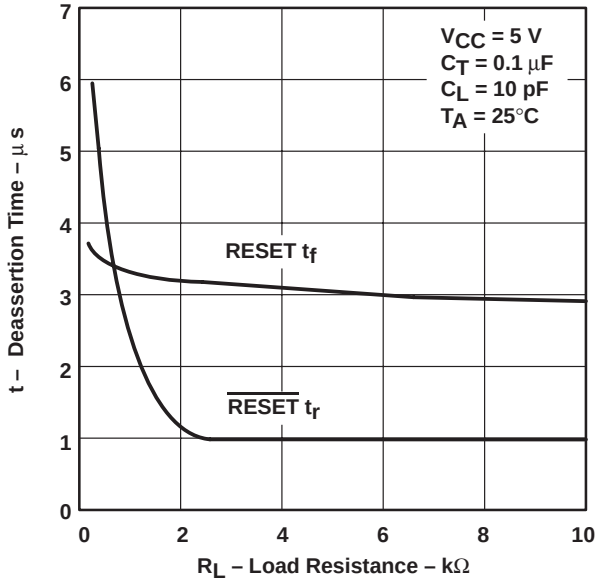


Figure 3

ASSERTION TIME vs LOAD CAPACITANCE

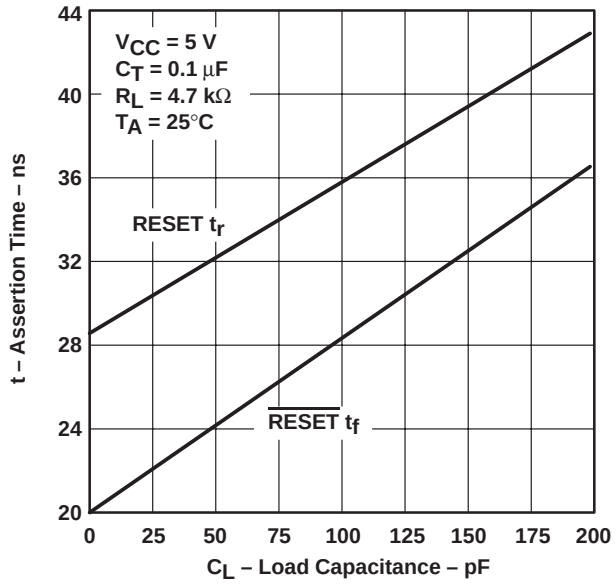


Figure 4

DEASSERTION TIME vs LOAD CAPACITANCE

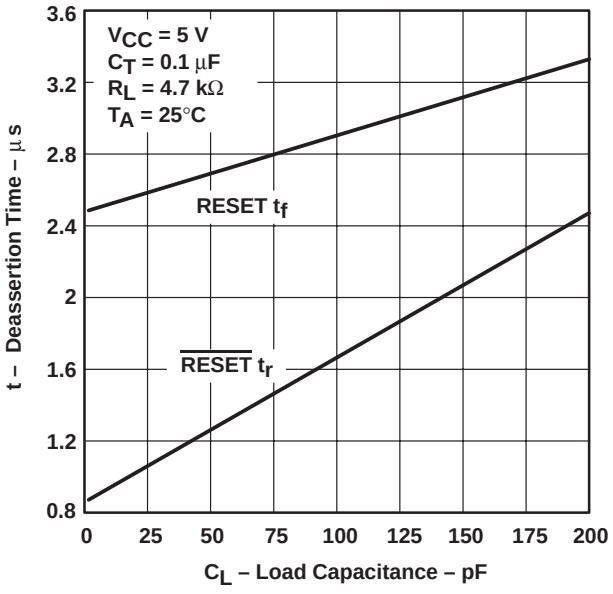


Figure 5

† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

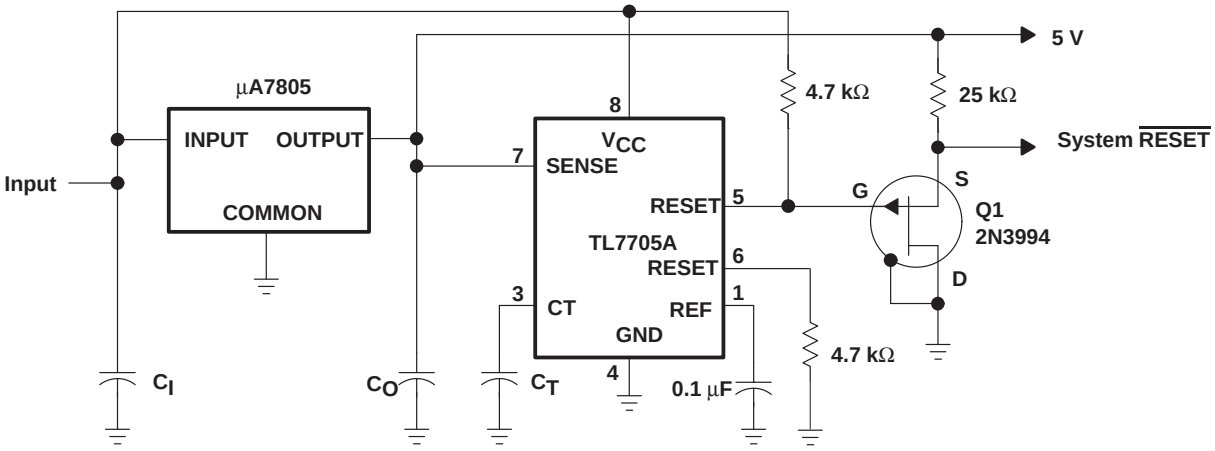


Figure 8. Eliminating Undefined States Using a P-Channel JFET

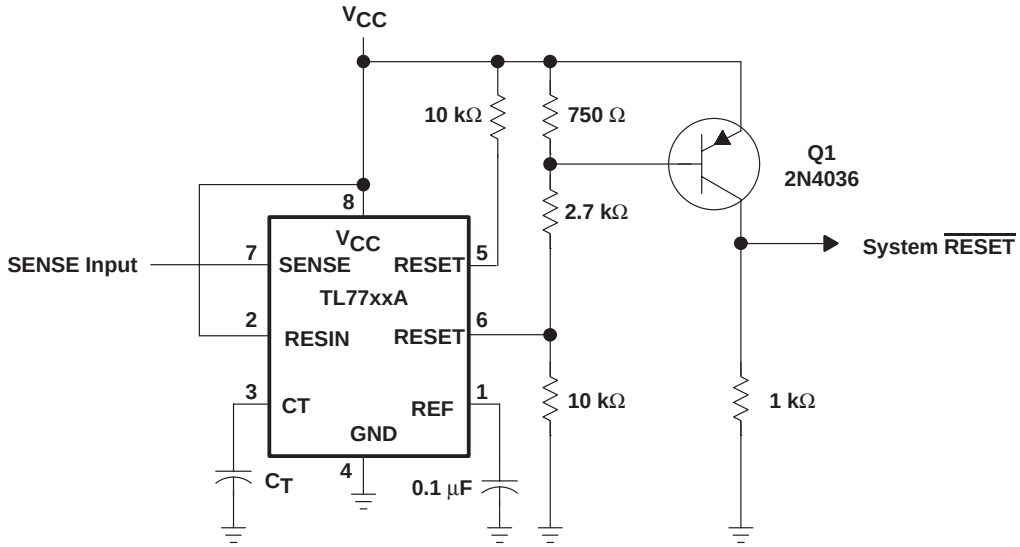


Figure 9. Eliminating Undefined States Using a pnp Transistor

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