- **High-Performance Fixed-Point Digital Signal Processor (DSP) – TMS320C6204**
  - **5-ns Instruction Cycle Time**
  - **200-MHz Clock Rate**
  - **Eight 32-Bit Instructions/Cycle**
  - **1600 MIPS**
- **C6204 GLW Ball Grid Array (BGA) Package is Pin-Compatible With the C6202/02B/03 GLS BGA Package†**
- **VelociTI™ Advanced Very-Long-Instruction-Word (VLIW) TMS320C62x™ DSP Core**
  - **Eight Highly Independent Functional Units:**
    - **Six ALUs (32-/40-Bit)**
    - **Two 16-Bit Multipliers (32-Bit Result)**
  - **Load-Store Architecture With 32 32-Bit General-Purpose Registers**
  - **Instruction Packing Reduces Code Size**
  - **All Instructions Conditional**
- **Instruction Set Features**
  - **Byte-Addressable (8-, 16-, 32-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Saturation**
  - **Bit-Field Extract, Set, Clear**
  - **Bit-Counting**
  - **Normalization**
- **1M-Bit On-Chip SRAM**
  - **512K-Bit Internal Program/Cache (16K 32-Bit Instructions)**
  - **512K-Bit Dual-Access Internal Data (64K Bytes)**
    - **Organized as Two 32K-Byte Blocks for Improved Concurrency**
- **32-Bit External Memory Interface (EMIF)**
  - **Glueless Interface to Synchronous Memories: SDRAM or SBSRAM**
  - **Glueless Interface to Asynchronous Memories: SRAM and EPROM**
  - **52M-Byte Addressable External Memory Space**
- **Four-Channel Bootloading Direct-Memory-Access (DMA) Controller With an Auxiliary Channel**
- **32-Bit Expansion Bus (XB)**
  - **Glueless/Low-Glue Interface to Popular PCI Bridge Chips**
  - **Glueless/Low-Glue Interface to Popular Synchronous or Asynchronous Microprocessor Buses**
  - **Master/Slave Functionality**
  - **Glueless Interface to Synchronous FIFOs and Asynchronous Peripherals**
- **Two Multichannel Buffered Serial Ports (McBSPs)**
  - **Direct Interface to T1/E1, MVIP, SCSA Framers**
  - **ST-Bus-Switching Compatible**
  - **Up to 256 Channels Each**
  - **AC97-Compatible**
  - **Serial-Peripheral Interface (SPI) Compatible (Motorola™)**
- **Two 32-Bit General-Purpose Timers**
- **Flexible Phase-Locked-Loop (PLL) Clock Generator**
- **IEEE-1149.1 (JTAG‡) Boundary-Scan-Compatible**
- **288-Pin MicroStar BGA™ Package (GHK)**
- **340-Pin BGA Package (GLW)**
- **0.15-μm/5-Level Metal Process**
  - **CMOS Technology**
- **3.3-V I/Os, 1.5-V Internal**

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† For more details, see the GLW BGA package bottom view.
‡ IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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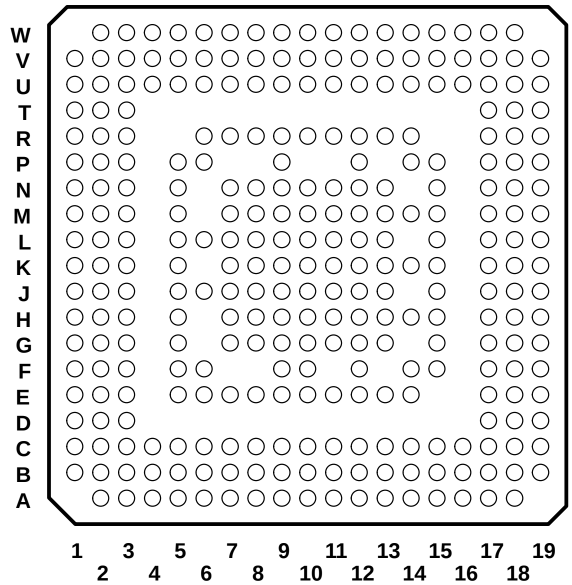
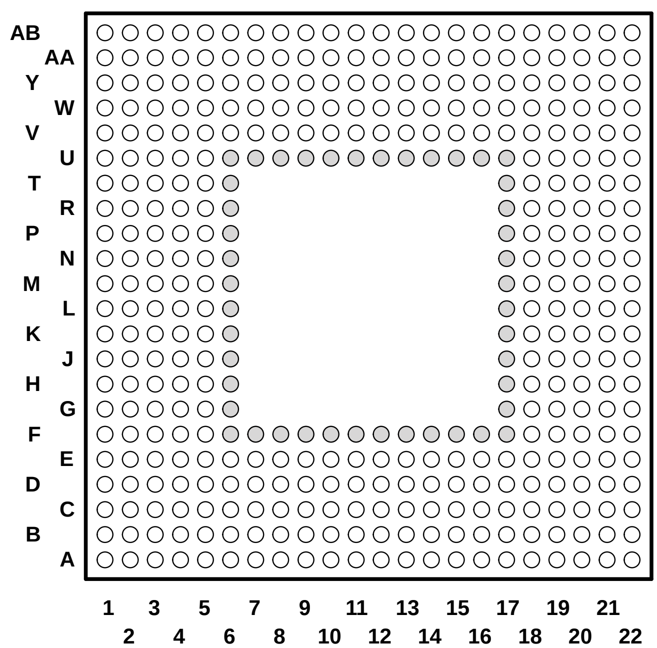
GHK and GLW BGA packages (bottom view)

GHK 288-PIN BALL GRID ARRAY (BGA) PACKAGE (BOTTOM VIEW)



GLW 340-PIN BGA PACKAGE (BOTTOM VIEW)



The C6204 GLW BGA package is pin-compatible with the C6202/02B/03 GLS package except that the inner row of balls (which are additional power and ground pins) are removed for the C6204 GLW package.

○ **These balls are *NOT* applicable for the C6204 devices 340-pin GLW BGA package.**

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description

The TMS320C62x™ DSPs (including the TMS320C6204 device) compose the fixed-point DSP generation in the TMS320C6000™ DSP platform. The TMS320C6204 (C6204) device is based on the high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making the C6204 an excellent choice for multichannel and multifunction applications.

With performance of up to 1600 million instructions per second (MIPS) at a clock rate of 200 MHz, the C6204 offers cost-effective solutions to high-performance DSP-programming challenges. The C6204 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide six arithmetic logic units (ALUs) for a high degree of parallelism and two 16-bit multipliers for a 32-bit result. The C6204 can produce two multiply-accumulates (MACs) per cycle for a total of 400 million MACs per second (MMACS). The C6204 DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals.

The C6204 includes a large bank of on-chip memory and has a powerful and diverse set of peripherals. Program memory consists of a 64K-byte block that is user-configurable as cache or memory-mapped as program space. Data memory consists of two 32K-byte blocks of RAM. The peripheral set includes two multichannel buffered serial ports (McBSPs), two general-purpose timers, a 32-bit expansion bus (XB) that offers ease of interface to synchronous or asynchronous industry-standard host bus protocols, and a glueless 32-bit external memory interface (EMIF) capable of interfacing to SDRAM or SBSRAM and asynchronous peripherals.

The C6204 has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

device characteristics

Table 1 provides an overview of the TMS320C6204, TMS320C6202/02B, and the TMS320C6203 pin-compatible C62x™ DSPs. The table shows significant features of each device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count, etc. This data sheet primarily focuses on the functionality of the TMS320C6204 device although it also identifies to the user the pin-compatibility of the 6204 GLW and the C6202/02B and C6203 GLS BGA packages. For the functionality information on the TMS320C6202/02B devices, see the *TMS320C6202, TMS320C6202B Fixed-Point Digital Signal Processors* data sheet (literature number SPRS104). For the functionality information on the TMS320C6203 device, see the *TMS320C6203 Fixed-Point Digital Signal Processor* data sheet (literature number SPRS086). And for more details on the C6000™ DSP device part numbers and part numbering, see Table 3 and Figure 4.

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device characteristics (continued)

Table 1. Characteristics of the Pin-Compatible TMS320C6204 and C6202/02B/03 DSPs

HARDWARE FEATURES		C6204	C6202	C6202B	C6203
Peripherals	EMIF	√	√	√	√
	DMA	4-Channel With Throughput Enhancements	4-Channel	4-Channel With Throughput Enhancements	4-Channel With Throughput Enhancements
	Expansion Bus	√	√	√	√
	McBSPs	2	3	3	3
	32-Bit Timers	2	2	2	2
Internal Program Memory	Size (Bytes)	64K	256K	256K	384K
	Organization	1 Block: 64K-Byte Cache/Mapped Program	Block 0: 128K-Byte Mapped Program Block 1: 128K-Byte Cache/Mapped Program	Block 0: 128K-Byte Mapped Program Block 1: 128K-Byte Cache/Mapped Program	Block 0: 256K-Byte Mapped Program Block 1: 128K-Byte Cache/Mapped Program
Internal Data Memory	Size (Bytes)	64K	128K	128K	512K
	Organization	2 Blocks: Four 16-Bit Banks per Block 50/50 Split	2 Blocks: Four 16-Bit Banks per Block 50/50 Split	2 Blocks: Four 16-Bit Banks per Block 50/50 Split	2 Blocks: Four 16-Bit Banks per Block 50/50 Split
CPU ID + Rev ID	Control Status Register (CSR.[31:16])	0x0003	0x0002	0x0003	0x0003
Frequency	MHz	200	200, 250	250	250, 300
Cycle Time	ns	5 ns (C6204-200)	4 ns (C6202-250) 5 ns (C6202-200)	4 ns (C6202B-250)	3.33 ns (C6203-300) 4 ns (C6203-250)
Voltage	Core (V)	1.5	1.8	1.5	1.5
	I/O (V)	3.3	3.3	3.3	3.3
PLL Options	CLKIN frequency multiplier [Bypass (x1), x4, x6, x7, x8, x9, x10, and x11]	x1, x4 (Both Pkgs)	x1, x4 (Both Pkgs)	x1, x4, x8, x10 (GJL Pkg) All PLL Options (GLS Pkg)	x1, x4, x8, x10 (GJL Pkg) All PLL Options (GLS Pkg)
BGA Packages	27 x 27 mm	–	352-pin GJL	352-pin GJL	352-pin GJL
	18 x 18 mm	340-pin GLW	384-pin GLS	384-pin GLS	384-pin GLS
	16 x 16 mm	288-pin GHK	–	–	–
Process Technology	μm	0.15 μm	0.18 μm	0.15 μm	0.15 μm
Product Status	Product Preview (PP) Advance Information (AI) Production Data (PD)	AI (GLW) PD (GHK)	PD	PP	PD

ADVANCE INFORMATION

C62x™ device compatibility

The TMS320C6202, C6202B, C6203, and C6204 devices are pin-compatible; thus, making new system designs easier and providing faster time to market. The following list summarizes the C62x™ DSP device characteristic differences:

- Core Supply Voltage (1.8 V versus 1.5 V)

  The C6202 device core supply voltage is 1.8 V while the C6202B, C6203, C6204 devices have core supply voltages of 1.5 V.

- PLL Options Availability

  Table 1 identifies the available PLL multiply factors [e.g., CLKIN x1 (PLL bypassed), x4, etc.] for each of the C62x™ DSP devices. For additional details on the PLL clock module and specific options for the C6204 device, see the *Clock PLL* section of this data sheet.

  For additional details on the PLL clock module and specific options for the C6202/02B/03 devices, see the *Clock PLL* sections of the *TMS320C6202, TMS320C6202B Fixed-Point Digital Signal Processors* data sheet (literature number SPRS104) and the *TMS320C6203 Fixed-Point Digital Signal Processor* data sheet (literature number SPRS086).

- On-Chip Memory Size

  The C6202/02B, C6203, and C6204 devices have different on-chip program memory and data memory sizes (see Table 1).

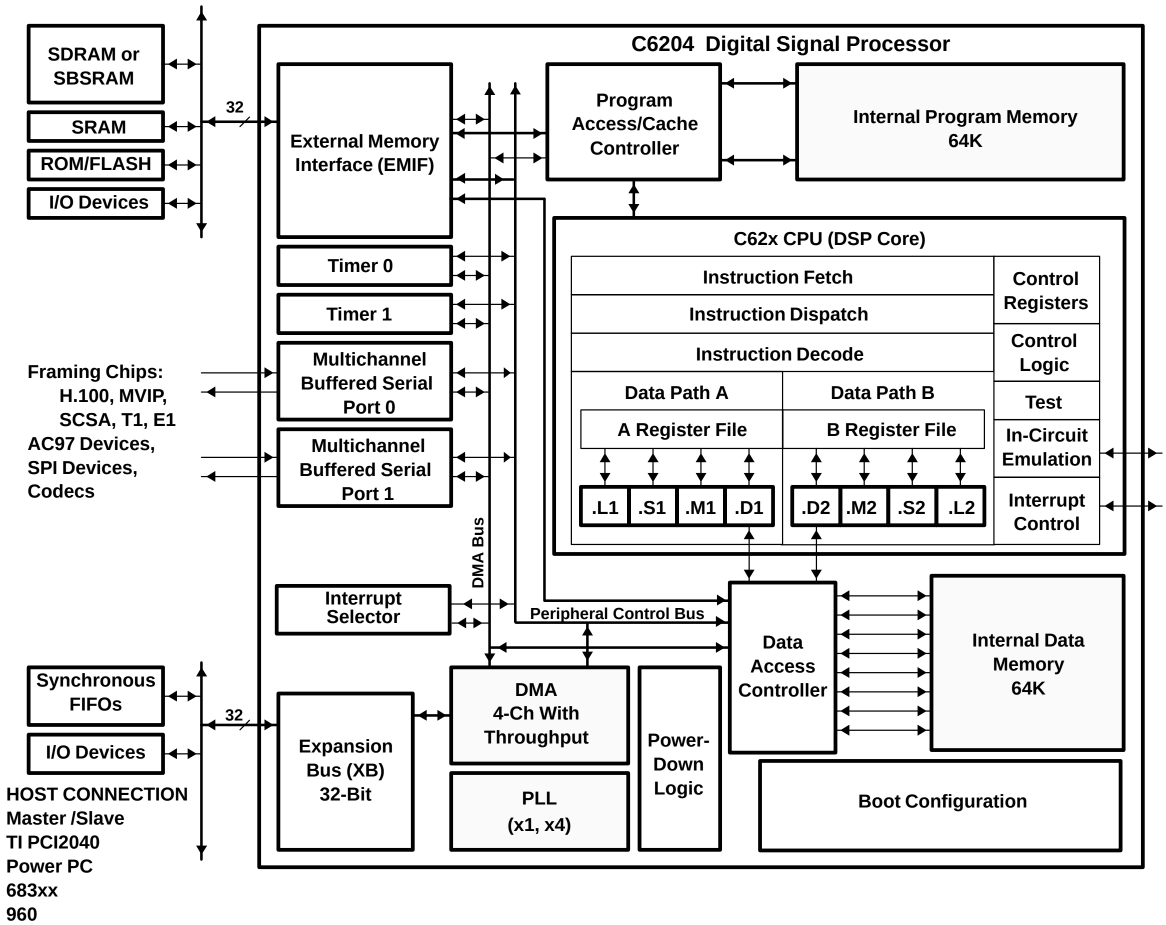
- McBSPs

  The C6204 device has two McBSPs on-chip while the C6202, C6202B, C6203 devices have three McBSPs on-chip.

For a more detailed discussion on migration concerns, and similarities/differences between the C6202, C6202B, C6203, and C6204 devices, see the *How to Begin Development and Migrate Across the TMS320C6202/6202B/6203/6204 DSPs* application report (literature number SPRA603).

ADVANCE INFORMATION

functional and CPU (DSP core) block diagram



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CPU (DSP core) description

The CPU fetches VelociTI™ advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VelociTI™ VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C62x CPU from other VLIW architectures.

The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 16 32-bit registers for a total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU [see the functional and CPU (DSP core) block diagram and Figure 1]. The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

Another key feature of the C62x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C62x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically "true"). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are "linked" together by "1" bits in the least significant bit (LSB) position of the instructions. The instructions that are "chained" together for simultaneous execution (up to eight in total) compose an execute packet. A "0" in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the 256-bit-wide fetch-packet boundary, the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte-, half-word, or word-addressable.

CPU (DSP core) description (continued)

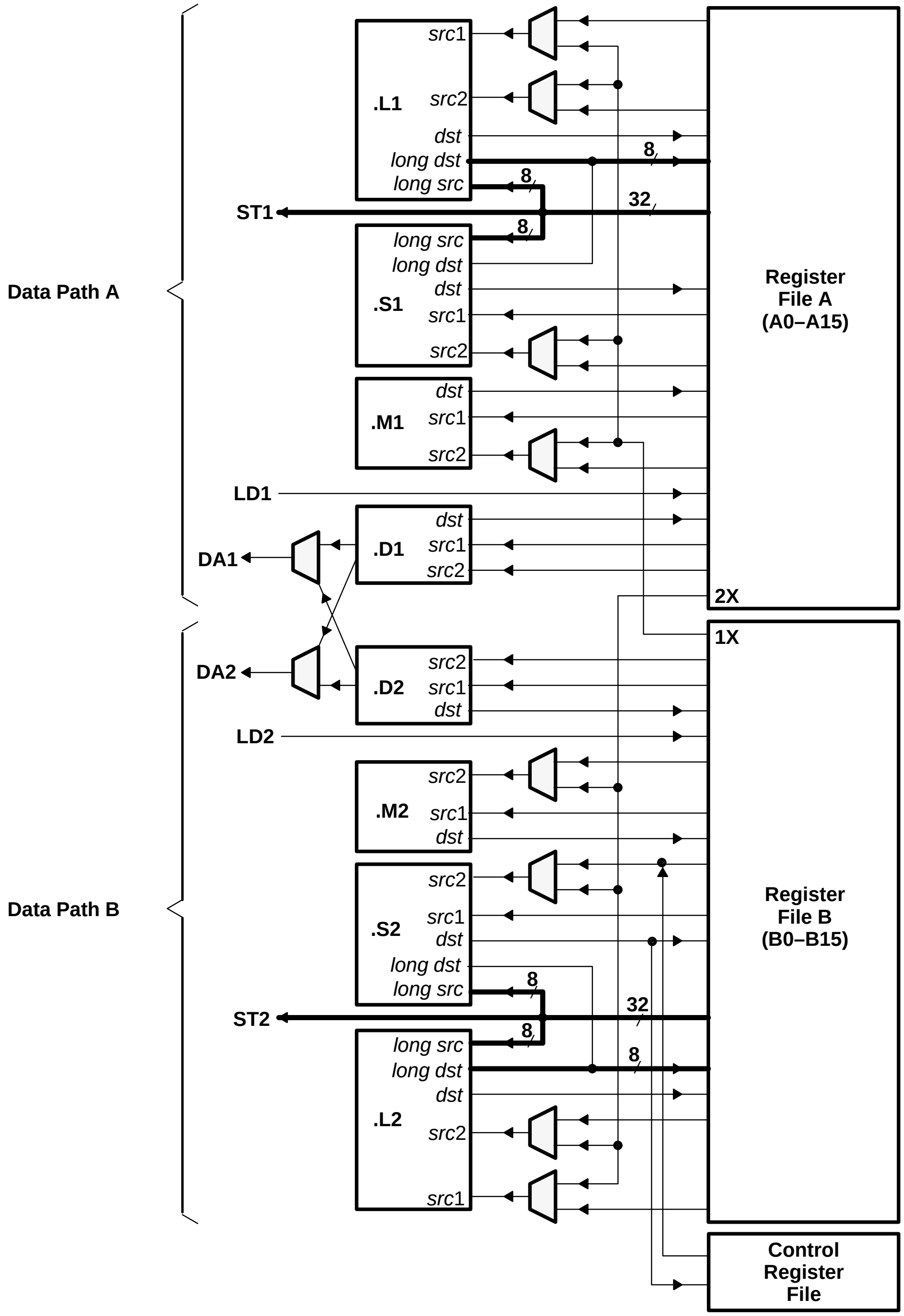

Figure 1. TMS320C62x CPU (DSP Core) Data Paths

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memory map summary

Table 2 shows the memory map address ranges of the C6204 device. The C6204 device has the capability of a MAP 0 or MAP 1 memory block configuration. The maps differ in that MAP 0 has *external memory* mapped at address 0x0000 0000 and MAP 1 has *internal memory* mapped at address 0x0000 0000. These memory block configurations are set up at reset by the boot configuration pins (generically called BOOTMODE[4:0]). For the C6204 device, the BOOTMODE configuration is handled, at reset, by the expansion bus module (specifically XD[4:0] pins). For more detailed information on the C6204 device settings, which include the device boot mode configuration at reset and other device-specific configurations, see the Boot Configuration section and the Boot Configuration Summary table of the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

Table 2. TMS320C6204 Memory Map Summary

MEMORY BLOCK DESCRIPTION		BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
MAP 0	MAP 1		
External Memory Interface (EMIF) CE0	Internal Program RAM	64K	0000 0000 – 0000 FFFF
EMIF CE0	Reserved	4M – 64K	0001 0000 – 003F FFFF
EMIF CE0	EMIF CE0	12M	0040 0000 – 00FF FFFF
EMIF CE1	EMIF CE0	4M	0100 0000 – 013F FFFF
Internal Program RAM	EMIF CE1	64K	0140 0000 – 0140 FFFF
Reserved	EMIF CE1	4M – 64K	0141 0000 – 017F FFFF
EMIF Registers		256K	0180 0000 – 0183 FFFF
DMA Controller Registers		256K	0184 0000 – 0187 FFFF
Expansion Bus (XBus) Registers		256K	0188 0000 – 018B FFFF
McBSP 0 Registers		256K	018C 0000 – 018F FFFF
McBSP 1 Registers		256K	0190 0000 – 0193 FFFF
Timer 0 Registers		256K	0194 0000 – 0197 FFFF
Timer 1 Registers		256K	0198 0000 – 019B FFFF
Interrupt Selector Registers		256K	019C 0000 – 019F FFFF
Reserved		6M	01A0 0000 – 01FF FFFF
EMIF CE2		16M	0200 0000 – 02FF FFFF
EMIF CE3		16M	0300 0000 – 03FF FFFF
Reserved		1G – 64M	0400 0000 – 3FFF FFFF
XBus XCE0		256M	4000 0000 – 4FFF FFFF
XBus XCE1		256M	5000 0000 – 5FFF FFFF
XBus XCE2		256M	6000 0000 – 6FFF FFFF
XBus XCE3		256M	7000 0000 – 7FFF FFFF
Internal Data RAM		64K	8000 0000 – 8000 FFFF
Reserved		2G – 64K	8001 0000 – FFFF FFFF

signal groups description

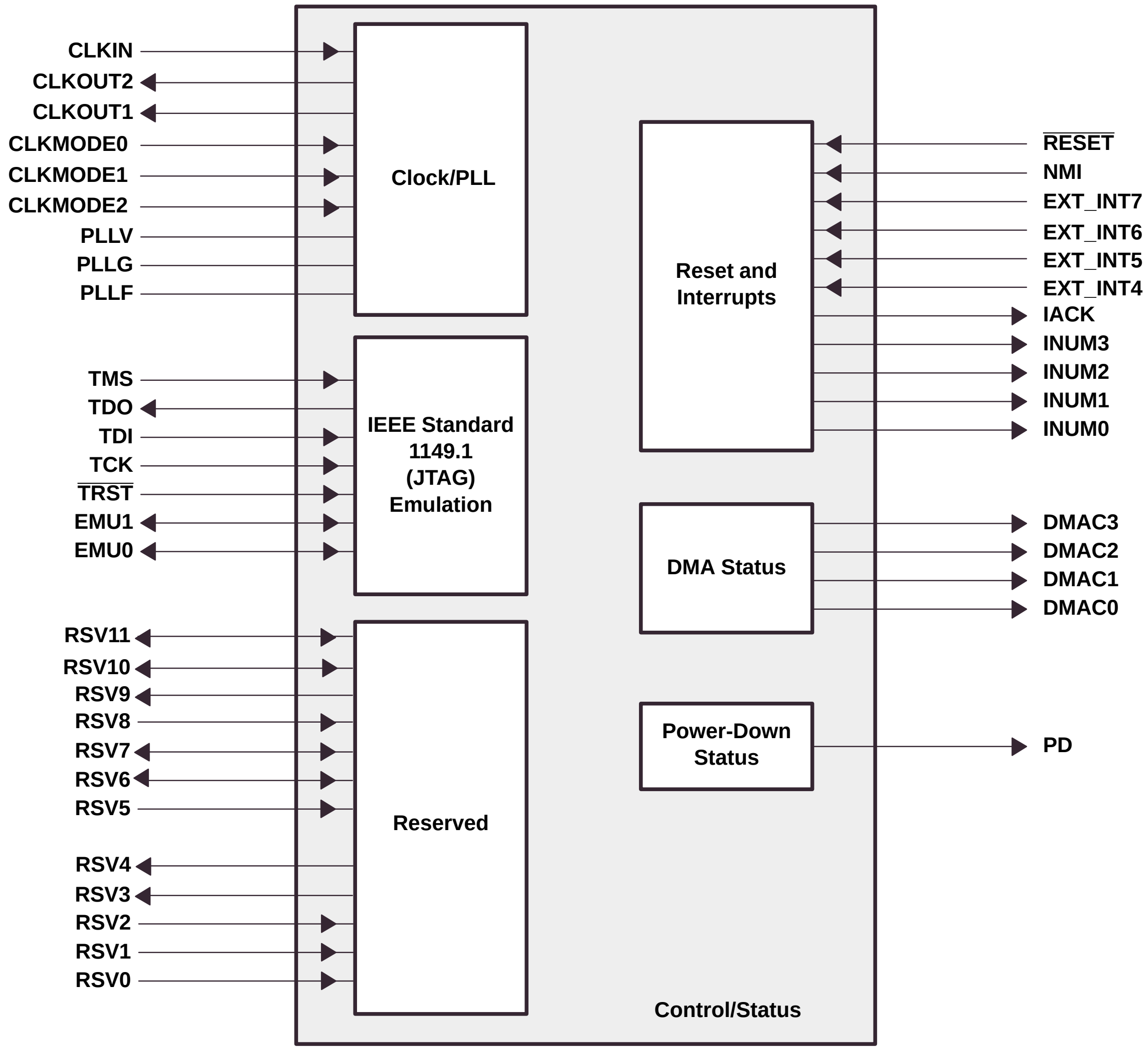

Figure 2. CPU (DSP Core) Signals

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signal groups description (continued)

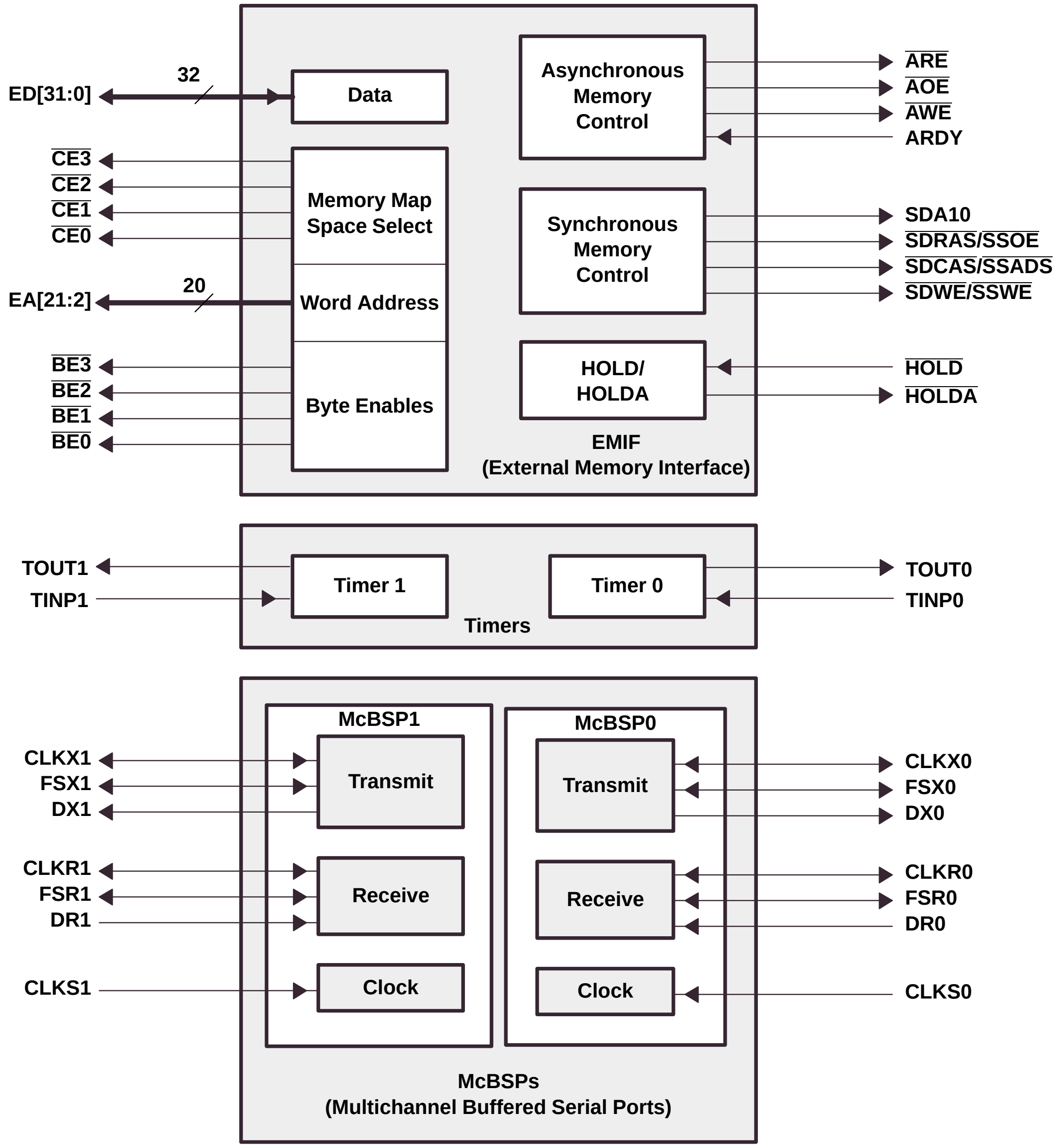

Figure 3. Peripheral Signals

signal groups description (continued)

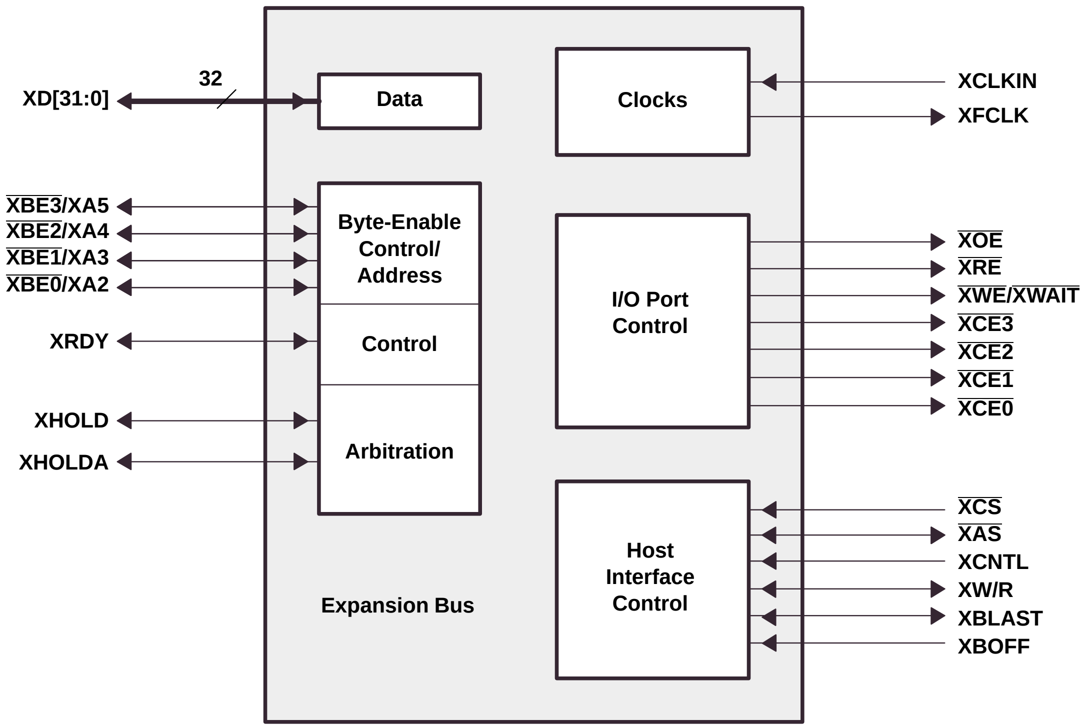

Figure 3. Peripheral Signals (Continued)

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Signal Descriptions

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
CLOCK/PLL				
CLKIN	J3	B10	I	Clock Input
CLKOUT1	T18	Y18	O	Clock output at full device speed
CLKOUT2	T19	AB19	O	Clock output at half of device speed • Used for synchronous memory interface
CLKMODE0	L3	B12	I	Clock mode selects • Selects what multiply factors of the input clock frequency the CPU frequency equals. For more details on CLKMODE pins and the PLL multiply factors, see the *Clock PLL* section of this data sheet. Note: For the C6204 GLW package, the CLKMODE2 (A14) and CLKMODE1 (A9) pins are internally unconnected.
CLKMODE1	–	A9	I	
CLKMODE2	–	A14	I	
PLLV§	K5	C11	A¶	PLL analog V_{CC} connection for the low-pass filter
PLLG§	L2	C12	A¶	PLL analog GND connection for the low-pass filter
PLLF§	L1	A11	A¶	PLL low-pass filter connection to external components and a bypass capacitor
JTAG EMULATION				
TMS	E17	Y5	I	JTAG test-port mode select (features an internal pullup)
TDO	D19	AA4	O/Z	JTAG test-port data out
TDI	D18	Y4	I	JTAG test-port data in (features an internal pullup)
TCK	D17	AB2	I	JTAG test-port clock
$\overline{\text{TRST}}$	C19	AA3	I	JTAG test-port reset (features an internal pulldown)
EMU1	E18	AA5	I/O/Z	Emulation pin 1, pullup with a dedicated 20-kΩ resistor#
EMU0	F15	AB4	I/O/Z	Emulation pin 0, pullup with a dedicated 20-kΩ resistor#
RESET AND INTERRUPTS				
$\overline{\text{RESET}}$	E8	J3	I	Device reset
NMI	A8	K2	I	Nonmaskable interrupt • Edge-driven (rising edge)
EXT_INT7	B15	U2	I	External interrupts • Edge-driven • Polarity independently selected via the external interrupt polarity register bits (EXTPOL.[3:0])
EXT_INT6	C15	U3		
EXT_INT5	A16	W1		
EXT_INT4	B16	V2		
IACK	A15	V1	O	Interrupt acknowledge for all active interrupts serviced by the CPU
INUM3	F12	R3	O	Active interrupt identification number • Valid during IACK for all active interrupts (not just external) • Encoding order follows the interrupt-service fetch-packet ordering
INUM2	A14	T1		
INUM1	B14	T2		
INUM0	C14	T3		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground
§ PLLV, PLLG, and PLLF are not part of external voltage supply or ground. See the *clock PLL* section for information on how to connect these pins.
¶ A = Analog Signal (PLL Filter)
# For emulation and normal operation, pull up EMU1 and EMU0 with a dedicated 20-kΩ resistor. For boundary scan, pull down EMU1 and EMU0 with a dedicated 20-kΩ resistor.

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
POWER-DOWN STATUS				
PD	B18	Y2	O	Power-down modes 2 or 3 (active if high)
EXPANSION BUS				
XCLKIN	H5	C8	I	Expansion bus synchronous host interface clock input
XFCLK	G2	A8	O	Expansion bus FIFO interface clock output
XD31	M1	C13	I/O/Z	Expansion bus data • Used for transfer of data, address, and control • Also controls initialization of DSP modes and expansion bus at reset via pullup/pulldown resistors (Note: Reserved boot configuration fields should be pulled down.) XD[30:16] – $\overline{XCE[3:0]}$ memory type XD13 – XBLAST polarity XD12 – XW/R polarity XD11 – Asynchronous or synchronous host operation XD10 – Arbitration mode (internal or external) XD9 – FIFO mode XD8 – Little endian/big endian XD[4:0] – Boot mode Others – Reserved
XD30	M2	A13		
XD29	M3	C14		
XD28	N1	B14		
XD27	N2	B15		
XD26	N3	C15		
XD25	P1	A15		
XD24	P2	B16		
XD23	N5	C16		
XD22	R1	A17		
XD21	R2	B17		
XD20	P5	C17		
XD19	T1	B18		
XD18	T2	A19		
XD17	U1	C18		
XD16	T3	B19		
XD15	U2	C19		
XD14	V1	B20		
XD13	V2	A21		
XD12	W2	C21		
XD11	U4	D20		
XD10	W3	B22		
XD9	V4	D21		
XD8	W4	E20		
XD7	U5	E21		
XD6	V5	D22		
XD5	W5	F20		
XD4	U6	F21		
XD3	V6	E22		
XD2	V3	G20		
XD1	W6	G21		
XD0	U7	G22		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

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ADVANCE INFORMATION

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
EXPANSION BUS (CONTINUED)				
$\overline{XCE3}$	B4	D2	O/Z	Expansion bus I/O port memory space enables • Enabled by bits 28, 29, and 30 of the word address • Only one asserted during any I/O port data access
$\overline{XCE2}$	A3	B1		
$\overline{XCE1}$	C4	D3		
$\overline{XCE0}$	B3	C2		
$\overline{XBE3}$/XA5	E3	C5	I/O/Z	Expansion bus multiplexed byte-enable control/address signals • Act as byte-enable for host port operation • Act as address for I/O port operation
$\overline{XBE2}$/XA4	E2	A4		
$\overline{XBE1}$/XA3	E1	B5		
$\overline{XBE0}$/XA2	F3	C6		
$\overline{XOE}$	F5	A6	O/Z	Expansion bus I/O port output-enable
$\overline{XRE}$	F1	C7	O/Z	Expansion bus I/O port read-enable
$\overline{XWE}$/$\overline{XWAIT}$	G3	B7	O/Z	Expansion bus I/O port write-enable and host-port wait signals
$\overline{XCS}$	H1	C9	I	Expansion bus host-port chip-select input
$\overline{XAS}$	F2	B6	I/O/Z	Expansion bus host-port address strobe
XCNTL	H2	B9	I	Expansion bus host control. XCNTL selects between expansion bus address or data register.
XW/R	H3	B8	I/O/Z	Expansion bus host-port write/read enable. XW/R polarity is selected at reset.
XRDY	D2	C4	I/O/Z	Expansion bus host-port ready (active low) and I/O port ready (active high)
XBLAST	D1	B4	I/O/Z	Expansion bus host-port burst last-polarity selected at reset
XBOFF	J1	A10	I	Expansion bus back off
XHOLD	C2	A2	I/O/Z	Expansion bus hold request
XHOLDA	C1	B3	I/O/Z	Expansion bus hold acknowledge
EMIF – CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY				
$\overline{CE3}$	V18	Y21	O/Z	Memory space enables • Enabled by bits 24 and 25 of the word address • Only one asserted during any external data access
$\overline{CE2}$	U17	W20		
$\overline{CE1}$	W18	AA22		
$\overline{CE0}$	V17	W21		
$\overline{BE3}$	U16	V20	O/Z	Byte-enable control • Decoded from the two lowest bits of the internal address • Byte-write enables for most types of memory • Can be directly connected to SDRAM read and write mask signal (SDQM)
$\overline{BE2}$	W17	V21		
$\overline{BE1}$	V16	W22		
$\overline{BE0}$	W16	U20		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
EMIF – ADDRESS				
EA21	V7	H20	O/Z	External address (word address)
EA20	W7	H21		
EA19	U8	H22		
EA18	V8	J20		
EA17	W8	J21		
EA16	W9	K21		
EA15	V9	K20		
EA14	U9	K22		
EA13	W10	L21		
EA12	V10	L20		
EA11	U10	L22		
EA10	W11	M20		
EA9	V11	M21		
EA8	U11	N22		
EA7	R11	N20		
EA6	W12	N21		
EA5	U12	P21		
EA4	R12	P20		
EA3	W13	R22		
EA2	V13	R21		
EMIF – DATA				
ED31	F14	Y6	I/O/Z	External data
ED30	E19	AA6		
ED29	F17	AB6		
ED28	G15	Y7		
ED27	F18	AA7		
ED26	F19	AB8		
ED25	G17	Y8		
ED24	G18	AA8		
ED23	G19	AA9		
ED22	H17	Y9		
ED21	H18	AB10		
ED20	H19	Y10		
ED19	J18	AA10		
ED18	J19	AA11		
ED17	K15	Y11		
ED16	K17	AB12		
ED15	K18	Y12		
ED14	K19	AA12		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

ADVANCE INFORMATION

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Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
EMIF – DATA (CONTINUED)				
ED13	L17	AA13	I/O/Z	External data
ED12	L18	Y13		
ED11	L19	AB13		
ED10	M19	Y14		
ED9	M18	AA14		
ED8	M17	AA15		
ED7	N19	Y15		
ED6	P19	AB15		
ED5	N15	AA16		
ED4	P18	Y16		
ED3	P17	AB17		
ED2	R19	AA17		
ED1	R18	Y17		
ED0	R17	AA18		
EMIF – ASYNCHRONOUS MEMORY CONTROL				
$\overline{\text{ARE}}$	U14	T21	O/Z	Asynchronous memory read-enable
$\overline{\text{AOE}}$	W14	R20	O/Z	Asynchronous memory output-enable
$\overline{\text{AWE}}$	V14	T22	O/Z	Asynchronous memory write-enable
ARDY	W15	T20	I	Asynchronous memory ready input
EMIF – SYNCHRONOUS DRAM (SDRAM)/SYNCHRONOUS BURST SRAM (SBSRAM) CONTROL				
SDA10	U19	AA19	O/Z	SDRAM address 10 (separate for deactivate command)
$\overline{\text{SDCAS}}/\overline{\text{SSADS}}$	V19	AB21	O/Z	SDRAM column-address strobe/SBSRAM address strobe
$\overline{\text{SDRAS}}/\overline{\text{SSOE}}$	U18	Y19	O/Z	SDRAM row-address strobe/SBSRAM output-enable
$\overline{\text{SDWE}}/\overline{\text{SSWE}}$	T17	AA20	O/Z	SDRAM write-enable/SBSRAM write-enable
EMIF – BUS ARBITRATION				
$\overline{\text{HOLD}}$	P14	V22	I	Hold request from the host
$\overline{\text{HOLDA}}$	V15	U21	O	Hold-request-acknowledge to the host
TIMER 0				
TOUT0	E5	D1	O	Timer 0 or general-purpose output
TINP0	C5	E2	I	Timer 0 or general-purpose input
TIMER 1				
TOUT1	A5	F2	O	Timer 1 or general-purpose output
TINP1	B5	F3	I	Timer 1 or general-purpose input
DMA ACTION COMPLETE STATUS				
DMAC3	A17	V3	O	DMA action complete
DMAC2	B17	W2		
DMAC1	C16	AA1		
DMAC0	A18	W3		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE‡	DESCRIPTION
	GHK	GLW†		
MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)				
CLKS0	A12	K3	I	External clock source (as opposed to internal)
CLKR0	B9	L2	I/O/Z	Receive clock
CLKX0	C9	K1	I/O/Z	Transmit clock
DR0	A10	M2	I	Receive data
DX0	B10	M3	O/Z	Transmit data
FSR0	E10	M1	I/O/Z	Receive frame sync
FSX0	A9	L3	I/O/Z	Transmit frame sync
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1)				
CLKS1	C6	E1	I	External clock source (as opposed to internal)
CLKR1	B6	G2	I/O/Z	Receive clock
CLKX1	E6	G3	I/O/Z	Transmit clock
DR1	A7	H1	I	Receive data
DX1	B7	H2	O/Z	Transmit data
FSR1	C7	H3	I/O/Z	Receive frame sync
FSX1	A6	G1	I/O/Z	Transmit frame sync
RESERVED FOR TEST				
RSV0	C8	J2	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV1	A4	E3	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV2	K3	B11	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV3	L5	B13	O	Reserved (leave unconnected, ***do not*** connect to power or ground)
RSV4	B19	C10	O	Reserved (leave unconnected, ***do not*** connect to power or ground)
RSV5	C17	N1	I	Reserved (leave unconnected)
RSV6	D3	N2	I/O	Reserved (leave unconnected)
RSV7	K2	N3	I/O	Reserved (leave unconnected)
RSV8	J17	R2	I	Reserved (leave unconnected)
RSV9	N18	R1	O	Reserved (leave unconnected)
RSV10	C11	P3	I/O	Reserved (leave unconnected)
RSV11	–	P2	I/O	Reserved (leave unconnected) [For C6204 GLW packages only]

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

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Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW[†]	TYPE[‡]	DESCRIPTION
SUPPLY VOLTAGE PINS				
DV_{DD}	A2	A3	S	3.3-V supply voltage (I/O)
	B1	A7		
	B2	A16		
	C3	A20		
	E7	D4		
	E9	D6		
	E11	D7		
	E13	D9		
	F6	D10		
	G1	D13		
	H14	D14		
	J6	D16		
	K14	D17		
	L6	D19		
	L15	F1		
	M14	F4		
	P3	F19		
	P15	F22		
	R3	G4		
	R6	G19		
	R7	J4		
	R8	J19		
	R9	K4		
	R10	K19		
	R13	L1		
	R14	M22		
	U3	N4		
	U15	N19		
	–	P4		
	–	P19		
	–	T4		
	–	T19		
	–	U1		
	–	U4		
	–	U19		
	–	U22		
	–	W4		
	–	W6		
	–	W7		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
SUPPLY VOLTAGE PINS (CONTINUED)				
DV_{DD}	–	W9	S	3.3-V supply voltage (I/O)
	–	W10		
	–	W13		
	–	W14		
	–	W16		
	–	W17		
	–	W19		
	–	AB5		
	–	AB9		
	–	AB14		
	–	AB18		
CV_{DD}	B12	E7	S	1.5-V supply voltage (core)
	E14	E8		
	F9	E10		
	F10	E11		
	G5	E12		
	H15	E13		
	J2	E15		
	J5	E16		
	J15	G5		
	M5	G18		
	M15	H5		
	N17	H18		
	P6	K5		
	P9	K18		
	P12	L5		
	U13	L18		
	–	M5		
	–	M18		
	–	N5		
	–	N18		
	–	R5		
	–	R18		
	–	T5		
	–	T18		
	–	V7		
	–	V8		
	–	V10		
	–	V11		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

ADVANCE INFORMATION

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
SUPPLY VOLTAGE PINS (CONTINUED)				
CV_{DD}	–	V12	S	1.5-V supply voltage (core)
	–	V13		
	–	V15		
	–	V16		
GROUND PINS				
V_{SS}	A11	A1	GND	Ground pins
	A13	A5		
	B8	A12		
	B11	A18		
	B13	A22		
	C10	B2		
	C12	B21		
	C13	C1		
	C18	C3		
	E12	C20		
	G7	C22		
	G8	D5		
	G9	D8		
	G10	D11		
	G11	D12		
	G12	D15		
	G13	D18		
	H7	E4		
	H8	E5		
	H9	E6		
	H10	E9		
	H11	E14		
	H12	E17		
	H13	E18		
	J7	E19		
	J8	F5		
	J9	F18		
	J10	H4		
	J11	H19		
	J12	J1		
	J13	J5		
	K1	J18		
	K7	J22		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO. GHK	PIN NO. GLW†	TYPE‡	DESCRIPTION
GROUND PINS (CONTINUED)				
V_{SS}	K8	L4	GND	Ground pins
	K9	L19		
	K10	M4		
	K11	M19		
	K12	P1		
	K13	P5		
	L7	P18		
	L8	P22		
	L9	R4		
	L10	R19		
	L11	U5		
	L12	U18		
	L13	V4		
	M7	V5		
	M8	V6		
	M9	V9		
	M10	V14		
	M11	V17		
	M12	V18		
	M13	V19		
	N7	W5		
	N8	W8		
	N9	W11		
	N10	W12		
	N11	W15		
	N12	W18		
	N13	Y1		
	V12	Y3		
	–	Y20		
	–	Y22		
	–	AA2		
	–	AA21		
	–	AB1		
	–	AB3		
	–	AB7		
	–	AB11		
	–	AB16		
	–	AB20		
	–	AB22		

† The C6204 GLW BGA package is a subset of the GLS package (C6202/02B/03), with the inner row of core supply voltage (CV_{DD}) and ground (V_{SS}) pins removed (see the GLW BGA package bottom view).
‡ I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

ADVANCE INFORMATION

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:
Code Composer Studio™ Integrated Development Environment (IDE) including Editor
C/C++/Assembly Code Generation, and Debug plus additional development tools
Scalable, Real-Time Foundation Software (DSP BIOS), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:
Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
EVM (Evaluation Module)

The *TMS320 DSP Development Support Reference Guide* (SPRU011) contains information about development-support products for all TMS320™ DSP family member devices, including documentation. See this document for further information on TMS320™ DSP documentation or any TMS320™ DSP support products from Texas Instruments. An additional document, the *TMS320 Third-Party Support Reference Guide* (SPRU052), contains information about TMS320™ DSP-related products from other companies in the industry. To receive TMS320™ DSP literature, contact the Literature Response Center at 800/477-8924.

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL) and select "Find Development Tools". For device-specific tools, under "Semiconductor Products" select "Digital Signal Processors", choose a product family, and select the particular DSP device. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

ADVANCE INFORMATION

device and development-support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX / TMDX) through fully qualified production devices/tools (TMS / TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GLW), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, -200 is 200 MHz).

Table 3 lists the device orderable part numbers (P/Ns) and Figure 4 provides a legend for reading the complete device name for any TMS320C6000™ DSP family member.

ADVANCE INFORMATION

device and development-support tool nomenclature (continued)

Table 3. TMS320C6204 Device Part Numbers (P/Ns) and Ordering Information

DEVICE ORDERABLE P/N	DEVICE SPEED	CV_{DD} (CORE VOLTAGE)	DV_{DD} (I/O VOLTAGE)	OPERATING CASE TEMPERATURE RANGE
TMX320C6204GHK	200 MHz/1600 MIPS	1.5 V	3.3 V	0°C to 90°C
TMX320C6204GLW	200 MHz/1600 MIPS	1.5 V	3.3 V	0°C to 90°C

TMS 320 C 6204 GLW ( ) 200

PREFIX
- TMX = Experimental device
- TMP = Prototype device
- TMS = Qualified device
- SMX = Experimental device, MIL
- SMJ = MIL-PRF-38535, QML
- SM = High Rel (non-38535)

DEVICE FAMILY
- 320 = TMS320™ DSP family

TECHNOLOGY
- C = CMOS

DEVICE SPEED RANGE

100 MHz	200 MHz
120 MHz	233 MHz
150 MHz	250 MHz
167 MHz	300 MHz

TEMPERATURE RANGE (DEFAULT: 0°C TO 90°C)
- Blank = 0°C to 90°C, commercial temperature
- A = –40°C to 105°C, extended temperature

PACKAGE TYPE†
- GFN = 256-pin plastic BGA
- GGP = 352-pin plastic BGA
- GJC = 352-pin plastic BGA
- GJL = 352-pin plastic BGA
- GLS = 384-pin plastic BGA
- GLW = 340-pin plastic BGA
- GHK = 288-pin plastic MicroStar BGA™

DEVICE

C6000 DSP:

6201	6204	6414	6711
6202	6205	6415	6712
6202B	6211	6416	
6203	6211B	6701	

† BGA = Ball Grid Array

Figure 4. TMS320C6000™ DSP Platform Device Nomenclature (Including the TMS320C6204)

documentation support

Extensive documentation supports all TMS320™ DSP family devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000™ DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000™ DSP core (CPU) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190) describes the functionality of the peripherals available on the C6000™ DSP platform of devices, such as the 64-/32-/16-bit external memory interfaces (EMIFs), 32-/16-bit host-port interfaces (HPIs), multichannel buffered serial ports (McBSPs), direct memory access (DMA), enhanced direct-memory-access (EDMA) controller, expansion bus (XB), peripheral component interconnect (PCI), clocking and phase-locked loop (PLL); and power-down modes. This guide also includes information on internal data and program memories.

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the C62x™/C67x™ devices, associated development tools, and third-party support.

The tools support documentation is electronically available within the Code Composer Studio™ IDE. For a complete listing of the latest C6000™ DSP documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

The *How to Begin Development and Migrate Across the TMS320C6202/6202B/6203/6204 DSPs* application report (literature number SPRA603) describes the migration concerns and identifies the similarities and differences between the C6202, C6202B, C6203, and C6204 C6000™ DSP devices.

ADVANCE INFORMATION

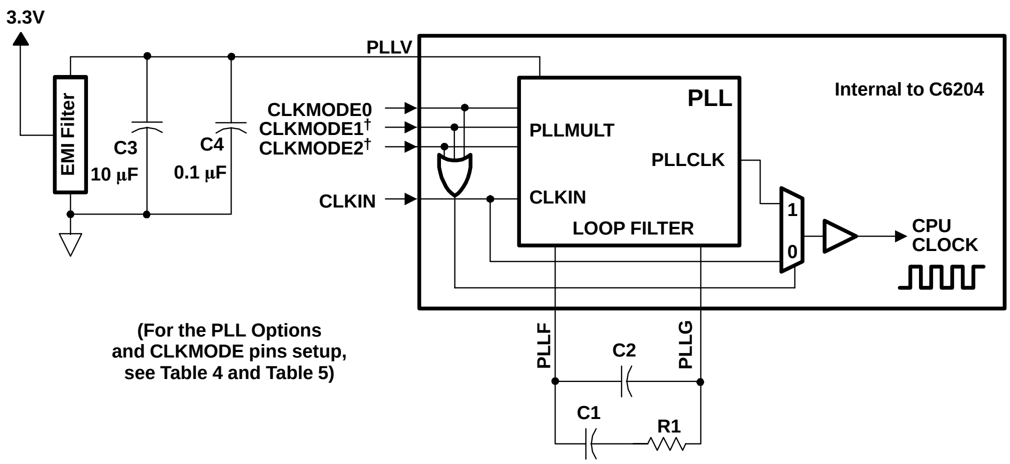
C67x is a trademark of Texas Instruments.

clock PLL

Most of the internal C6204 clocks are generated from a single source through the CLKIN pin. This source clock either drives the PLL, which multiplies the source clock in frequency to generate the internal CPU clock, or bypasses the PLL to become the internal CPU clock.

To use the PLL to generate the CPU clock, the external PLL filter circuit must be properly designed. Figure 5, Table 4, and Table 5 show the external PLL circuitry for either x1 (PLL bypass) or x4 PLL multiply modes. Figure 6 shows the external PLL circuitry for a system with ONLY x1 (PLL bypass) mode.

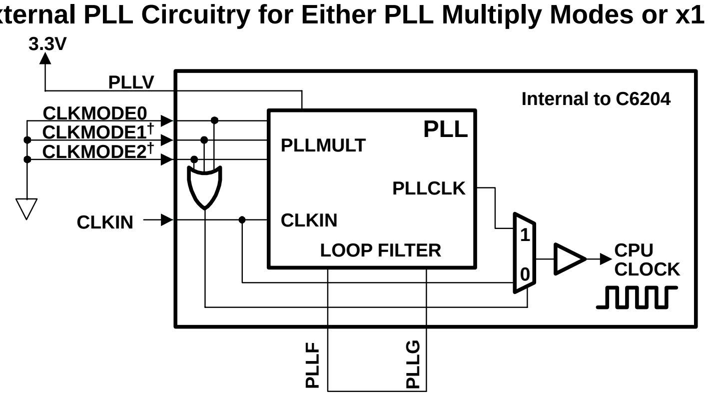
To minimize the clock jitter, a single clean power supply should power both the C6204 device and the external clock oscillator circuit. Noise coupling into PLLF directly impacts PLL clock jitter. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see the *input and output clocks* electricals section.



† CLKMODE1 and CLKMODE2 pins are not applicable to the GHK package.

NOTES: A. Keep the lead length and the number of vias between pin PLLF, pin PLLG, R1, C1, and C2 to a minimum. In addition, place all PLL components (R1, C1, C2, C3, C4, and EMI Filter) as close to the C6000™ DSP device as possible. Best performance is achieved with the PLL components on a single side of the board without jumpers, switches, or components other than the ones shown.
B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (R1, C1, C2, C3, C4, and the EMI Filter).
C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.
D. EMI filter manufacturer: TDK part number ACF451832-333, 223, 153, 103. Panasonic part number EXCCET103U.

Figure 5. External PLL Circuitry for Either PLL Multiply Modes or x1 (Bypass) Mode



† CLKMODE1 and CLKMODE2 pins are not applicable to the GHK package.

NOTES: A. For a system with ONLY PLL x1 (bypass) mode, short the PLLF to PLLG.
B. The 3.3-V supply for PLLV must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.

Figure 6. External PLL Circuitry for x1 (Bypass) PLL Mode Only

ADVANCE INFORMATION

clock PLL (continued)

Table 4. GHK/GLW Packages PLL Multiply and Bypass (x1) Options†

GHK PACKAGE – 16 x 16 mm MicroStar BGA™ GLW PACKAGE – 18 x 18 mm BGA				
BIT (PIN NO.)	**CLKMODE2 (A14) [GLW only]**	**CLKMODE1 (A9) [GLW only]**	**CLKMODE0 (L3) [GHK] CLKMODE0 (B12) [GLW]**	**PLL MULTIPLY FACTOR‡**
Value	X (Don’t Cares)	X	0	Bypass (x1)
	X	X	1	x4

† For the GLW package only, the CLKMODE2 (A14) and CLKMODE1 (A9) pins are internally unconnected. These pins are not applicable to the GHK package.
‡ f(CPU Clock) = f(CLKIN) x (PLL mode)

Table 5. PLL Component Selection Table§

CLKMODE	CLKIN RANGE (MHz)	CPU CLOCK FREQUENCY (CLKOUT1) RANGE (MHz)	CLKOUT2 RANGE (MHz)	R1 [±1%] (Ω)	C1 [±10%] (nF)	C2 [±10%] (pF)	TYPICAL LOCK TIME (µs)
x4	32.5–50	130–200	65–100	60.4	27	560	75

§ Under some operating conditions, the maximum PLL lock time may vary by as much as 150% from the specified typical value. For example, if the typical lock time is specified as 100 µs, the maximum value may be as long as 250 µs.

power-supply sequencing

TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage.

system-level design considerations

System-level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus, preventing bus contention with other chips on the board.

power-supply design considerations

For systems using the C6000™ DSP platform of devices, the core supply may be required to provide in excess of 2 A per DSP until the I/O supply is powered up. This extra current condition is a result of uninitialized logic within the DSP(s) and is corrected once the CPU sees an internal clock pulse. With the PLL enabled, as the I/O supply is powered on, a clock pulse is produced stopping the extra current draw from the supply. With the PLL disabled, as many as five external clock cycle pulses may be required to stop this extra current draw. A normal current state returns once the I/O power supply is turned on and the CPU sees a clock pulse. Decreasing the amount of time between the core supply power up and the I/O supply power up can minimize the effects of this current draw.

A dual-power supply with simultaneous sequencing, such as available with TPS563xx controllers or PT69xx plug-in power modules, can be used to eliminate the delay between core and I/O power up [see the *Using the TPS56300 to Power DSPs* application report (literature number SLVA088)]. A Schottky diode can also be used to tie the core rail to the I/O rail, effectively pulling up the I/O power supply to a level that can help initialize the logic within the DSP.

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power-supply design considerations (continued)

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000™ platform of DSPs, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

ADVANCE INFORMATION

absolute maximum ratings over operating case temperature ranges (unless otherwise noted)†

Supply voltage range, CV_{DD} (see Note 1) . . . . – 0.3 V to 2.3 V
Supply voltage range, DV_{DD} (see Note 1) . . . . –0.3 V to 4 V
Input voltage range . . . . –0.3 V to 4 V
Output voltage range . . . . –0.3 V to 4 V
Operating case temperature ranges, T_C: (default) . . . . 0°C to 90°C
(A version) . . . . –40°C to105°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Temperature cycle range, (1000-cycle performance) . . . . –40°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core	1.43	1.5	1.57	V
DV_{DD}	Supply voltage, I/O	3.14	3.3	3.46	V
V_{SS}	Supply ground	0	0	0	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–8	mA
I_{OL}	Low-level output current			8	mA
T_C	Operating case temperature	0		90	°C

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DV_{DD} = MIN, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	DV_{DD} = MIN, I_{OL} = MAX			0.6	V
I_I	Input current‡	$V_I = V_{SS}$ to DV_{DD}			±10	uA
I_{OZ}	Off-state output current	$V_O = DV_{DD}$ or 0 V			±10	uA
I_{DD2V}	Supply current, CPU + CPU memory access§	CV_{DD} = NOM, CPU clock = 200 MHz		290		mA
I_{DD2V}	Supply current, peripherals§	CV_{DD} = NOM, CPU clock = 200 MHz		240		mA
I_{DD3V}	Supply current, I/O pins§	DV_{DD} = NOM, CPU clock = 200 MHz		100		mA
C_i	Input capacitance				10	pF
C_o	Output capacitance				10	pF

‡ TMS and TDI are not included due to internal pullups. $\overline{TRST}$ is not included due to internal pulldown.
§ Measured with average activity (50% high / 50% low power). For more details on CPU, peripheral, and I/O activity, see the *TMS320C6000 Power Consumption Summary* application report (literature number SPRA486).

ADVANCE INFORMATION

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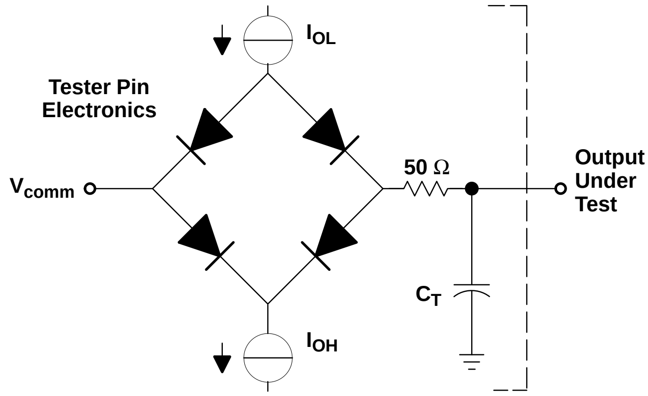
PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA
I_{OH} = 2 mA
V_{comm} = 0.8 V
C_T = 15–30-pF typical load-circuit capacitance

Figure 7. Test Load Circuit for AC Timing Measurements

signal transition levels

All input and output timing parameters are referenced to 1.5 V for both “0” and “1” logic levels.

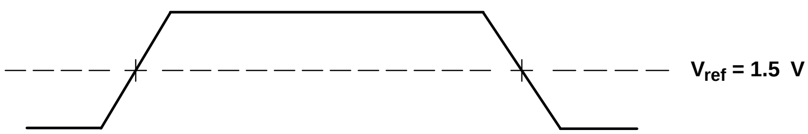


Figure 8. Input and Output Voltage Reference Levels for ac Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, and V_{OL} MAX and V_{OH} MIN for output clocks.

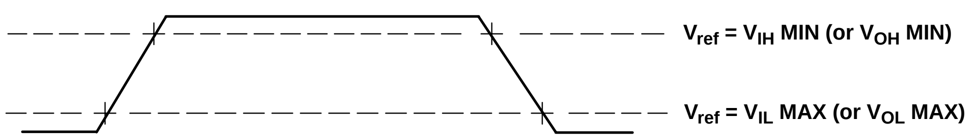


Figure 9. Rise and Fall Transition Time Voltage Reference Levels

INPUT AND OUTPUT CLOCKS

timing requirements for CLKIN†‡§ (see Figure 10)

NO.			-200				UNIT
			PLL mode x4		PLL mode x1 (BYPASS)		
			MIN	MAX	MIN	MAX	
1	$t_{c(CLKIN)}$	Cycle time, CLKIN	5 * M		5		ns
2	$t_{w(CLKINH)}$	Pulse duration, CLKIN high	0.4C		0.45C		ns
3	$t_{w(CLKINL)}$	Pulse duration, CLKIN low	0.4C		0.45C		ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN		5		0.6	ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
‡ M = the PLL multiplier factor (x4). For more details, see the *Clock PLL* section of this data sheet.
§ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 50 MHz, use C = 20 ns.

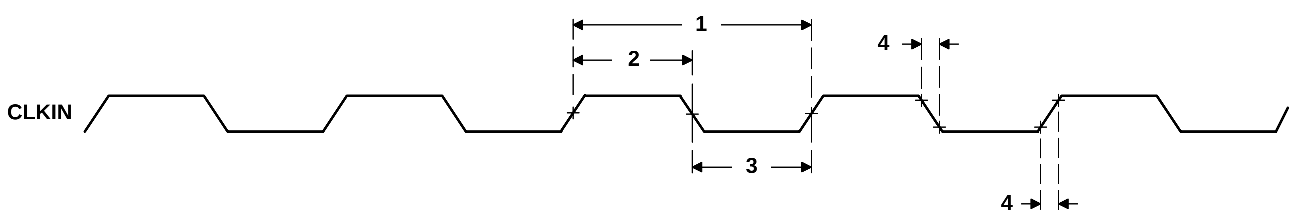


Figure 10. CLKIN Timings

timing requirements for XCLKIN¶ (see Figure 11)

NO.			-200		UNIT
			MIN	MAX	
1	$t_{c(XCLKIN)}$	Cycle time, XCLKIN	4P		ns
2	$t_{w(XCLKINH)}$	Pulse duration, XCLKIN high	1.8P		ns
3	$t_{w(XCLKINL)}$	Pulse duration, XCLKIN low	1.8P		ns

¶ P = 1/CPU clock frequency in nanoseconds (ns).

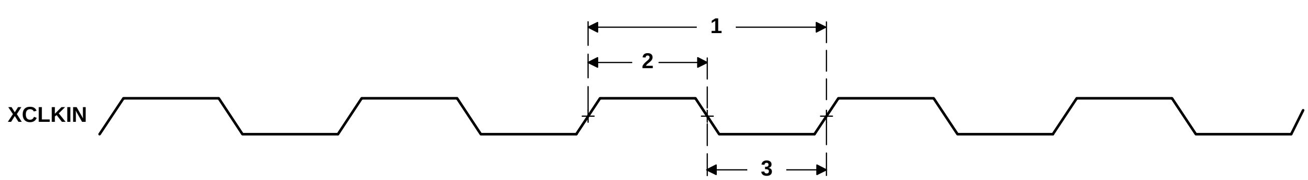


Figure 11. XCLKIN Timings

ADVANCE INFORMATION

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for CLKOUT1†‡§ (see Figure 12)

NO.	PARAMETER		-200 CLKMODE = x4 MIN	-200 CLKMODE = x4 MAX	-200 CLKMODE = x1 MIN	-200 CLKMODE = x1 MAX	UNIT
1	$t_{c(CKO1)}$	Cycle time, CLKOUT1	P – 0.7	P + 0.7	P – 0.7	P + 0.7	ns
2	$t_{w(CKO1H)}$	Pulse duration, CLKOUT1 high	(P/2) – 0.7	(P/2) + 0.7	PH – 0.7	PH + 0.7	ns
3	$t_{w(CKO1L)}$	Pulse duration, CLKOUT1 low	(P/2) – 0.7	(P/2) + 0.7	PL – 0.7	PL + 0.7	ns
4	$t_{t(CKO1)}$	Transition time, CLKOUT1		0.6		0.6	ns

† The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
‡ PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.
§ P = 1/CPU clock frequency in ns.

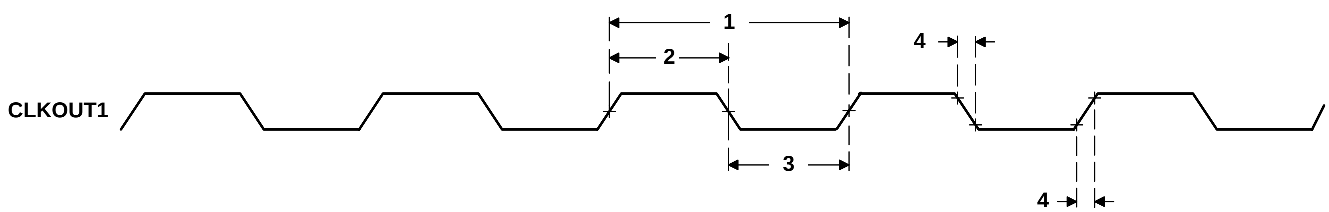


Figure 12. CLKOUT1 Timings

switching characteristics over recommended operating conditions for CLKOUT2†§ (see Figure 13)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{c(CKO2)}$	Cycle time, CLKOUT2	2P – 0.7	2P + 0.7	ns
2	$t_{w(CKO2H)}$	Pulse duration, CLKOUT2 high	P – 0.7	P + 0.7	ns
3	$t_{w(CKO2L)}$	Pulse duration, CLKOUT2 low	P – 0.7	P + 0.7	ns
4	$t_{t(CKO2)}$	Transition time, CLKOUT2		0.6	ns

† The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
§ P = 1/CPU clock frequency in ns.

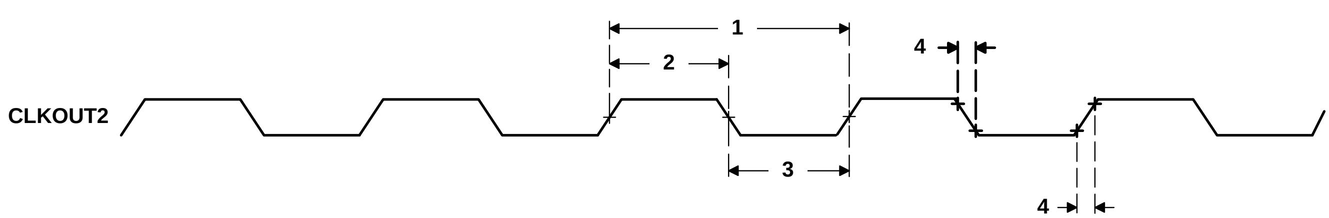


Figure 13. CLKOUT2 Timings

ADVANCE INFORMATION

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for XFCLK†‡ (see Figure 14)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{c(XFCK)}$	Cycle time, XFCLK	D * P – 0.7	D * P + 0.7	ns
2	$t_{w(XFCKH)}$	Pulse duration, XFCLK high	(D/2) * P – 0.7	(D/2) * P + 0.7	ns
3	$t_{w(XFCKL)}$	Pulse duration, XFCLK low	(D/2) * P – 0.7	(D/2) * P + 0.7	ns
4	$t_{t(CKO2)}$	Transition time, XFCLK		0.6	ns

† P = 1/CPU clock frequency in ns.
‡ D = 8, 6, 4, or 2; FIFO clock divide ratio, user-programmable

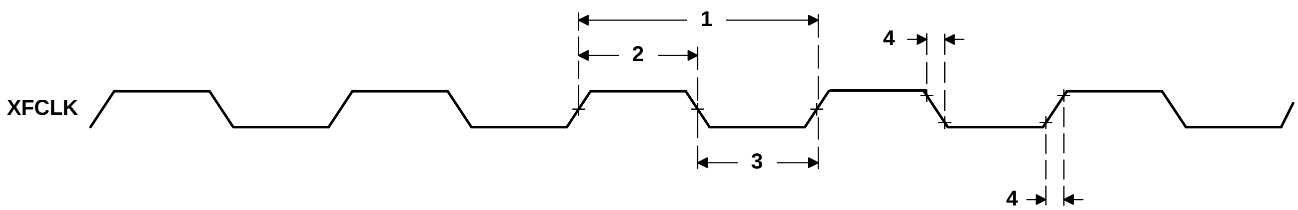


Figure 14. XFCLK Timings

ADVANCE INFORMATION

ASYNCHRONOUS MEMORY TIMING

timing requirements for asynchronous memory cycles†‡§¶ (see Figure 15 – Figure 18)

NO.			-200		UNIT
			MIN	MAX	
3	$t_{su(EDV-AREH)}$	Setup time, EDx valid before $\overline{ARE}$ high	1.5		ns
4	$t_{h(AREH-EDV)}$	Hold time, EDx valid after $\overline{ARE}$ high	3.5		ns
6	$t_{su(ARDYH-AREL)}$	Setup time, ARDY high before $\overline{ARE}$ low	–[(RST – 3) * P – 6]		ns
7	$t_{h(AREL-ARDYH)}$	Hold time, ARDY high after $\overline{ARE}$ low	(RST – 3) * P + 3		ns
9	$t_{su(ARDYL-AREL)}$	Setup time, ARDY low before $\overline{ARE}$ low	–[(RST – 3) * P – 6]		ns
10	$t_{h(AREL-ARDYL)}$	Hold time, ARDY low after $\overline{ARE}$ low	(RST – 3) * P + 3		ns
11	$t_{w(ARDYH)}$	Pulse width, ARDY high	2P		ns
15	$t_{su(ARDYH-AWEL)}$	Setup time, ARDY high before $\overline{AWE}$ low	–[(WST – 3) * P – 6]		ns
16	$t_{h(AWEL-ARDYH)}$	Hold time, ARDY high after $\overline{AWE}$ low	(WST – 3) * P + 3		ns
18	$t_{su(ARDYL-AWEL)}$	Setup time, ARDY low before $\overline{AWE}$ low	–[(WST – 3) * P – 6]		ns
19	$t_{h(AWEL-ARDYL)}$	Hold time, ARDY low after $\overline{AWE}$ low	(WST – 3) * P + 3		ns

† To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be an asynchronous input.
‡ RS = Read Setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold. These parameters are programmed via the EMIF CE space control registers.
§ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
¶ The sum of RS and RST (or WS and WST) must be a minimum of 4 in order to use ARDY input to extend strobe width.

switching characteristics over recommended operating conditions for asynchronous memory cycles‡§¶# (see Figure 15 – Figure 18)

NO.	PARAMETER		-200			UNIT
			MIN	TYP	MAX	
1	$t_{osu(SELV-AREL)}$	Output setup time, select signals valid to $\overline{ARE}$ low	RS * P – 2			ns
2	$t_{oh(AREH-SELIV)}$	Output hold time, $\overline{ARE}$ high to select signals invalid	RH * P – 2			ns
5	$t_{w(AREL)}$	Pulse width, $\overline{ARE}$ low		RST * P		ns
8	$t_{d(ARDYH-AREH)}$	Delay time, ARDY high to $\overline{ARE}$ high	3P		4P + 5	ns
12	$t_{osu(SELV-AWEL)}$	Output setup time, select signals valid to $\overline{AWE}$ low	WS * P – 2			ns
13	$t_{oh(AWEH-SELIV)}$	Output hold time, $\overline{AWE}$ high to select signals invalid	WH * P – 2			ns
14	$t_{w(AWEL)}$	Pulse width, $\overline{AWE}$ low		WST * P		ns
17	$t_{d(ARDYH-AWEH)}$	Delay time, ARDY high to $\overline{AWE}$ high	3P		4P + 5	ns

‡ RS = Read Setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold. These parameters are programmed via the EMIF CE space control registers.
§ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
¶ The sum of RS and RST (or WS and WST) must be a minimum of 4 in order to use ARDY input to extend strobe width.
# Select signals include: $\overline{CEx}$, $\overline{BE[3:0]}$, EA[21:2], $\overline{AOE}$; and for writes, include ED[31:0], with the exception that $\overline{CEx}$ can stay active for an additional 7P ns following the end of the cycle.

ADVANCE INFORMATION

ASYNCHRONOUS MEMORY TIMING (CONTINUED)

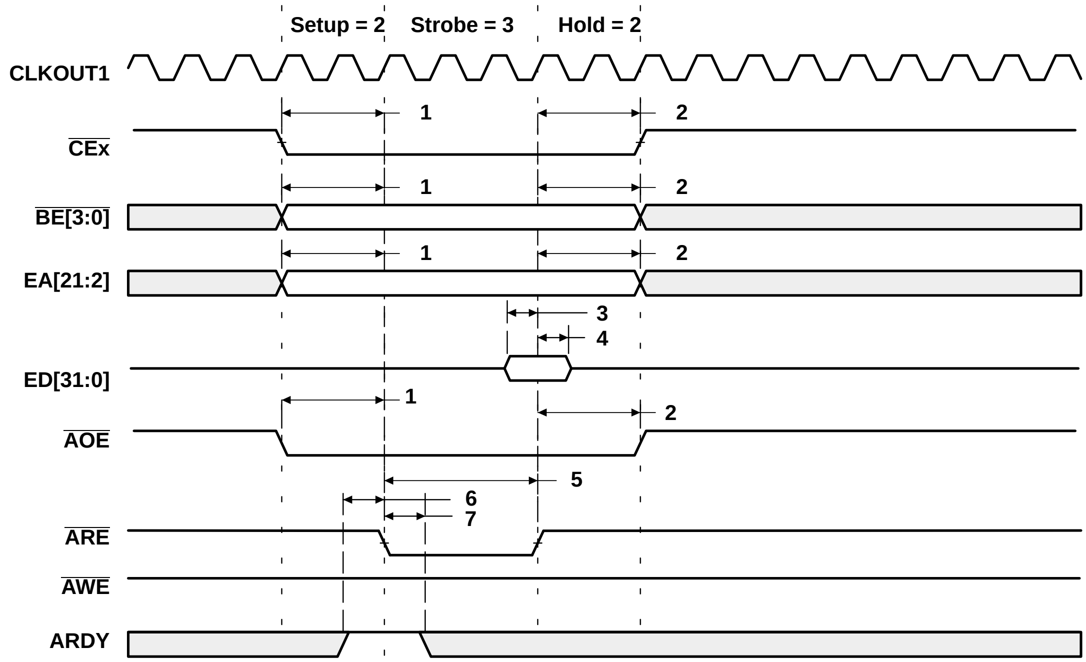


Figure 15. Asynchronous Memory Read Timing (ARDY Not Used)

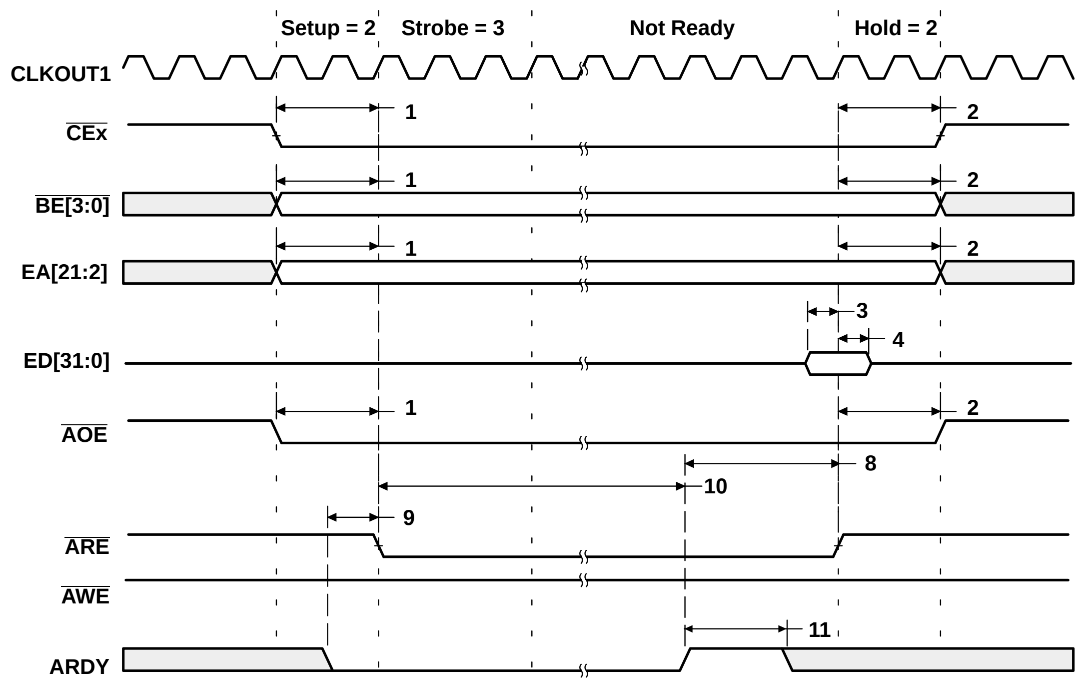


Figure 16. Asynchronous Memory Read Timing (ARDY Used)

ADVANCE INFORMATION

ASYNCHRONOUS MEMORY TIMING (CONTINUED)

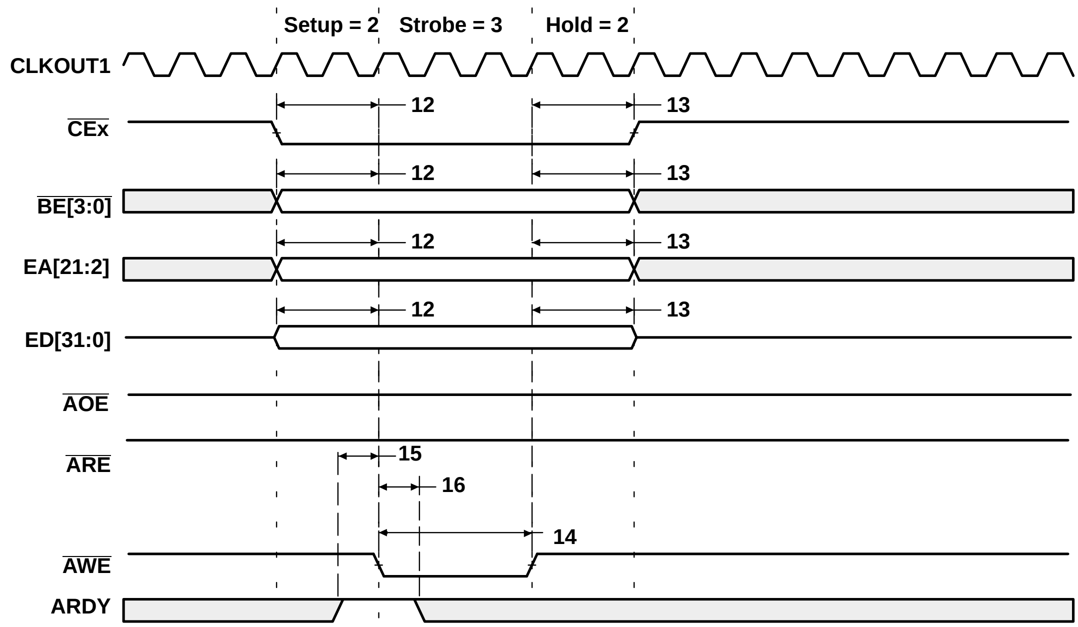


Figure 17. Asynchronous Memory Write Timing (ARDY Not Used)

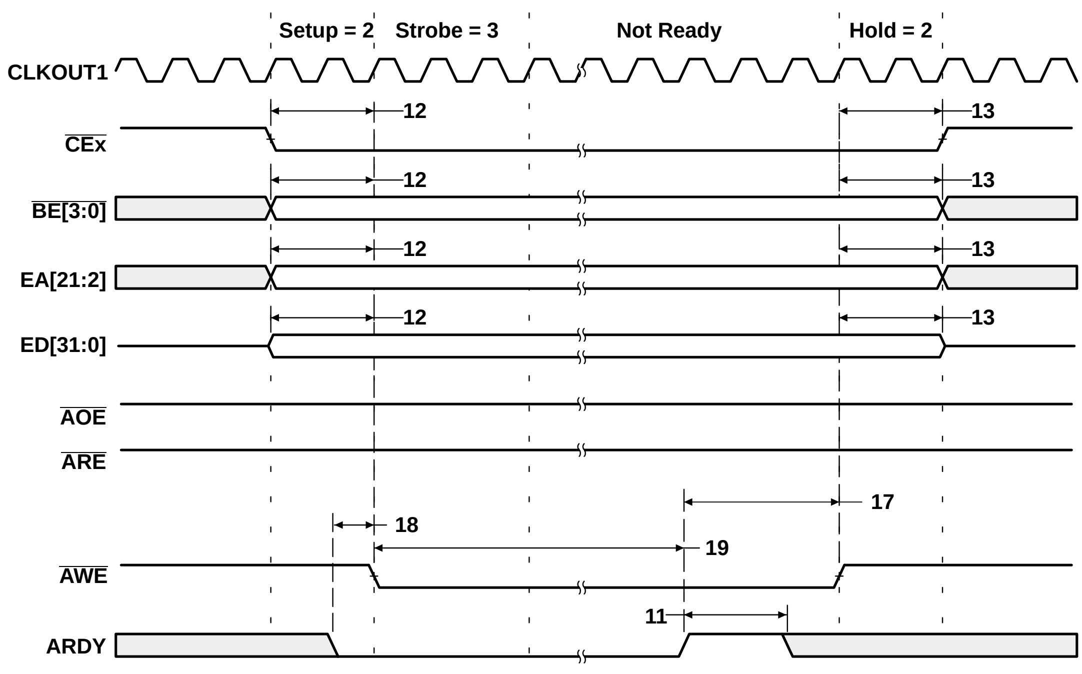


Figure 18. Asynchronous Memory Write Timing (ARDY Used)

SYNCHRONOUS-BURST MEMORY TIMING

timing requirements for synchronous-burst SRAM cycles (see Figure 19)

NO.			-200 MIN	-200 MAX	UNIT
7	$t_{su(EDV-CKO2H)}$	Setup time, read EDx valid before CLKOUT2 high	2.5		ns
8	$t_{h(CKO2H-EDV)}$	Hold time, read EDx valid after CLKOUT2 high	1.5		ns

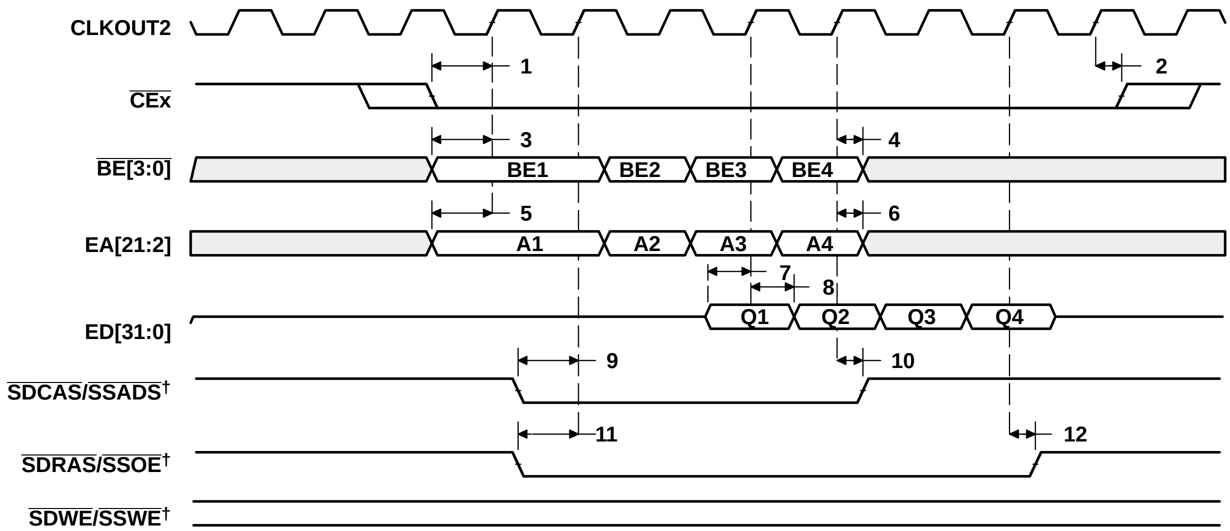
switching characteristics over recommended operating conditions for synchronous-burst SRAM cycles†‡ (see Figure 19 and Figure 20)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{osu(CEV-CKO2H)}$	Output setup time, $\overline{\text{CEx}}$ valid before CLKOUT2 high	P – 0.8		ns
2	$t_{oh(CKO2H-CEV)}$	Output hold time, $\overline{\text{CEx}}$ valid after CLKOUT2 high	P – 4		ns
3	$t_{osu(BEV-CKO2H)}$	Output setup time, $\overline{\text{BEx}}$ valid before CLKOUT2 high	P – 0.8		ns
4	$t_{oh(CKO2H-BEIV)}$	Output hold time, $\overline{\text{BEx}}$ invalid after CLKOUT2 high	P – 4		ns
5	$t_{osu(EAV-CKO2H)}$	Output setup time, EAx valid before CLKOUT2 high	P – 0.8		ns
6	$t_{oh(CKO2H-EAIV)}$	Output hold time, EAx invalid after CLKOUT2 high	P – 4		ns
9	$t_{osu(ADSV-CKO2H)}$	Output setup time, $\overline{\text{SDCAS}}/\overline{\text{SSADS}}$ valid before CLKOUT2 high	P – 0.8		ns
10	$t_{oh(CKO2H-ADSV)}$	Output hold time, $\overline{\text{SDCAS}}/\overline{\text{SSADS}}$ valid after CLKOUT2 high	P – 4		ns
11	$t_{osu(OEV-CKO2H)}$	Output setup time, $\overline{\text{SDRAS}}/\overline{\text{SSOE}}$ valid before CLKOUT2 high	P – 0.8		ns
12	$t_{oh(CKO2H-OEV)}$	Output hold time, $\overline{\text{SDRAS}}/\overline{\text{SSOE}}$ valid after CLKOUT2 high	P – 4		ns
13	$t_{osu(EDV-CKO2H)}$	Output setup time, EDx valid before CLKOUT2 high§	P – 1		ns
14	$t_{oh(CKO2H-EDIV)}$	Output hold time, EDx invalid after CLKOUT2 high	P – 4		ns
15	$t_{osu(WEV-CKO2H)}$	Output setup time, $\overline{\text{SDWE}}/\overline{\text{SSWE}}$ valid before CLKOUT2 high	P – 0.8		ns
16	$t_{oh(CKO2H-WEV)}$	Output hold time, $\overline{\text{SDWE}}/\overline{\text{SSWE}}$ valid after CLKOUT2 high	P – 4		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ $\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.
§ For the first write in a series of one or more consecutive adjacent writes, the write data is generated one CLKOUT2 cycle early to accommodate the ED enable time.

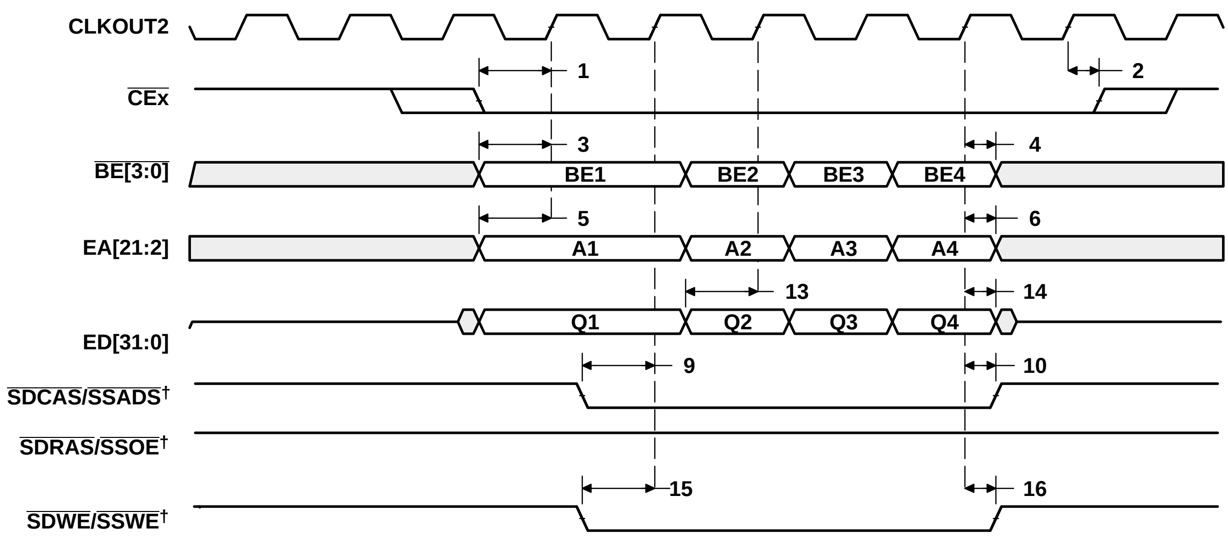
ADVANCE INFORMATION

SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)



† $\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$, and $\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.

Figure 19. SBSRAM Read Timing



† $\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$, and $\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.

Figure 20. SBSRAM Write Timing

SYNCHRONOUS DRAM TIMING

timing requirements for synchronous DRAM cycles (see Figure 21)

NO.			-200		UNIT
			MIN	MAX	
7	$t_{su(EDV-CKO2H)}$	Setup time, read EDx valid before CLKOUT2 high	1.25		ns
8	$t_{h(CKO2H-EDV)}$	Hold time, read EDx valid after CLKOUT2 high	3		ns

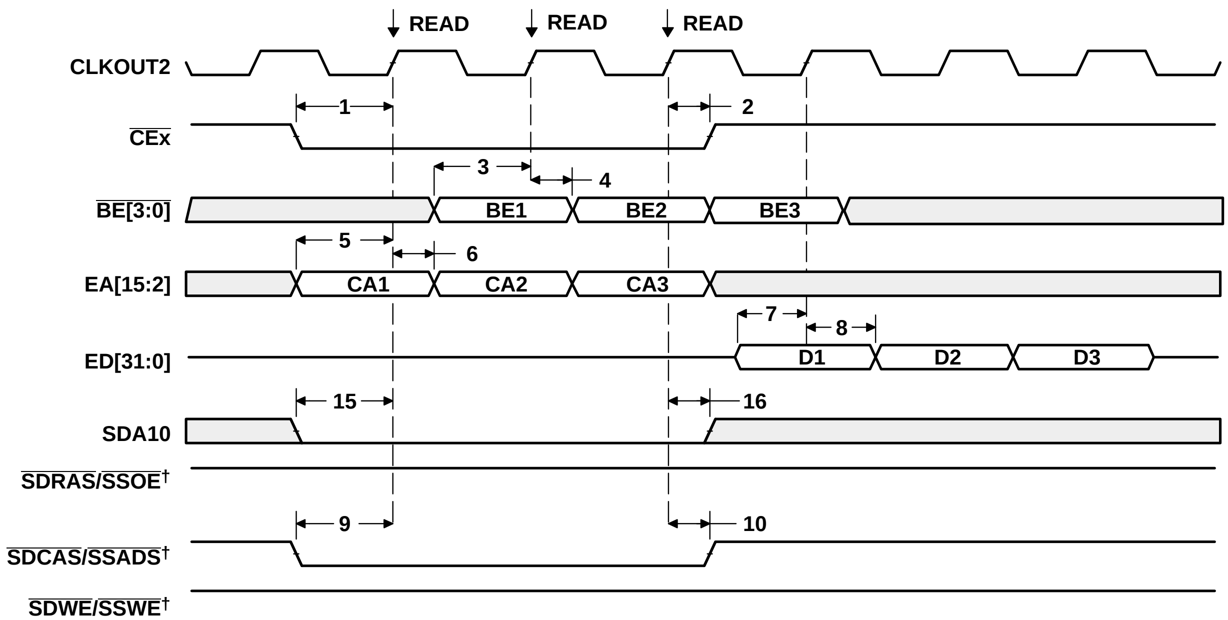
switching characteristics over recommended operating conditions for synchronous DRAM cycles†‡ (see Figure 21–Figure 26)

NO.	PARAMETER		-200		UNIT
			MIN	MAX	
1	$t_{osu(CEV-CKO2H)}$	Output setup time, $\overline{CEx}$ valid before CLKOUT2 high	P – 1		ns
2	$t_{oh(CKO2H-CEV)}$	Output hold time, $\overline{CEx}$ valid after CLKOUT2 high	P – 3.5		ns
3	$t_{osu(BEV-CKO2H)}$	Output setup time, $\overline{BEx}$ valid before CLKOUT2 high	P – 1		ns
4	$t_{oh(CKO2H-BEIV)}$	Output hold time, $\overline{BEx}$ invalid after CLKOUT2 high	P – 3.5		ns
5	$t_{osu(EAV-CKO2H)}$	Output setup time, EAx valid before CLKOUT2 high	P – 1		ns
6	$t_{oh(CKO2H-EAIV)}$	Output hold time, EAx invalid after CLKOUT2 high	P – 3.5		ns
9	$t_{osu(CASV-CKO2H)}$	Output setup time, $\overline{SDCAS}$/$\overline{SSADS}$ valid before CLKOUT2 high	P – 1		ns
10	$t_{oh(CKO2H-CASV)}$	Output hold time, $\overline{SDCAS}$/$\overline{SSADS}$ valid after CLKOUT2 high	P – 3.5		ns
11	$t_{osu(EDV-CKO2H)}$	Output setup time, EDx valid before CLKOUT2 high§	P – 3		ns
12	$t_{oh(CKO2H-EDIV)}$	Output hold time, EDx invalid after CLKOUT2 high	P – 3.5		ns
13	$t_{osu(WEV-CKO2H)}$	Output setup time, $\overline{SDWE}$/$\overline{SSWE}$ valid before CLKOUT2 high	P – 1		ns
14	$t_{oh(CKO2H-WEV)}$	Output hold time, $\overline{SDWE}$/$\overline{SSWE}$ valid after CLKOUT2 high	P – 3.5		ns
15	$t_{osu(SDA10V-CKO2H)}$	Output setup time, SDA10 valid before CLKOUT2 high	P – 1		ns
16	$t_{oh(CKO2H-SDA10IV)}$	Output hold time, SDA10 invalid after CLKOUT2 high	P – 3.5		ns
17	$t_{osu(RASV-CKO2H)}$	Output setup time, $\overline{SDRAS}$/$\overline{SSOE}$ valid before CLKOUT2 high	P – 1		ns
18	$t_{oh(CKO2H-RASV)}$	Output hold time, $\overline{SDRAS}$/$\overline{SSOE}$ valid after CLKOUT2 high	P – 3.5		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ $\overline{SDCAS}$/$\overline{SSADS}$, $\overline{SDRAS}$/$\overline{SSOE}$, and $\overline{SDWE}$/$\overline{SSWE}$ operate as $\overline{SDCAS}$, $\overline{SDRAS}$, and $\overline{SDWE}$, respectively, during SDRAM accesses.
§ For the first write in a series of one or more consecutive adjacent writes, the write data is generated one CLKOUT2 cycle early to accommodate the ED enable time.

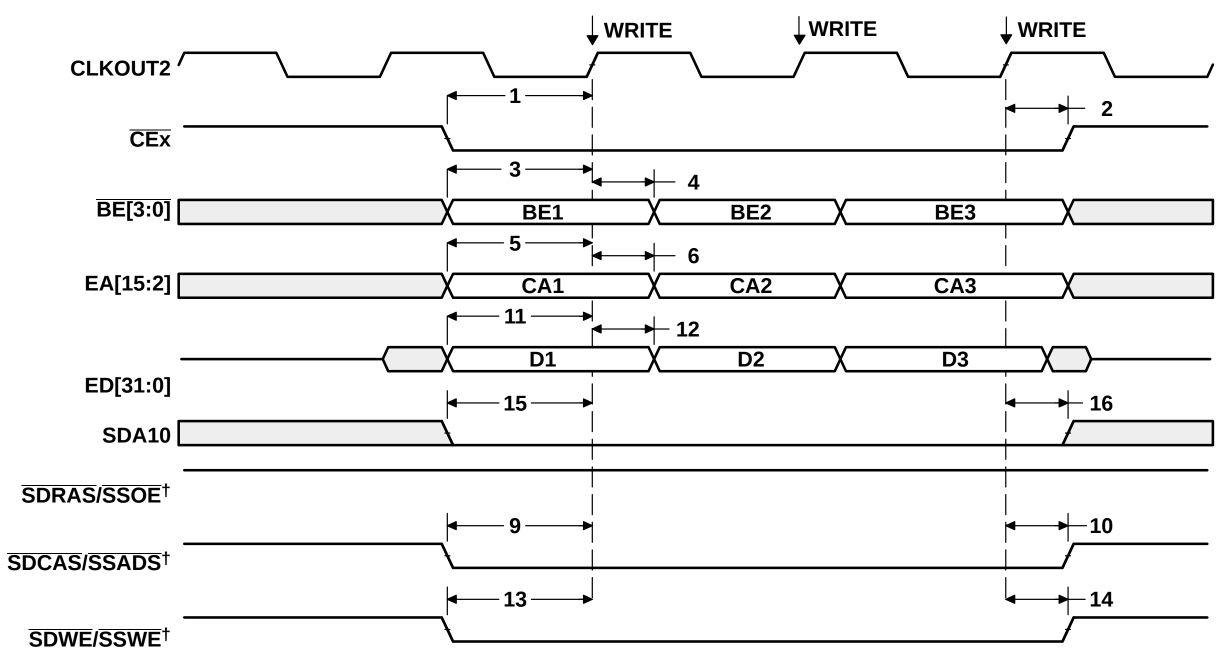
ADVANCE INFORMATION

SYNCHRONOUS DRAM TIMING (CONTINUED)



† SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SDCAS, SDRAS, and SDWE, respectively, during SDRAM accesses.

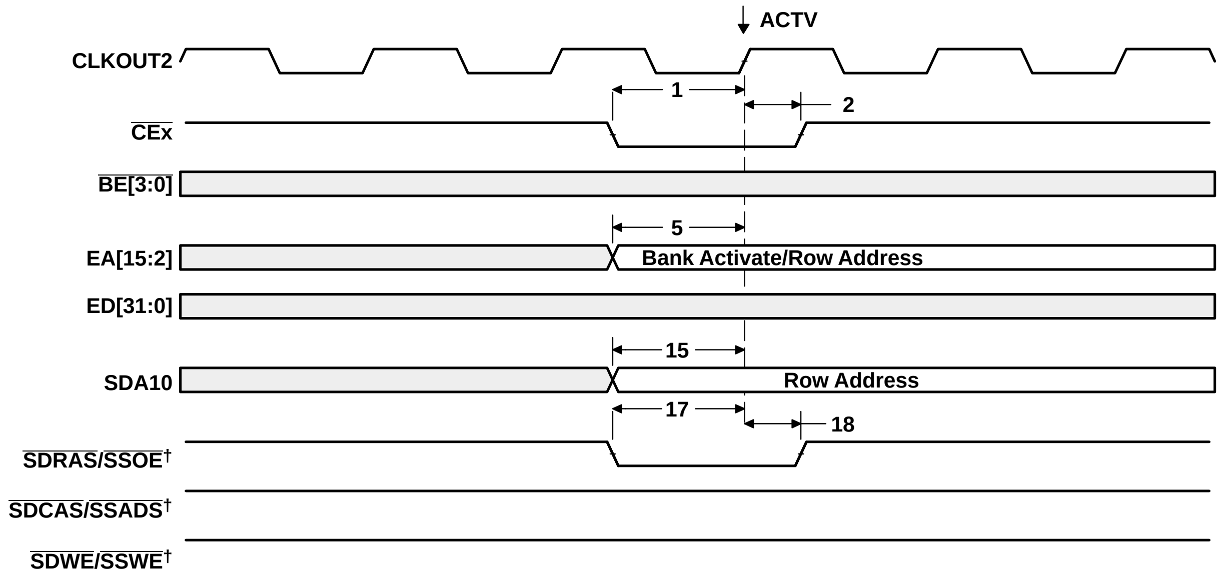
Figure 21. Three SDRAM READ Commands



† SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SDCAS, SDRAS, and SDWE, respectively, during SDRAM accesses.

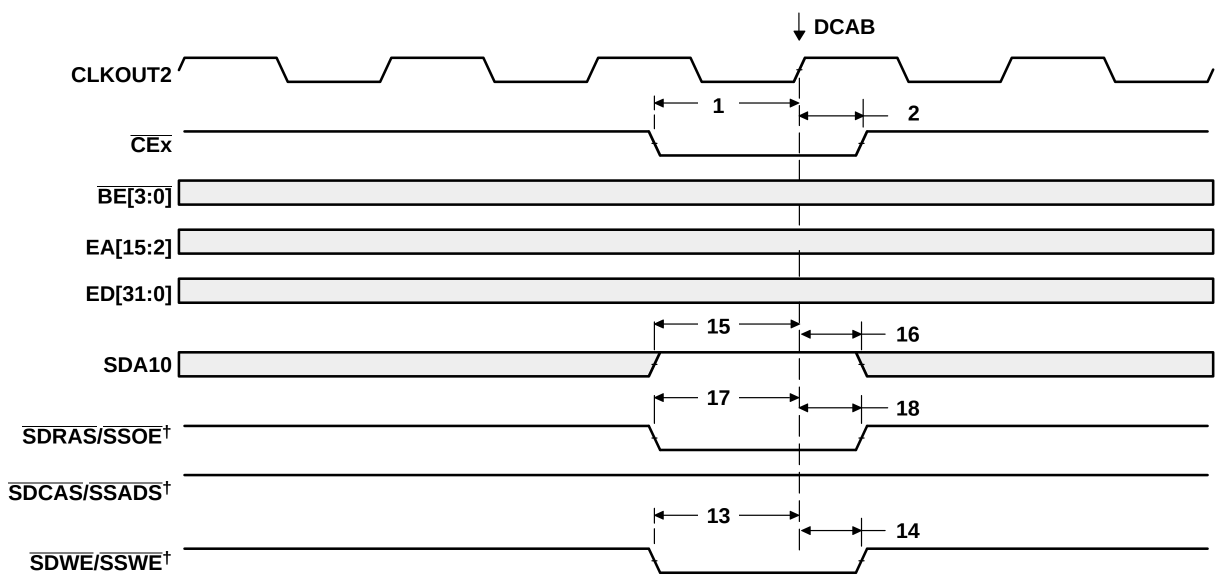
Figure 22. Three SDRAM WRT Commands

SYNCHRONOUS DRAM TIMING (CONTINUED)



† SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SDCAS, SDRAS, and SDWE, respectively, during SDRAM accesses.

Figure 23. SDRAM ACTV Command

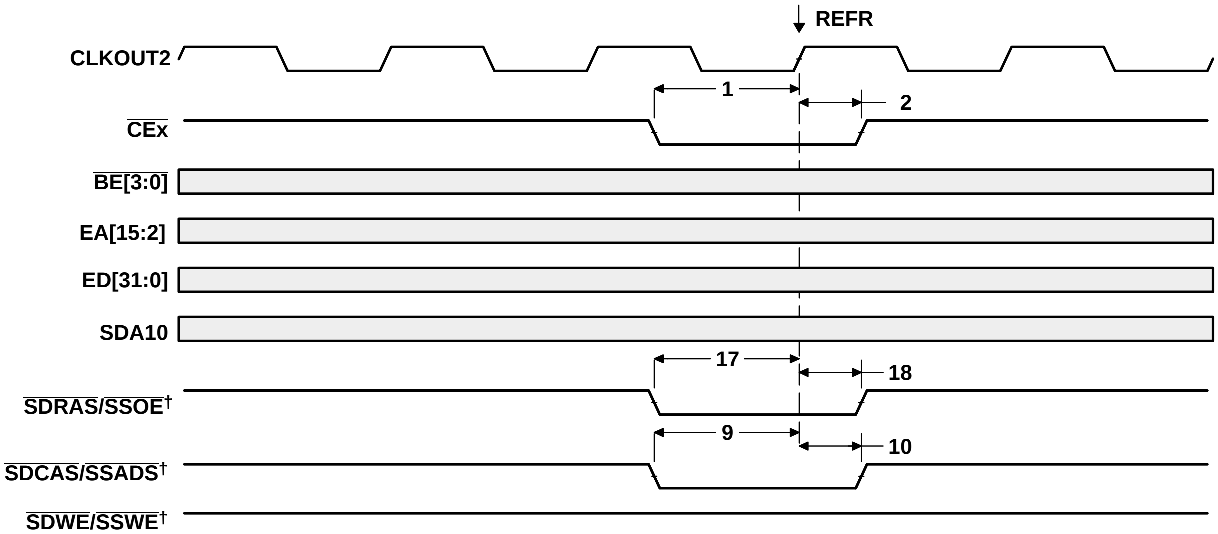


† SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SDCAS, SDRAS, and SDWE, respectively, during SDRAM accesses.

Figure 24. SDRAM DCAB Command

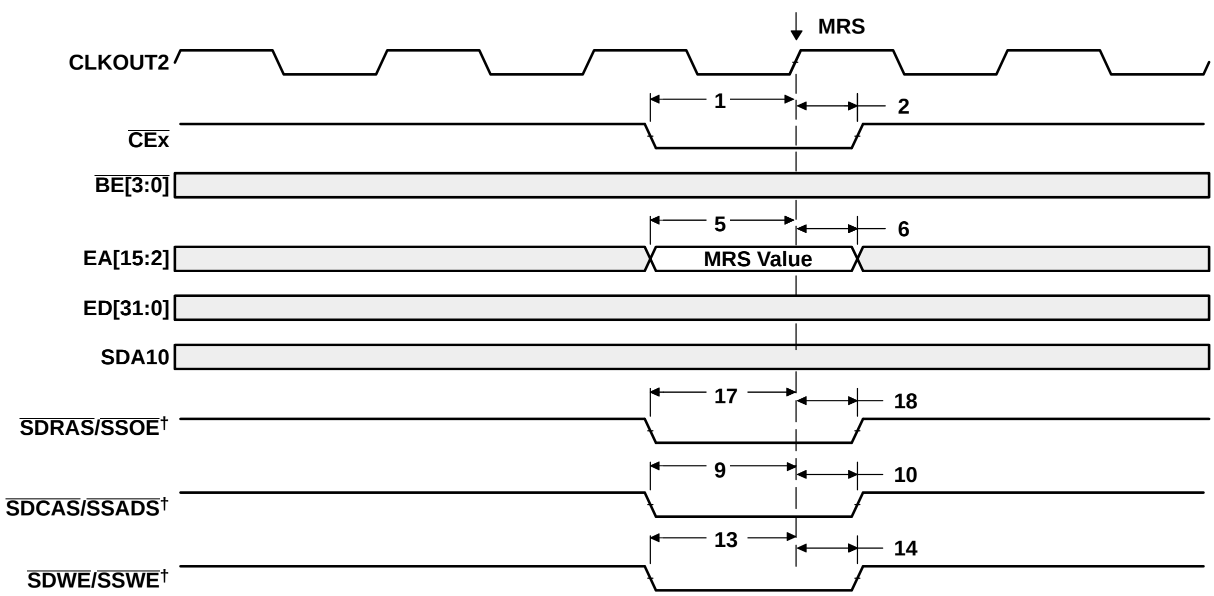
ADVANCE INFORMATION

SYNCHRONOUS DRAM TIMING (CONTINUED)



† SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SDCAS, SDRAS, and SDWE, respectively, during SDRAM accesses.

Figure 25. SDRAM REFR Command



† SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SDCAS, SDRAS, and SDWE, respectively, during SDRAM accesses.

Figure 26. SDRAM MRS Command

HOLD/HOLDA TIMING

timing requirements for the HOLD/HOLDA cycles† (see Figure 27)

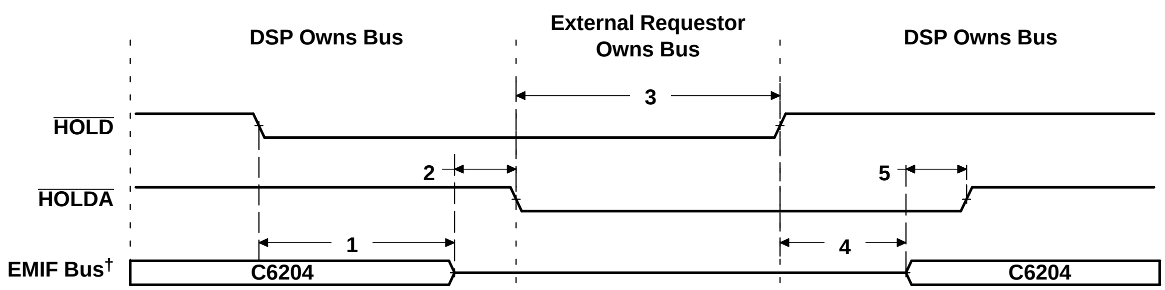
NO.			-200 MIN	-200 MAX	UNIT
3	$t_{oh(HOLDAL-HOLDL)}$	Output hold time, HOLD low after HOLDA low	P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

switching characteristics over recommended operating conditions for the HOLD/HOLDA cycles†‡ (see Figure 27)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{d(HOLDL-EMHZ)}$	Delay time, HOLD low to EMIF Bus high impedance	4P	§	ns
2	$t_{d(EMHZ-HOLDAL)}$	Delay time, EMIF Bus high impedance to HOLDA low	0	2P	ns
4	$t_{d(HOLDH-EMLZ)}$	Delay time, HOLD high to EMIF Bus low impedance	3P	7P	ns
5	$t_{d(EMLZ-HOLDAH)}$	Delay time, EMIF Bus low impedance to HOLDA high	0	2P	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE, AOE, AWE, SDCAS/SSADS, SDRAS/SSOE, SDWE/SSWE, and SDA10.
§ All pending EMIF transactions are allowed to complete before HOLDA is asserted. The worst case for this is an asynchronous read or write with external ARDY used or a minimum of eight consecutive SDRAM reads or writes when RBTR8 = 1. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.



† EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE, AOE, AWE, SDCAS/SSADS, SDRAS/SSOE, SDWE/SSWE, and SDA10.

Figure 27. HOLD/HOLDA Timing

ADVANCE INFORMATION

ADVANCE INFORMATION

RESET TIMING

timing requirements for reset† (see Figure 28)

NO.			-200 MIN	-200 MAX	UNIT
1	$t_{w(RST)}$	Width of the $\overline{\text{RESET}}$ pulse (PLL stable)‡	10P		ns
		Width of the $\overline{\text{RESET}}$ pulse (PLL needs to sync up)§	250		µs
10	$t_{su(XD)}$	Setup time, XD configuration bits valid before $\overline{\text{RESET}}$ high¶	5P		ns
11	$t_{h(XD)}$	Hold time, XD configuration bits valid after $\overline{\text{RESET}}$ high¶	5P		ns

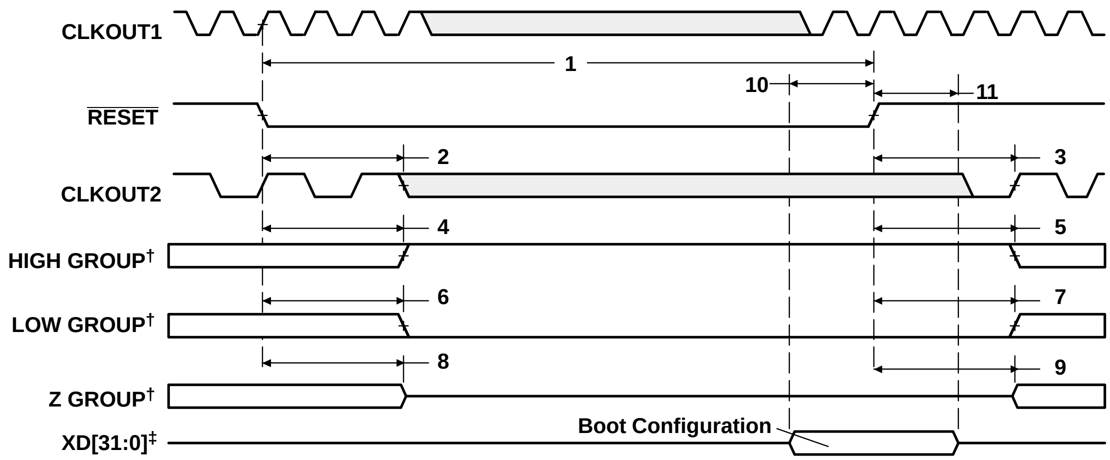
† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x4 when CLKIN and PLL are stable.
§ This parameter applies to CLKMODE x4 only (it does not apply to CLKMODE x1). The $\overline{\text{RESET}}$ signal is not connected internally to the Clock PLL circuit. The PLL requires a minimum of 250 µs to stabilize following device power up or after PLL configuration has been changed. During that time, $\overline{\text{RESET}}$ must be asserted to ensure proper device operation. See the *clock PLL* section for PLL lock times.
¶ XD[31:0] are the boot configuration pins during device reset.

switching characteristics over recommended operating conditions during reset†# (see Figure 28)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
2	$t_{d(RSTL-CKO2IV)}$	Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 invalid	P		ns
3	$t_{d(RSTH-CKO2V)}$	Delay time, $\overline{\text{RESET}}$ high to CLKOUT2 valid		4P	ns
4	$t_{d(RSTL-HIGHIV)}$	Delay time, $\overline{\text{RESET}}$ low to high group invalid	P		ns
5	$t_{d(RSTH-HIGHV)}$	Delay time, $\overline{\text{RESET}}$ high to high group valid		4P	ns
6	$t_{d(RSTL-LOWIV)}$	Delay time, $\overline{\text{RESET}}$ low to low group invalid	P		ns
7	$t_{d(RSTH-LOWV)}$	Delay time, $\overline{\text{RESET}}$ high to low group valid		4P	ns
8	$t_{d(RSTL-ZHZ)}$	Delay time, $\overline{\text{RESET}}$ low to Z group high impedance	P		ns
9	$t_{d(RSTH-ZV)}$	Delay time, $\overline{\text{RESET}}$ high to Z group valid		4P	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
# High group consists of: XFCLK, $\overline{\text{HOLDA}}$
Low group consists of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0, and TOUT1.
Z group consists of: EA[21:2], ED[31:0], $\overline{\text{CE[3:0]}}$, $\overline{\text{BE[3:0]}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AOE}}$, $\overline{\text{SDCAS/SSADS}}$, $\overline{\text{SDRAS/SSOE}}$, $\overline{\text{SDWE/SSWE}}$, SDA10, CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, $\overline{\text{XCE[3:0]}}$, $\overline{\text{XBE[3:0]}}$/XA[5:2], $\overline{\text{XOE}}$, $\overline{\text{XRE}}$, $\overline{\text{XWE/XWAIT}}$, $\overline{\text{XAS}}$, XW/R, XRDY, XBLAST, XHOLD, and XHOLDA.

RESET TIMING (CONTINUED)



† High group consists of: XFCLK, $\overline{\text{HOLDA}}$
  Low group consists of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0, and TOUT1.
  Z group consists of: EA[21:2], ED[31:0], $\overline{\text{CE[3:0]}}$, $\overline{\text{BE[3:0]}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AOE}}$, $\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$, $\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, SDA10, CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, $\overline{\text{XCE[3:0]}}$, $\overline{\text{XBE[3:0]}}$/XA[5:2], $\overline{\text{XOE}}$, $\overline{\text{XRE}}$, $\overline{\text{XWE}}$/$\overline{\text{XWAIT}}$, $\overline{\text{XAS}}$, XW/R, XRDY, XBLAST, XHOLD, and XHOLDA.

‡ XD[31:0] are the boot configuration pins during device reset.

Figure 28. Reset Timing

EXTERNAL INTERRUPT TIMING

timing requirements for interrupt response cycles† (see Figure 29)

NO.			-200 MIN	-200 MAX	UNIT
2	$t_{w(ILOW)}$	Width of the interrupt pulse low	2P		ns
3	$t_{w(IHIGH)}$	Width of the interrupt pulse high	2P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

switching characteristics over recommended operating conditions during interrupt response cycles† (see Figure 29)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{R(EINTH – IACKH)}$	Response time, EXT_INTx high to IACK high	9P		ns
4	$t_{d(CKO2L-IACKV)}$	Delay time, CLKOUT2 low to IACK valid	0	10	ns
5	$t_{d(CKO2L-INUMV)}$	Delay time, CLKOUT2 low to INUMx valid	0	10	ns
6	$t_{d(CKO2L-INUMIV)}$	Delay time, CLKOUT2 low to INUMx invalid	0	10	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

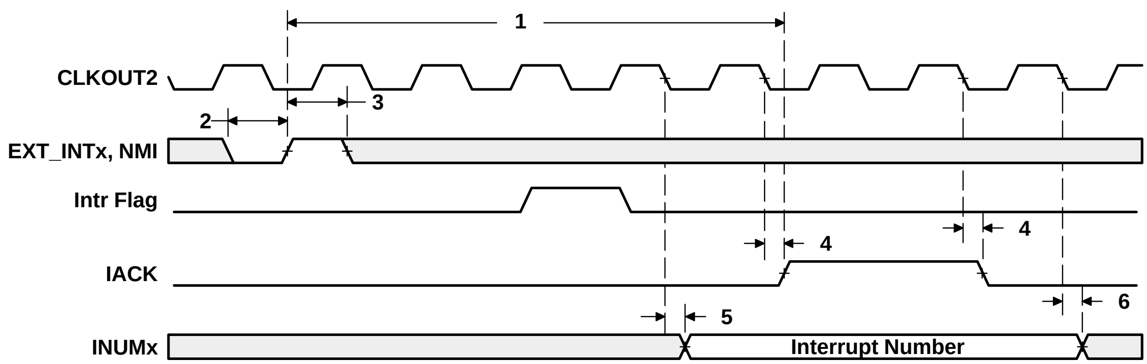


Figure 29. Interrupt Timing

ADVANCE INFORMATION

EXPANSION BUS SYNCHRONOUS FIFO TIMING

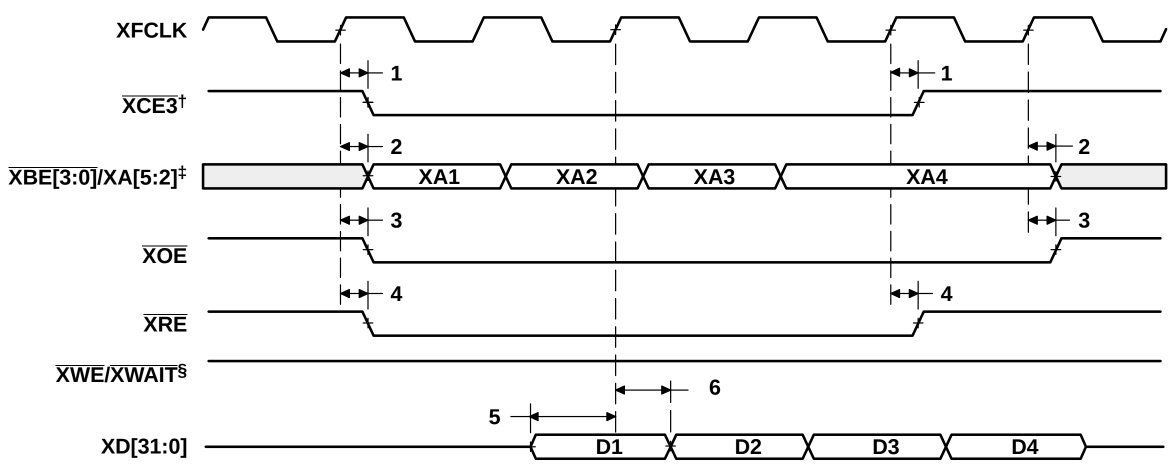
timing requirements for synchronous FIFO interface (see Figure 30, Figure 31, and Figure 32)

NO.			-200		UNIT
			MIN	MAX	
5	$t_{su(XDV-XFCKH)}$	Setup time, read XDx valid before XFCLK high	3.5		ns
6	$t_{h(XFCKH-XDV)}$	Hold time, read XDx valid after XFCLK high	2		ns

switching characteristics over recommended operating conditions for synchronous FIFO interface (see Figure 30, Figure 31, and Figure 32)

NO.	PARAMETER		-200		UNIT
			MIN	MAX	
1	$t_{d(XFCKH-XCEV)}$	Delay time, XFCLK high to $\overline{\text{XCE}}$x valid	1	7	ns
2	$t_{d(XFCKH-XAV)}$	Delay time, XFCLK high to $\overline{\text{XBE[3:0]}}$/XA[5:2] valid†	1	7	ns
3	$t_{d(XFCKH-XOEV)}$	Delay time, XFCLK high to $\overline{\text{XOE}}$ valid	1	7	ns
4	$t_{d(XFCKH-XREV)}$	Delay time, XFCLK high to $\overline{\text{XRE}}$ valid	1	7	ns
7	$t_{d(XFCKH-XWEV)}$	Delay time, XFCLK high to $\overline{\text{XWE}}$/$\overline{\text{XWAIT}}$‡ valid	1	7	ns
8	$t_{d(XFCKH-XDV)}$	Delay time, XFCLK high to XDx valid		9	ns
9	$t_{d(XFCKH-XDIV)}$	Delay time, XFCLK high to XDx invalid	1		ns

† $\overline{\text{XBE[3:0]}}$/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
‡ $\overline{\text{XWE}}$/$\overline{\text{XWAIT}}$ operates as the write-enable signal $\overline{\text{XWE}}$ during synchronous FIFO accesses.

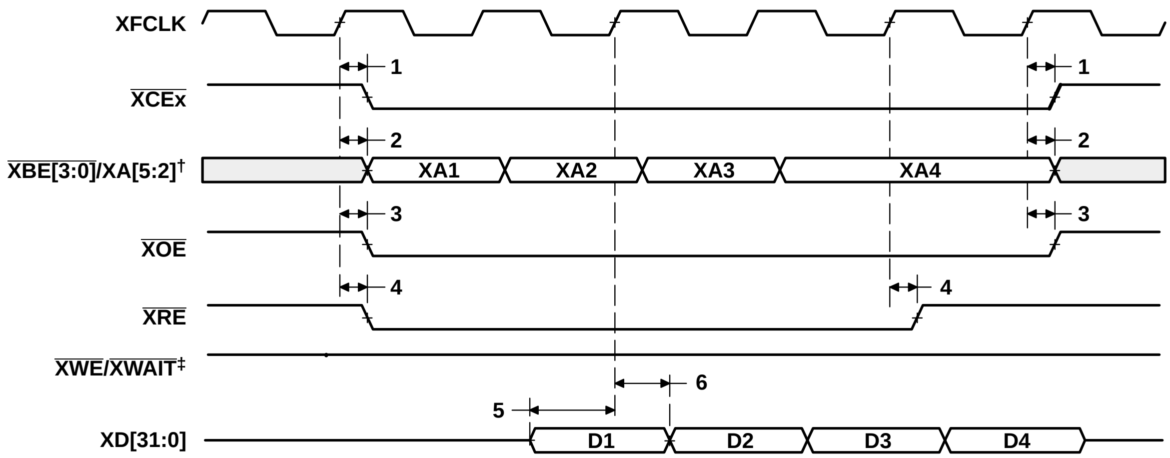


† FIFO read (glueless) mode only available in $\overline{\text{XCE3}}$.
‡ $\overline{\text{XBE[3:0]}}$/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
§ $\overline{\text{XWE}}$/$\overline{\text{XWAIT}}$ operates as the write-enable signal $\overline{\text{XWE}}$ during synchronous FIFO accesses.

Figure 30. FIFO Read Timing (Glueless Read Mode)

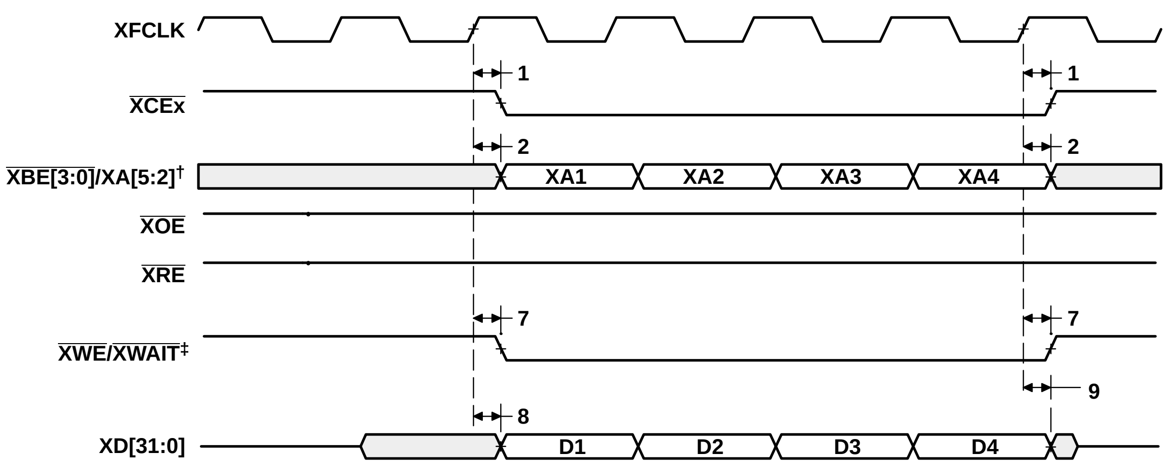
ADVANCE INFORMATION

EXPANSION BUS SYNCHRONOUS FIFO TIMING (CONTINUED)



† XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
‡ XWE/XWAIT operates as the write-enable signal XWE during synchronous FIFO accesses.

Figure 31. FIFO Read Timing



† XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
‡ XWE/XWAIT operates as the write-enable signal XWE during synchronous FIFO accesses.

Figure 32. FIFO Write Timing

EXPANSION BUS ASYNCHRONOUS PERIPHERAL TIMING

timing requirements for asynchronous peripheral cycles†‡§¶ (see Figure 33–Figure 36)

NO.			-200		UNIT
			MIN	MAX	
3	$t_{su(XDV-XREH)}$	Setup time, XDx valid before $\overline{\text{XRE}}$ high	8.5		ns
4	$t_{h(XREH-XDV)}$	Hold time, XDx valid after $\overline{\text{XRE}}$ high	1		ns
6	$t_{su(XRDYH-XREL)}$	Setup time, XRDY high before $\overline{\text{XRE}}$ low	–[(RST – 3) * P – 10]		ns
7	$t_{h(XREL-XRDYH)}$	Hold time, XRDY high after $\overline{\text{XRE}}$ low	(RST – 3) * P + 2		ns
9	$t_{su(XRDYL-XREL)}$	Setup time, XRDY low before $\overline{\text{XRE}}$ low	–[(RST – 3) * P – 6]		ns
10	$t_{h(XREL-XRDYL)}$	Hold time, XRDY low after $\overline{\text{XRE}}$ low	(RST – 3) * P + 2		ns
11	$t_{w(XRDYH)}$	Pulse width, XRDY high	2P		ns
15	$t_{su(XRDYH-XWEL)}$	Setup time, XRDY high before $\overline{\text{XWE}}$ low	–[(WST – 3) * P – 10]		ns
16	$t_{h(XWEL-XRDYH)}$	Hold time, XRDY high after $\overline{\text{XWE}}$ low	(WST – 3) * P + 2		ns
18	$t_{su(XRDYL-XWEL)}$	Setup time, XRDY low before $\overline{\text{XWE}}$ low	–[(WST – 3) * P – 6]		ns
19	$t_{h(XWEL-XRDYL)}$	Hold time, XRDY low after $\overline{\text{XWE}}$ low	(WST – 3) * P + 2		ns

† To ensure data setup time, simply program the strobe width wide enough. XRDY is internally synchronized. If XRDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, XRDY can be an asynchronous input.
‡ RS = Read Setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold. These parameters are programmed via the XBUS XCE space control registers.
§ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
¶ The sum of RS and RST (or WS and WST) must be a minimum of 4 in order to use XRDY input to extend strobe width.

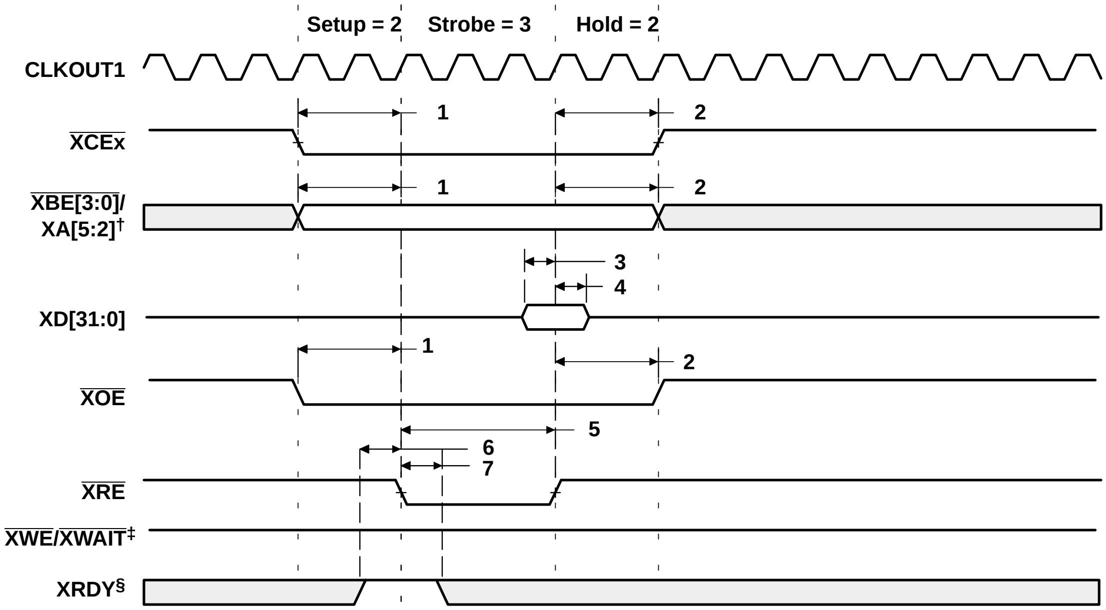
switching characteristics over recommended operating conditions for asynchronous peripheral cycles‡§¶# (see Figure 33–Figure 36)

NO.	PARAMETER		-200			UNIT
			MIN	TYP	MAX	
1	$t_{osu(SELV-XREL)}$	Output setup time, select signals valid to $\overline{\text{XRE}}$ low	RS * P – 2			ns
2	$t_{oh(XREH-SELIV)}$	Output hold time, $\overline{\text{XRE}}$ low to select signals invalid	RH * P – 2			ns
5	$t_{w(XREL)}$	Pulse width, $\overline{\text{XRE}}$ low		RST * P		ns
8	$t_{d(XRDYH-XREH)}$	Delay time, XRDY high to $\overline{\text{XRE}}$ high	3P		4P + 5	ns
12	$t_{osu(SELV-XWEL)}$	Output setup time, select signals valid to $\overline{\text{XWE}}$ low	WS * P – 2			ns
13	$t_{oh(XWEH-SELIV)}$	Output hold time, $\overline{\text{XWE}}$ low to select signals invalid	WH * P – 2			ns
14	$t_{w(XWEL)}$	Pulse width, $\overline{\text{XWE}}$ low		WST * P		ns
17	$t_{d(XRDYH-XWEH)}$	Delay time, XRDY high to $\overline{\text{XWE}}$ high	3P		4P + 5	ns

‡ RS = Read Setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold. These parameters are programmed via the XBUS XCE space control registers.
§ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
¶ The sum of RS and RST (or WS and WST) must be a minimum of 4 in order to use XRDY input to extend strobe width.
# Select signals include: $\overline{\text{XCEx}}$, $\overline{\text{XBE[3:0]}}$/XA[5:2], $\overline{\text{XOE}}$; and for writes, include XD[31:0], with the exception that $\overline{\text{XCEx}}$ can stay active for an additional 7P ns following the end of the cycle.

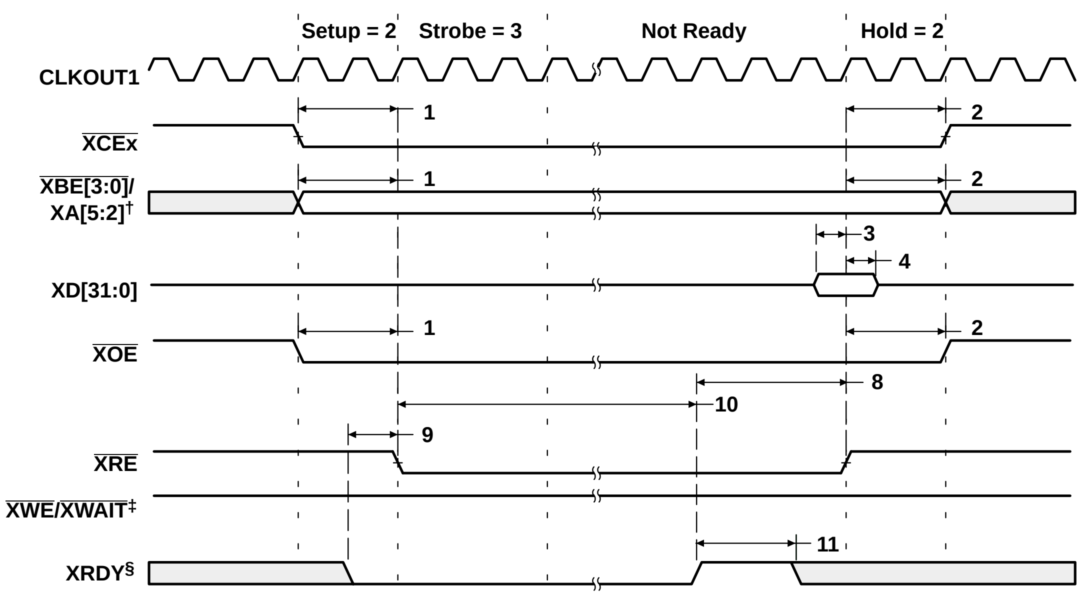
ADVANCE INFORMATION

EXPANSION BUS ASYNCHRONOUS PERIPHERAL TIMING (CONTINUED)



† XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during expansion bus asynchronous peripheral accesses.
‡ XWE/XWAIT operates as the write-enable signal XWE during expansion bus asynchronous peripheral accesses.
§ XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.

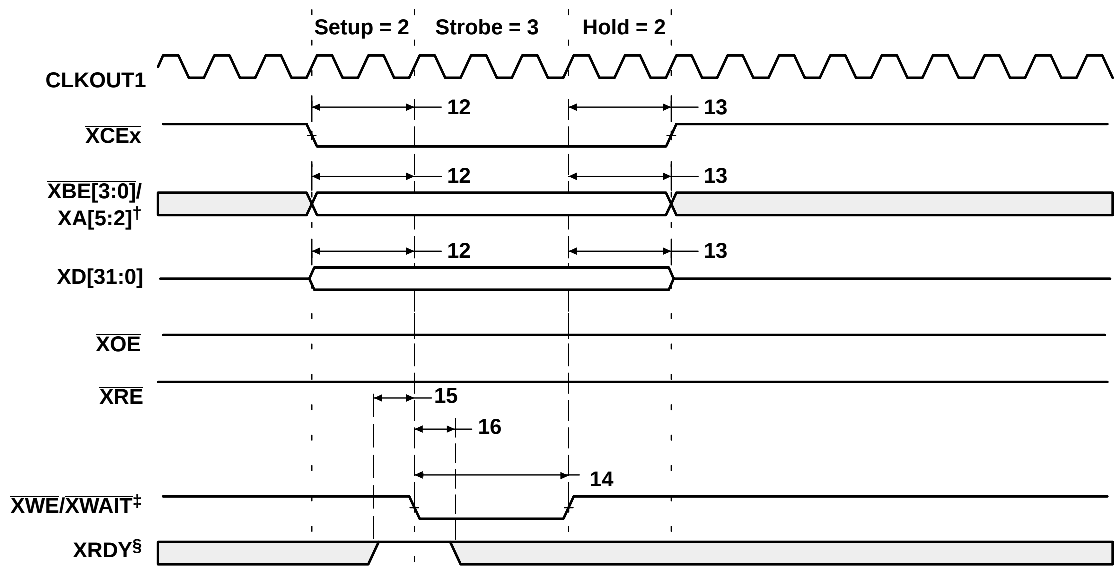
Figure 33. Expansion Bus Asynchronous Peripheral Read Timing (XRDY Not Used)



† XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during expansion bus asynchronous peripheral accesses.
‡ XWE/XWAIT operates as the write-enable signal XWE during expansion bus asynchronous peripheral accesses.
§ XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.

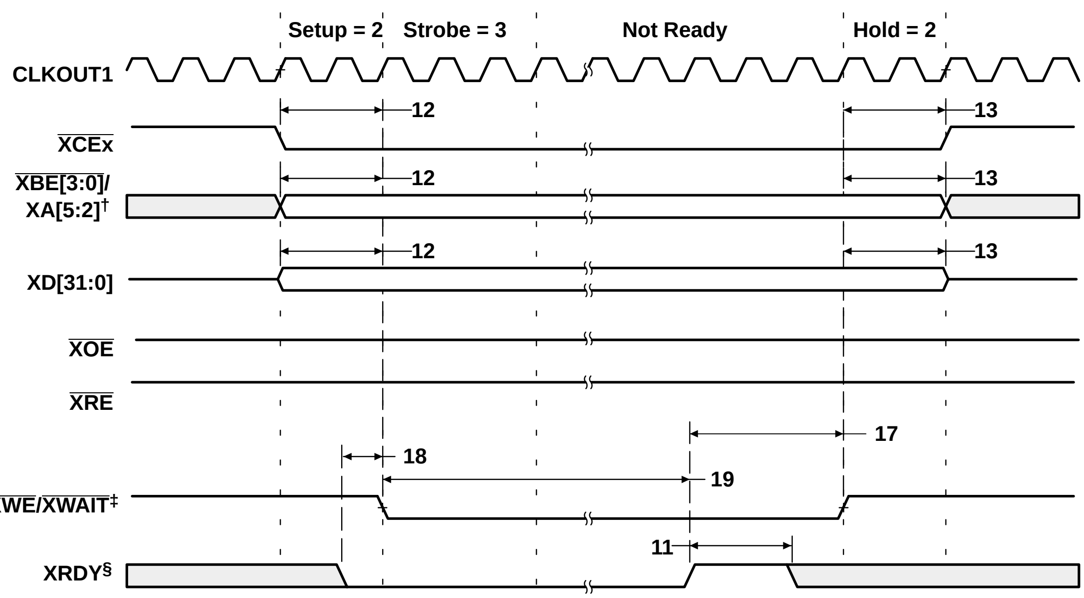
Figure 34. Expansion Bus Asynchronous Peripheral Read Timing (XRDY Used)

EXPANSION BUS ASYNCHRONOUS PERIPHERAL TIMING (CONTINUED)



† XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during expansion bus asynchronous peripheral accesses.
‡ XWE/XWAIT operates as the write-enable signal XWE during expansion bus asynchronous peripheral accesses.
§ XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.

Figure 35. Expansion Bus Asynchronous Peripheral Write Timing (XRDY Not Used)



† XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during expansion bus asynchronous peripheral accesses.
‡ XWE/XWAIT operates as the write-enable signal XWE during expansion bus asynchronous peripheral accesses.
§ XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.

Figure 36. Expansion Bus Asynchronous Peripheral Write Timing (XRDY Used)

ADVANCE INFORMATION

EXPANSION BUS SYNCHRONOUS HOST-PORT TIMING

timing requirements with external device as bus master (see Figure 37 and Figure 38)

NO.			-200 MIN	-200 MAX	UNIT
1	$t_{su(XCSV-XCKIH)}$	Setup time, $\overline{XCS}$ valid before XCLKIN high	3.5		ns
2	$t_{h(XCKIH-XCS)}$	Hold time, $\overline{XCS}$ valid after XCLKIN high	2.8		ns
3	$t_{su(XAS-XCKIH)}$	Setup time, $\overline{XAS}$ valid before XCLKIN high	3.5		ns
4	$t_{h(XCKIH-XAS)}$	Hold time, $\overline{XAS}$ valid after XCLKIN high	2.8		ns
5	$t_{su(XCTL-XCKIH)}$	Setup time, XCNTL valid before XCLKIN high	3.5		ns
6	$t_{h(XCKIH-XCTL)}$	Hold time, XCNTL valid after XCLKIN high	2.8		ns
7	$t_{su(XWR-XCKIH)}$	Setup time, XW/R valid before XCLKIN high†	3.5		ns
8	$t_{h(XCKIH-XWR)}$	Hold time, XW/R valid after XCLKIN high†	2.8		ns
9	$t_{su(XBLTV-XCKIH)}$	Setup time, XBLAST valid before XCLKIN high‡	3.5		ns
10	$t_{h(XCKIH-XBLTV)}$	Hold time, XBLAST valid after XCLKIN high‡	2.8		ns
16	$t_{su(XBEV-XCKIH)}$	Setup time, $\overline{XBE[3:0]}$/XA[5:2] valid before XCLKIN high§	3.5		ns
17	$t_{h(XCKIH-XBEV)}$	Hold time, $\overline{XBE[3:0]}$/XA[5:2] valid after XCLKIN high§	2.8		ns
18	$t_{su(XD-XCKIH)}$	Setup time, XDx valid before XCLKIN high	3.5		ns
19	$t_{h(XCKIH-XD)}$	Hold time, XDx valid after XCLKIN high	2.8		ns

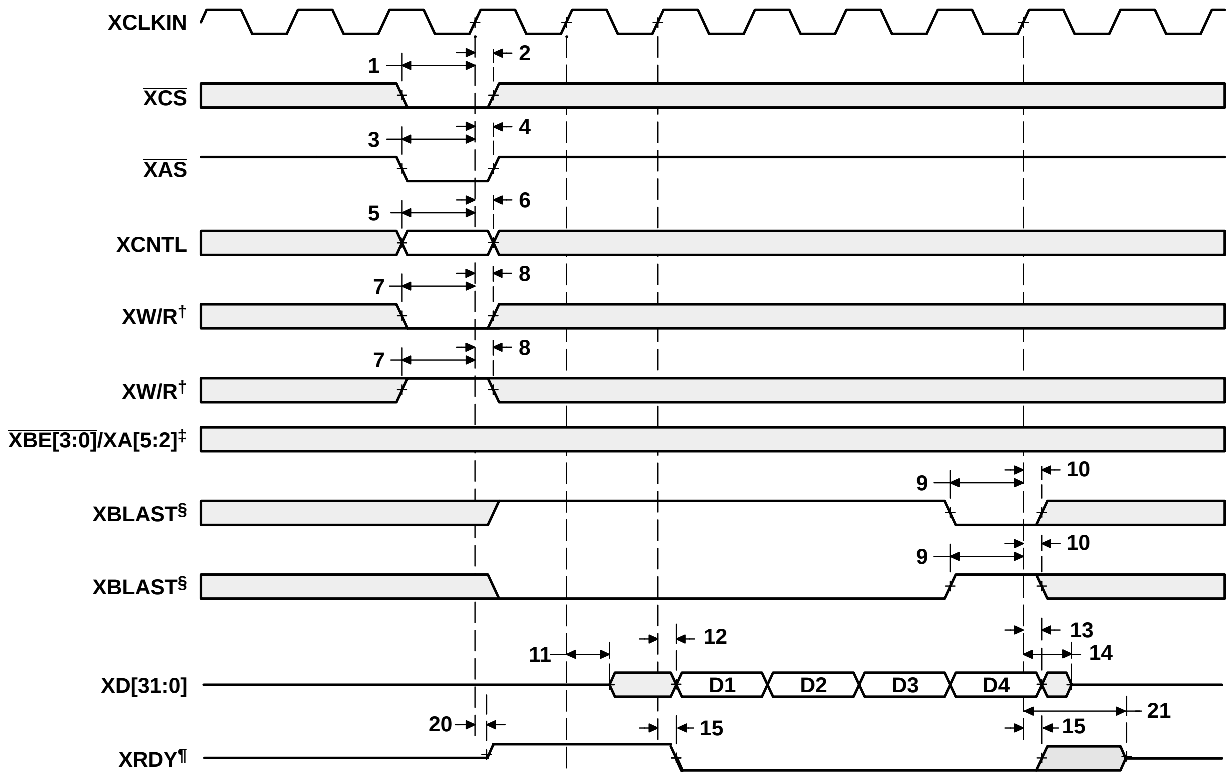
† XW/R input/output polarity selected at boot.
‡ XBLAST input polarity selected at boot.
§ $\overline{XBE[3:0]}$/XA[5:2] operate as byte-enables $\overline{XBE[3:0]}$ during host-port accesses.

switching characteristics over recommended operating conditions with external device as bus master¶ (see Figure 37 and Figure 38)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
11	$t_{d(XCKIH-XDLZ)}$	Delay time, XCLKIN high to XDx low impedance	0		ns
12	$t_{d(XCKIH-XDV)}$	Delay time, XCLKIN high to XDx valid		16.5	ns
13	$t_{d(XCKIH-XDIV)}$	Delay time, XCLKIN high to XDx invalid	5		ns
14	$t_{d(XCKIH-XDHZ)}$	Delay time, XCLKIN high to XDx high impedance		4P	ns
15	$t_{d(XCKIH-XRY)}$	Delay time, XCLKIN high to XRDY invalid#	5	16.5	ns
20	$t_{d(XCKIH-XRYLZ)}$	Delay time, XCLKIN high to XRDY low impedance	5	16.5	ns
21	$t_{d(XCKIH-XRYHZ)}$	Delay time, XCLKIN high to XRDY high impedance#	2P + 5	3P + 16.5	ns

¶ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
# XRDY operates as active-low ready input/output during host-port accesses.

EXPANSION BUS SYNCHRONOUS HOST-PORT TIMING (CONTINUED)

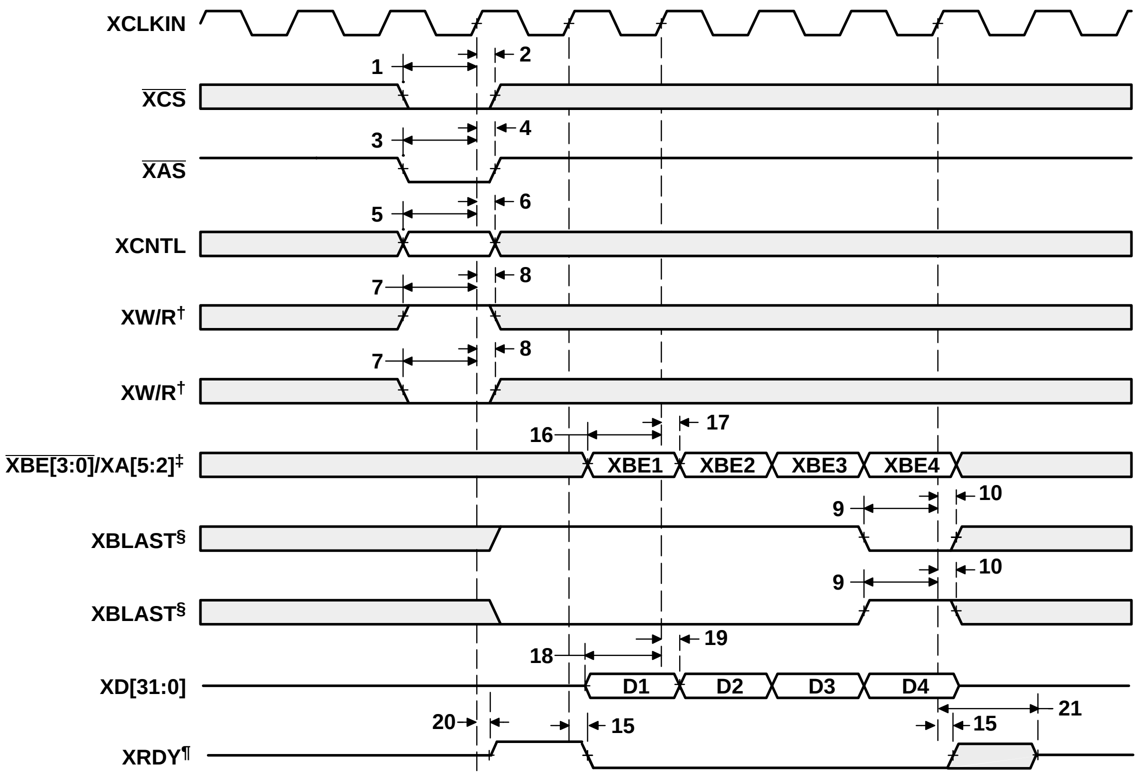


† XW/R input/output polarity selected at boot
‡ XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
§ XBLAST input polarity selected at boot
¶ XRDY operates as active-low ready input/output during host-port accesses.

Figure 37. External Host as Bus Master—Read

ADVANCE INFORMATION

EXPANSION BUS SYNCHRONOUS HOST-PORT TIMING (CONTINUED)



† XW/R input/output polarity selected at boot
‡ XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
§ XBLAST input polarity selected at boot
¶ XRDY operates as active-low ready input/output during host-port accesses.

Figure 38. External Host as Bus Master—Write

ADVANCE INFORMATION

EXPANSION BUS SYNCHRONOUS HOST-PORT TIMING (CONTINUED)

timing requirements with C62x™ as bus master (see Figure 39, Figure 40, and Figure 41)

NO.			-200		UNIT
			MIN	MAX	
9	$t_{su(XDV-XCKIH)}$	Setup time, XDx valid before XCLKIN high	3.5		ns
10	$t_{h(XCKIH-XDV)}$	Hold time, XDx valid after XCLKIN high	2.8		ns
11	$t_{su(XRY-XCKIH)}$	Setup time, XRDY valid before XCLKIN high†	3.5		ns
12	$t_{h(XCKIH-XRY)}$	Hold time, XRDY valid after XCLKIN high†	2.8		ns
14	$t_{su(XBFF-XCKIH)}$	Setup time, XBOFF valid before XCLKIN high	3.5		ns
15	$t_{h(XCKIH-XBFF)}$	Hold time, XBOFF valid after XCLKIN high	2.8		ns

† XRDY operates as active-low ready input/output during host-port accesses.

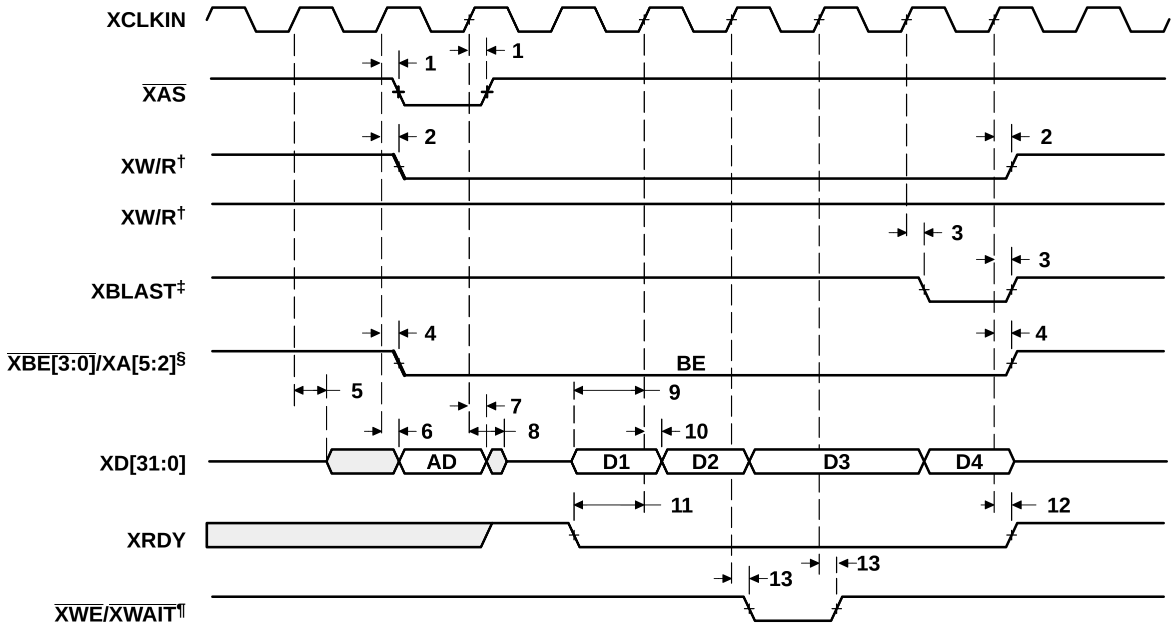
switching characteristics over recommended operating conditions with C62x™ as bus master (see Figure 39, Figure 40, and Figure 41)

NO.	PARAMETER		-200		UNIT
			MIN	MAX	
1	$t_{d(XCKIH-XASV)}$	Delay time, XCLKIN high to $\overline{XAS}$ valid	5	16.5	ns
2	$t_{d(XCKIH-XWRV)}$	Delay time, XCLKIN high to XW/R valid‡	5	16.5	ns
3	$t_{d(XCKIH-XBLTV)}$	Delay time, XCLKIN high to XBLAST valid§	5	16.5	ns
4	$t_{d(XCKIH-XBEV)}$	Delay time, XCLKIN high to $\overline{XBE[3:0]}$/XA[5:2] valid¶	5	16.5	ns
5	$t_{d(XCKIH-XDLZ)}$	Delay time, XCLKIN high to XDx low impedance	0		ns
6	$t_{d(XCKIH-XDV)}$	Delay time, XCLKIN high to XDx valid		16.5	ns
7	$t_{d(XCKIH-XDIV)}$	Delay time, XCLKIN high to XDx invalid	5		ns
8	$t_{d(XCKIH-XDHZ)}$	Delay time, XCLKIN high to XDx high impedance		4P	ns
13	$t_{d(XCKIH-XWTV)}$	Delay time, XCLKIN high to $\overline{XWE}$/$\overline{XWAIT}$ valid#	5	16.5	ns

‡ XW/R input/output polarity selected at boot.
§ XBLAST output polarity is always active low.
¶ $\overline{XBE[3:0]}$/XA[5:2] operate as byte-enables $\overline{XBE[3:0]}$ during host-port accesses.
# $\overline{XWE}$/$\overline{XWAIT}$ operates as $\overline{XWAIT}$ output signal during host-port accesses.

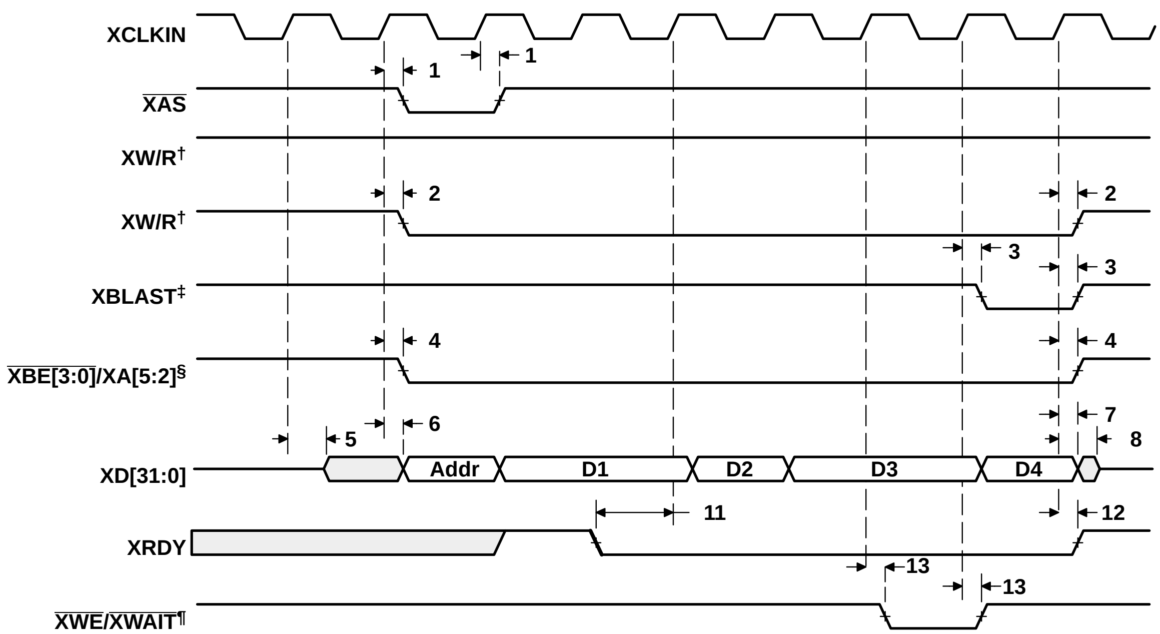
ADVANCE INFORMATION

EXPANSION BUS SYNCHRONOUS HOST-PORT TIMING (CONTINUED)



† XW/R input/output polarity selected at boot
‡ XBLAST output polarity is always active low.
§ XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
¶ XWE/XWAIT operates as XWAIT output signal during host-port accesses.

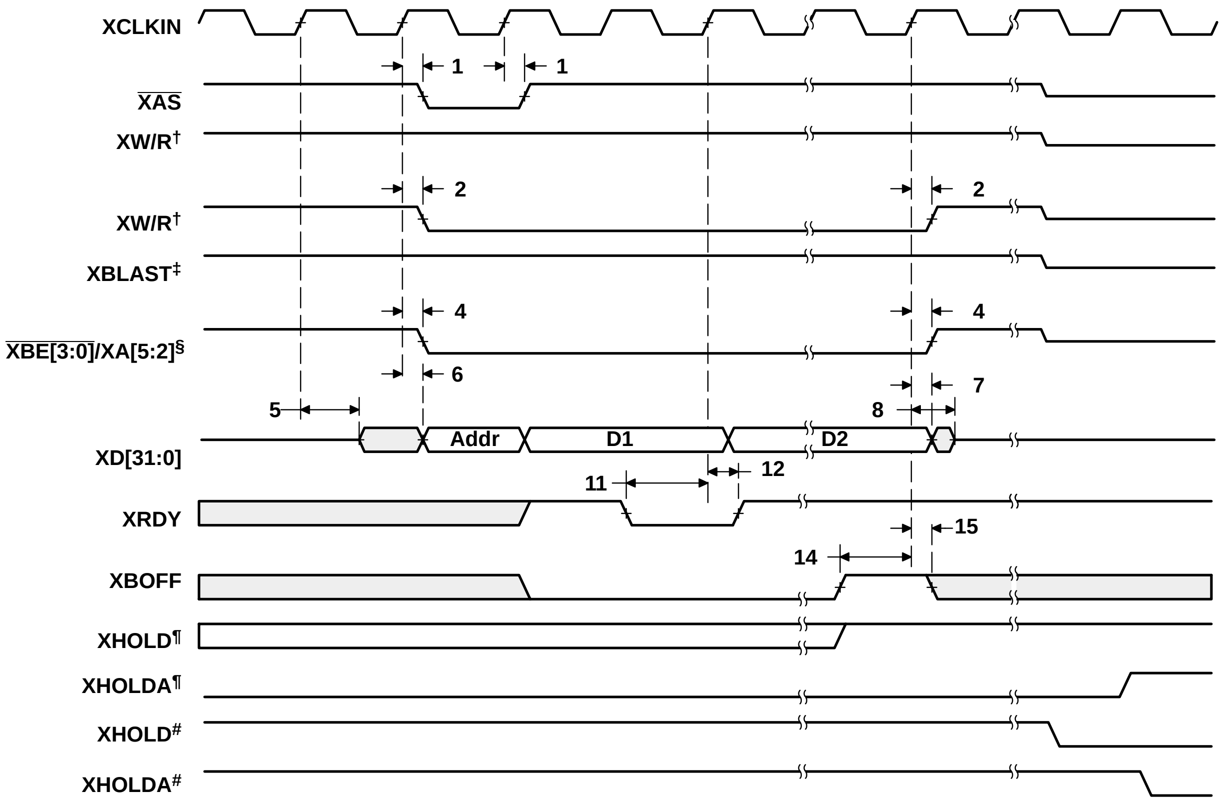
Figure 39. C62x™ as Bus Master—Read



† XW/R input/output polarity selected at boot
‡ XBLAST output polarity is always active low.
§ XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
¶ XWE/XWAIT operates as XWAIT output signal during host-port accesses.

Figure 40. C62x™ as Bus Master—Write

EXPANSION BUS SYNCHRONOUS HOST-PORT TIMING (CONTINUED)



† XW/R input/output polarity selected at boot
‡ XBLAST output polarity is always active low.
§ XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
¶ Internal arbiter enabled
# External arbiter enabled
|| This diagram illustrates XBOFF timing. Bus arbitration timing is shown in Figure 44 and Figure 45.

Figure 41. C62x™ as Bus Master—BOFF Operation||

ADVANCE INFORMATION

EXPANSION BUS ASYNCHRONOUS HOST-PORT TIMING

timing requirements with external device as asynchronous bus master† (see Figure 42 and Figure 43)

NO.			-200 MIN	-200 MAX	UNIT
1	$t_{w(XCSL)}$	Pulse duration, $\overline{\text{XCS}}$ low	4P		ns
2	$t_{w(XCSH)}$	Pulse duration, $\overline{\text{XCS}}$ high	4P		ns
3	$t_{su(XSEL-XCSL)}$	Setup time, expansion bus select signals‡ valid before $\overline{\text{XCS}}$ low	1		ns
4	$t_{h(XCSL-XSEL)}$	Hold time, expansion bus select signals‡ valid after $\overline{\text{XCS}}$ low	3		ns
10	$t_{h(XRYL-XCSL)}$	Hold time, $\overline{\text{XCS}}$ low after XRDY low	P + 1.5		ns
11	$t_{su(XBEV-XCSH)}$	Setup time, $\overline{\text{XBE[3:0]}}$/XA[5:2] valid before $\overline{\text{XCS}}$ high§	1		ns
12	$t_{h(XCSH-XBEV)}$	Hold time, $\overline{\text{XBE[3:0]}}$/XA[5:2] valid after $\overline{\text{XCS}}$ high§	3		ns
13	$t_{su(XDV-XCSH)}$	Setup time, XDx valid before $\overline{\text{XCS}}$ high	1		ns
14	$t_{h(XCSH-XDV)}$	Hold time, XDx valid after $\overline{\text{XCS}}$ high	3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ Expansion bus select signals include XCNTL and XR/W.
§ $\overline{\text{XBE[3:0]}}$/XA[5:2] operate as byte-enables $\overline{\text{XBE[3:0]}}$ during host-port accesses.

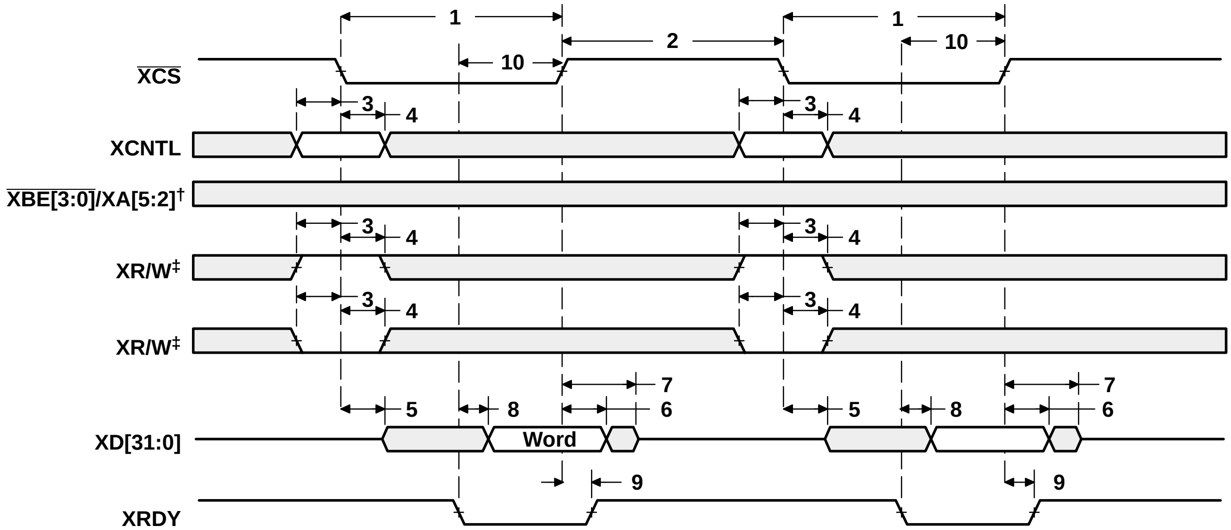
switching characteristics over recommended operating conditions with external device as asynchronous bus master† (see Figure 42 and Figure 43)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
5	$t_{d(XCSL-XDLZ)}$	Delay time, $\overline{\text{XCS}}$ low to XDx low impedance	0		ns
6	$t_{d(XCSH-XDIV)}$	Delay time, $\overline{\text{XCS}}$ high to XDx invalid	0	12	ns
7	$t_{d(XCSH-XDHZ)}$	Delay time, $\overline{\text{XCS}}$ high to XDx high impedance		4P	ns
8	$t_{d(XRYL-XDV)}$	Delay time, XRDY low to XDx valid		1	ns
9	$t_{d(XCSH-XRYH)}$	Delay time, $\overline{\text{XCS}}$ high to XRDY high	0	12	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

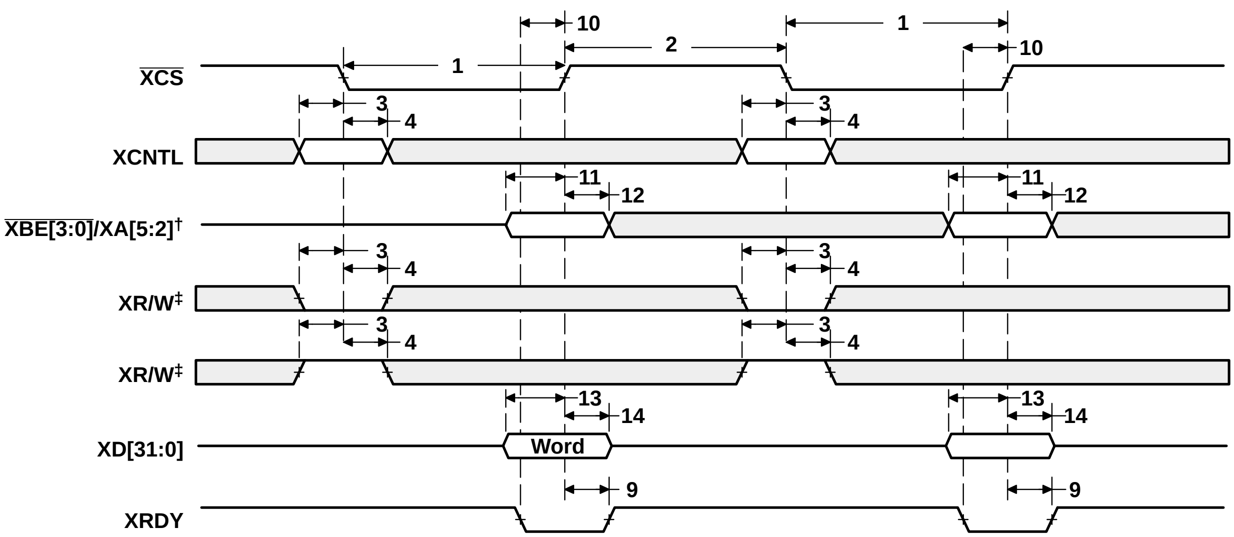
ADVANCE INFORMATION

EXPANSION BUS ASYNCHRONOUS HOST-PORT TIMING (CONTINUED)



† XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
‡ XW/R input/output polarity selected at boot

Figure 42. External Device as Asynchronous Master—Read



† XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
‡ XW/R input/output polarity selected at boot

Figure 43. External Device as Asynchronous Master—Write

ADVANCE INFORMATION

XHOLD/XHOLDA TIMING

timing requirements for expansion bus arbitration (internal arbiter enabled)† (see Figure 44)

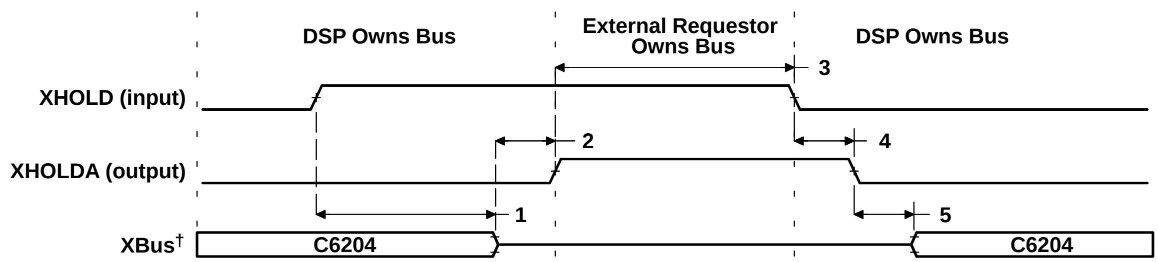
NO.			-200 MIN	-200 MAX	UNIT
3	$t_{oh(XHDAH-XHDH)}$	Output hold time, XHOLD high after XHOLDA high	P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

switching characteristics over recommended operating conditions for expansion bus arbitration (internal arbiter enabled)†‡ (see Figure 44)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{d(XHDH-XBHZ)}$	Delay time, XHOLD high to XBus high impedance	3P	§	ns
2	$t_{d(XBHZ-XHDAH)}$	Delay time, XBus high impedance to XHOLDA high	0	2P	ns
4	$t_{d(XHDL-XHDAL)}$	Delay time, XHOLD low to XHOLDA low	3P		ns
5	$t_{d(XHDAL-XBLZ)}$	Delay time, XHOLDA low to XBus low impedance	0	2P	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ XBus consists of $\overline{\text{XBE[3:0]}}$/XA[5:2], $\overline{\text{XAS}}$, XW/R, and XBLAST.
§ All pending XBus transactions are allowed to complete before XHOLDA is asserted.



† XBus consists of $\overline{\text{XBE[3:0]}}$/XA[5:2], $\overline{\text{XAS}}$, XW/R, and XBLAST.

Figure 44. Expansion Bus Arbitration—Internal Arbiter Enabled

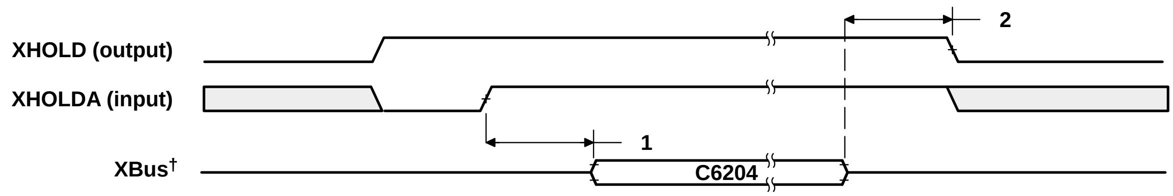
ADVANCE INFORMATION

XHOLD/XHOLDA TIMING (CONTINUED)

switching characteristics over recommended operating conditions for expansion bus arbitration (internal arbiter disabled)† (see Figure 45)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{d(XHDAH-XBLZ)}$	Delay time, XHOLDA high to XBus low impedance‡	2P	2P + 10	ns
2	$t_{d(XBHZ-XHDL)}$	Delay time, XBus high impedance to XHOLD low‡	0	2P	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ XBus consists of $\overline{XBE[3:0]}$/XA[5:2], $\overline{XAS}$, XW/R, and XBLAST.



† XBus consists of $\overline{XBE[3:0]}$/XA[5:2], $\overline{XAS}$, XW/R, and XBLAST.

Figure 45. Expansion Bus Arbitration—Internal Arbiter Disabled

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING

timing requirements for McBSP†‡ (see Figure 46)

NO.				-200		UNIT
				MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P§		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P–1¶		ns
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	9		ns
			CLKR ext	2		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		ns
			CLKR ext	3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	8		ns
			CLKR ext	0.5		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	4		ns
			CLKR ext	3		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	9		ns
			CLKX ext	2		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		ns
			CLKX ext	3		

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ The maximum bit rate for the C6204 devices is 100 Mbps or CPU/2 (the slower of the two). Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 100 MHz; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 10 ns (100 MHz), whichever value is larger. For example, when running parts at 200 MHz (P = 5 ns), use 10 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 100 MHz (P = 10 ns), use 2P = 20 ns (50 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.
¶ The minimum CLKR/X pulse duration is either (P–1) or 4 ns, whichever is larger. For example, when running parts at 200 MHz (P = 5 ns), use 4 ns as the minimum CLKR/X pulse duration. When running parts at 100 MHz (P = 10 ns), use (P–1) = 9 ns as the minimum CLKR/X pulse duration.

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP†‡ (see Figure 46)

NO.	PARAMETER			-200		UNIT
				MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		3	12	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P–2§¶		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C – 2#	C + 2#	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	–3	3	ns
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	–3	3	ns
			CLKX ext	3	9	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	–1	5	ns
			CLKX ext	2	9	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	–1	4	ns
			CLKX ext	2	11	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode.	FSX int	–1	5	ns
			FSX ext	2	12	

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ Minimum delay times also represent minimum output hold times.
§ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
¶ The maximum bit rate for the C6204 devices is 100 Mbps or CPU/2 (the slower of the two). Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 100 MHz; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 10 ns (100 MHz), whichever value is larger. For example, when running parts at 200 MHz (P = 5 ns), use 10 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 100 MHz (P = 10 ns), use 2P = 20 ns (50 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.
# C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 100-MHz limit.

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

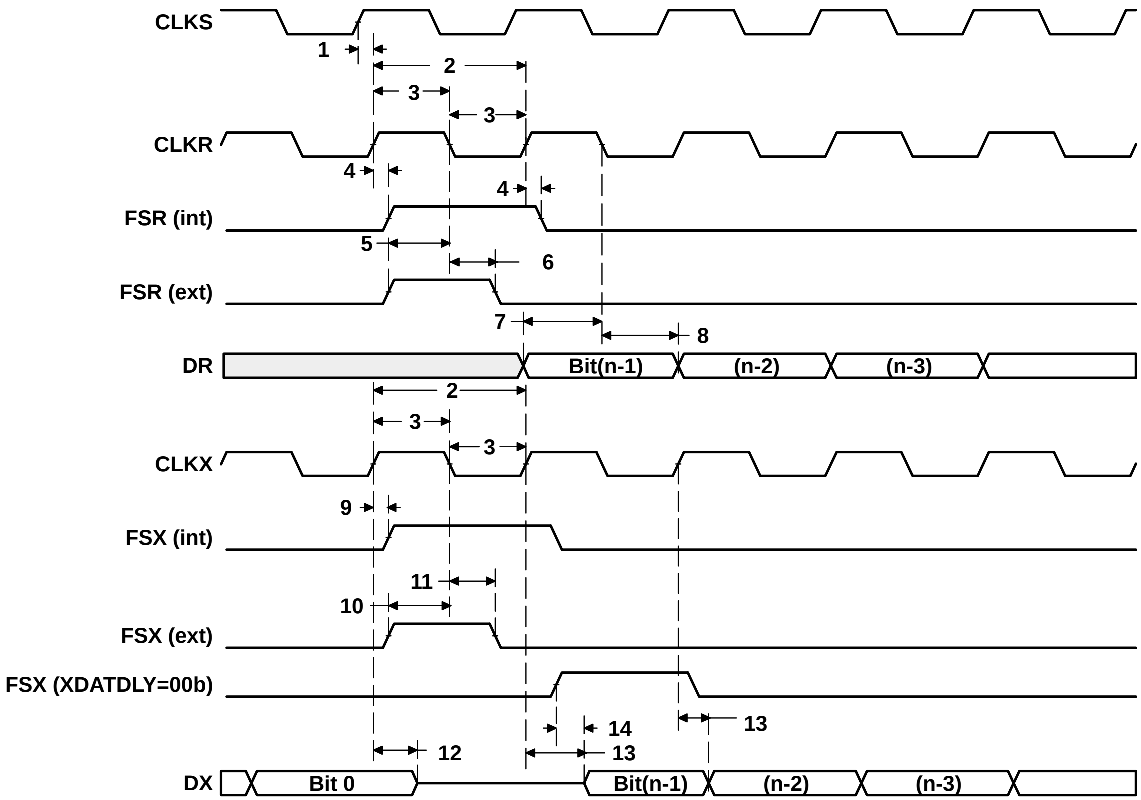


Figure 46. McBSP Timings

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for FSR when GSYNC = 1 (see Figure 47)

NO.			-200 MIN	-200 MAX	UNIT
1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high	4		ns
2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high	4		ns

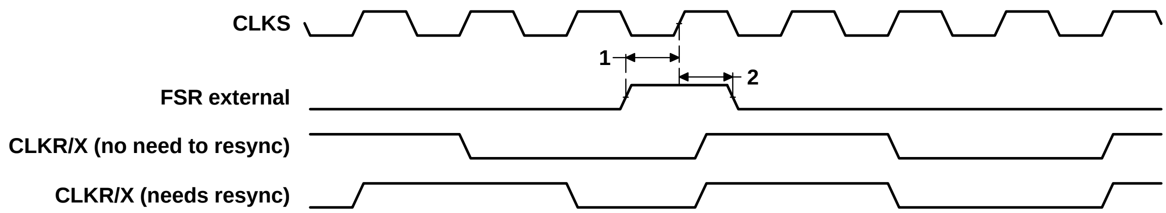


Figure 47. FSR Timing When GSYNC = 1

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0†‡ (see Figure 48)

NO.			-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	12		2 – 3P		ns
5	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	4		6 + 6P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0†‡ (see Figure 48)

NO.	PARAMETER		-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶	T – 3	T + 5			ns
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	L – 4	L + 5			ns
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	–4	5	3P + 3	5P + 17	ns
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	L – 2	L + 3			ns
7	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			P + 3	3P + 17	ns
8	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			2P + 2	4P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 100-MHz limit.
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

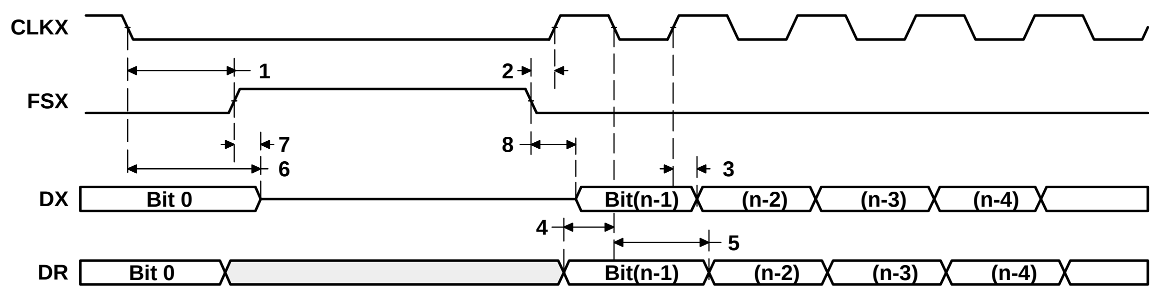


Figure 48. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 49)

NO.			-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 – 3P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 6P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 49)

NO.	PARAMETER		-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶	L – 2	L + 3			ns
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	T – 2	T + 3			ns
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	–2	4	3P + 4	5P + 17	ns
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	–2	4	3P + 3	5P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	H – 2	H + 4	2P + 2	4P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 100-MHz limit.
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

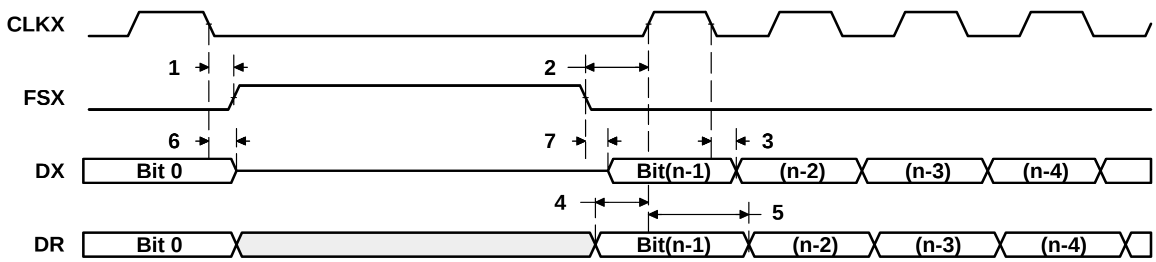


Figure 49. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 50)

NO.			-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 – 3P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 6P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 50)

NO.	PARAMETER		-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high¶	T – 2	T + 3			ns
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#	H – 2	H + 3			ns
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	–2	4	3P + 4	5P + 17	ns
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	H – 2	H + 3			ns
7	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			P + 3	3P + 17	ns
8	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			2P + 2	4P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 100-MHz limit.
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

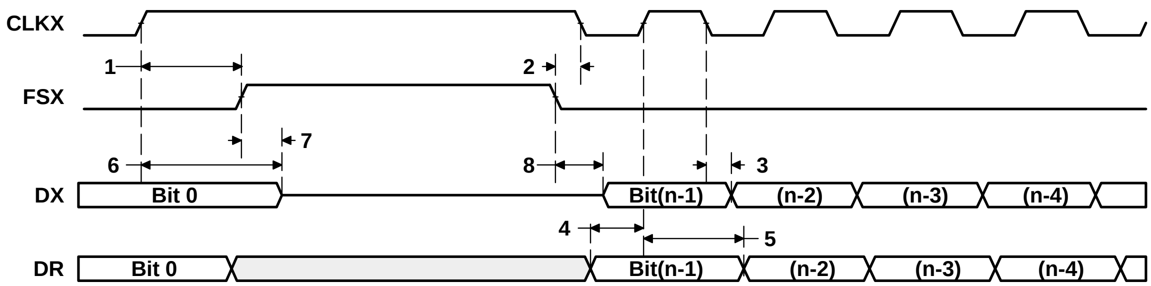


Figure 50. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 51)

NO.			-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	12		2 – 3P		ns
5	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	4		5 + 6P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 51)

NO.	PARAMETER		-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high¶	H – 2	H + 3			ns
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#	T – 2	T + 1			ns
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	–2	4	3P + 4	5P + 17	ns
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	–2	4	3P + 3	5P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	L – 2	L + 4	2P + 2	4P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
  = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
  T = CLKX period = (1 + CLKGDV) * S
  H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
  = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
  L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
  = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
  CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 100-MHz limit.
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
  CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
  CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

ADVANCE INFORMATION

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

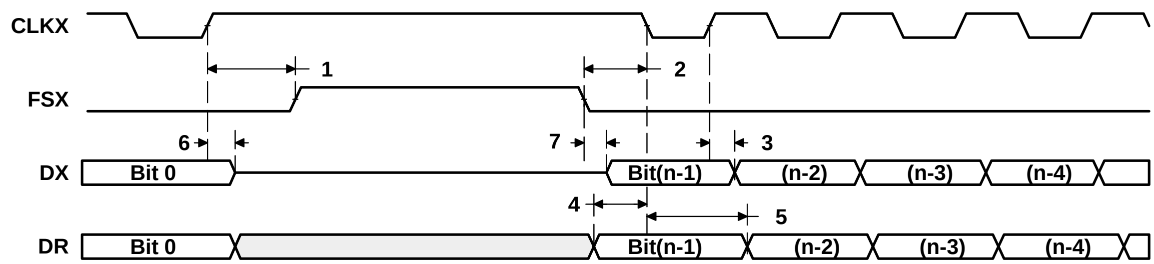


Figure 51. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

ADVANCE INFORMATION

DMAC, TIMER, POWER-DOWN TIMING

switching characteristics over recommended operating conditions for DMAC outputs† (see Figure 52)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
1	$t_{w(DMACH)}$	Pulse duration, DMAC high	2P – 3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

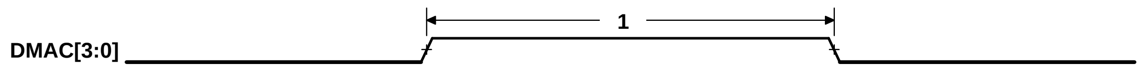


Figure 52. DMAC Timing

timing requirements for timer inputs† (see Figure 53)

NO.			-200 MIN	-200 MAX	UNIT
1	$t_{w(TINPH)}$	Pulse duration, TINP high	2P		ns
2	$t_{w(TINPL)}$	Pulse duration, TINP low	2P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

switching characteristics over recommended operating conditions for timer outputs† (see Figure 53)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
3	$t_{w(TOUTH)}$	Pulse duration, TOUT high	2P – 3		ns
4	$t_{w(TOUTL)}$	Pulse duration, TOUT low	2P – 3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

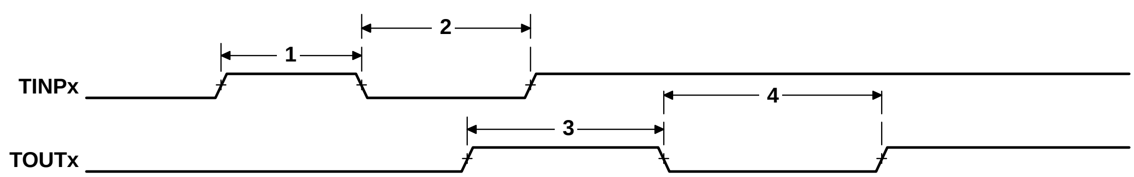


Figure 53. Timer Timing

DMAC, TIMER, POWER-DOWN TIMING (CONTINUED)

switching characteristics over recommended operating conditions for power-down outputs† (see Figure 54)

NO.	PARAMETER		-200		UNIT
			MIN	MAX	
1	$t_{w(PDH)}$	Pulse duration, PD high	2P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

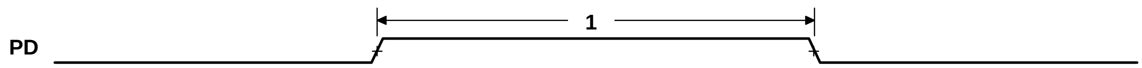


Figure 54. Power-Down Timing

ADVANCE INFORMATION

JTAG TEST-PORT TIMING

timing requirements for JTAG test port (see Figure 55)

NO.			-200 MIN	-200 MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	35		ns
3	$t_{su(TDIV-TCKH)}$	Setup time, TDI/TMS/$\overline{\text{TRST}}$ valid before TCK high	11		ns
4	$t_{h(TCKH-TDIV)}$	Hold time, TDI/TMS/$\overline{\text{TRST}}$ valid after TCK high	9		ns

switching characteristics over recommended operating conditions for JTAG test port (see Figure 55)

NO.	PARAMETER		-200 MIN	-200 MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	–4.5	12	ns

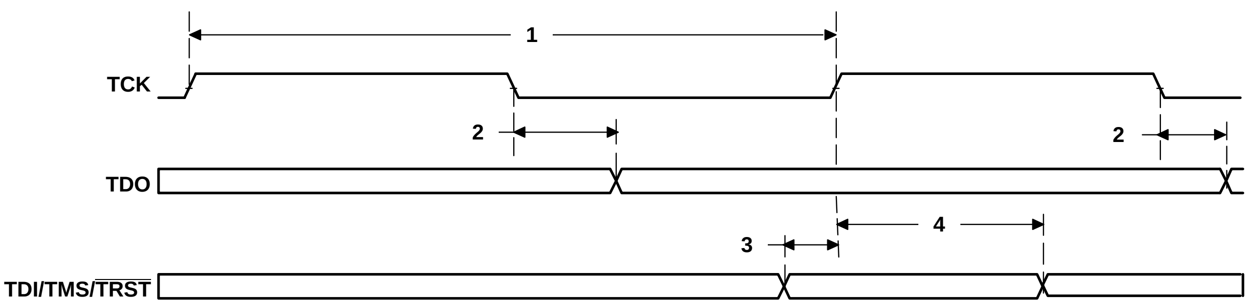
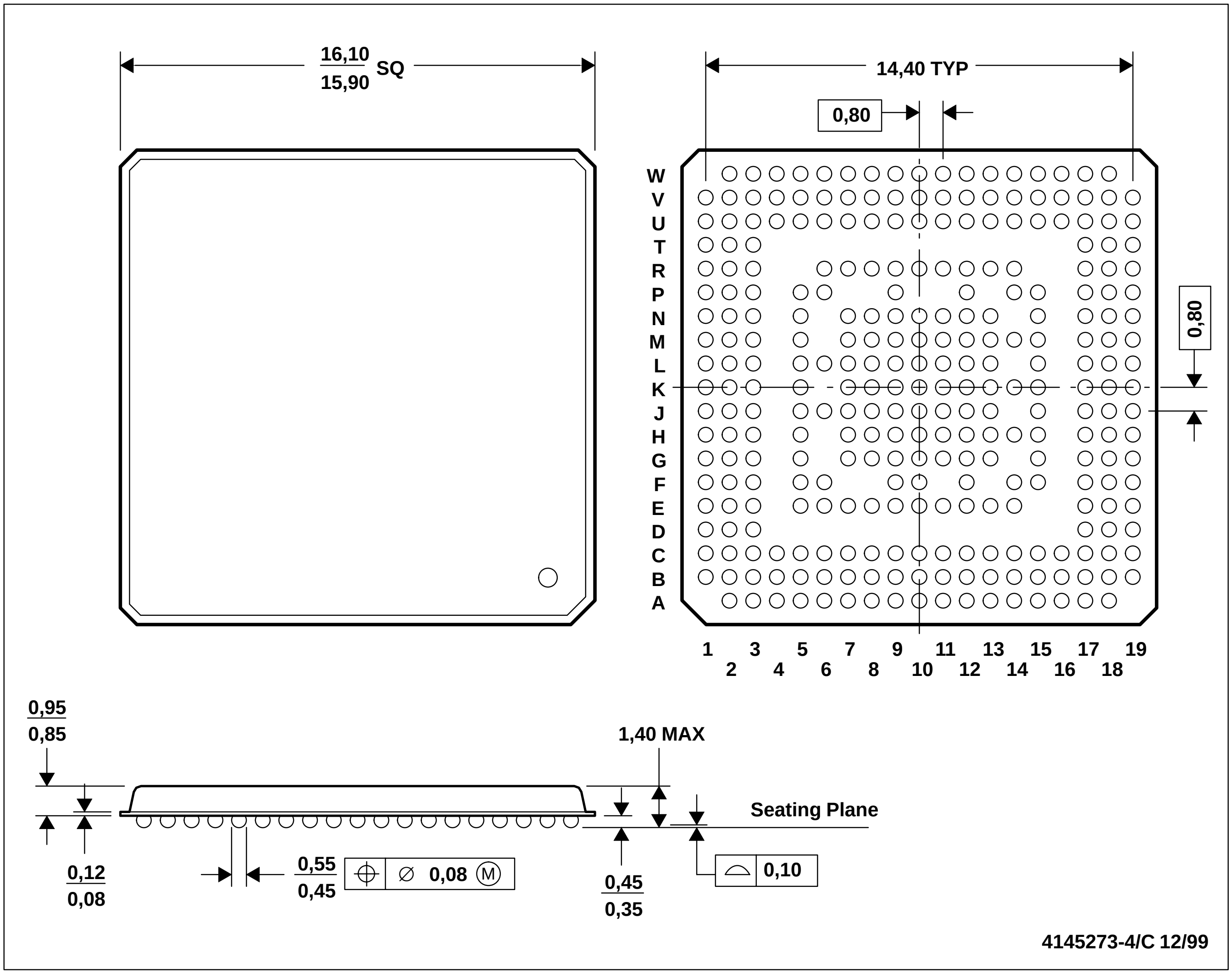


Figure 55. JTAG Test-Port Timing

ADVANCE INFORMATION

MECHANICAL DATA

GHK (S-PBGA-N288) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

ADVANCE INFORMATION

thermal resistance characteristics (S-PBGA package)

NO			°C/W	Air Flow (m/s†)
1	$R\Theta_{JC}$	Junction-to-case	9.5	N/A
2	$R\Theta_{JA}$	Junction-to-free air	26.5	0.00
3	$R\Theta_{JA}$	Junction-to-free air	23.9	0.50
4	$R\Theta_{JA}$	Junction-to-free air	22.6	1.00
5	$R\Theta_{JA}$	Junction-to-free air	21.3	2.00

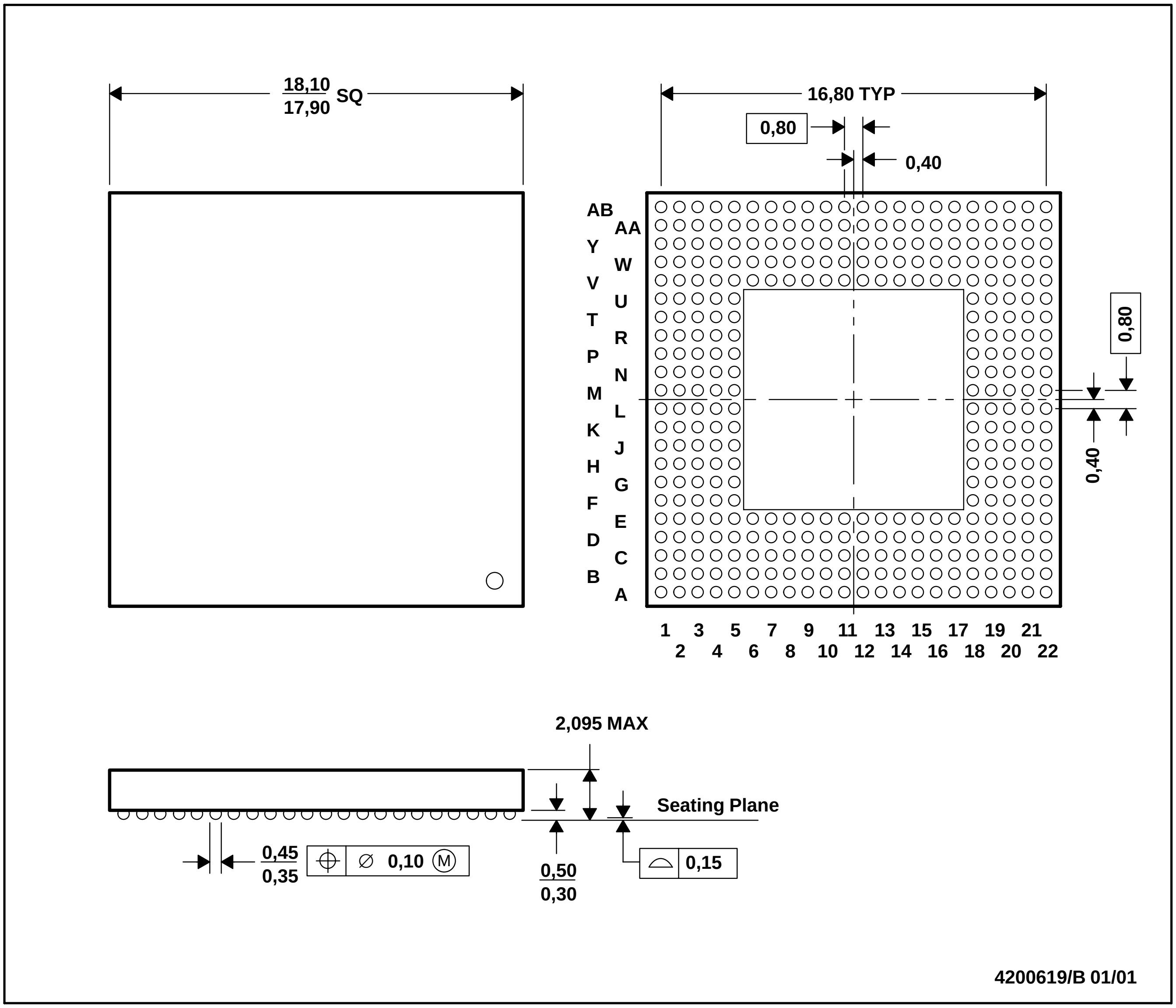
† m/s = meters per second

MicroStar BGA is a trademark of Texas Instruments.

ADVANCE INFORMATION

MECHANICAL DATA

GLW (S-PBGA-N340) **PLASTIC BALL GRID ARRAY (CAVITY DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

thermal resistance characteristics (S-PBGA package)

NO		°C/W	Air Flow (m/s†)
1	$R\Theta_{JC}$ Junction-to-case	11.7	N/A
2	$R\Theta_{JA}$ Junction-to-free air	14.2	0.00
3	$R\Theta_{JA}$ Junction-to-free air	12.3	0.50
4	$R\Theta_{JA}$ Junction-to-free air	10.9	1.00
5	$R\Theta_{JA}$ Junction-to-free air	9.3	2.00

† m/s = meters per second

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