FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16702-4E

32-bit Microcontrollers

CMOS

FR60Lite MB91265A Series

MB91267A/267NA/F267A/F267NA/V265A

■ DESCRIPTION

The MB91265A series is a 32-bit RISC microcontroller designed by Fujitsu for embedded control applications which require high-speed processing.
The CPU is used the FR family* and the compatibility of FR60Lite.
MB91267NA/F267NA loads the C-CAN (1 channel) .

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURES

- FR60Lite CPU
  - 32-bit RISC, load/store architecture with a five-stage pipeline
  - Maximum operating frequency : 33 MHz (oscillation frequency 4.192 MHz, oscillation frequency 8-multiplier (PLL clock multiplication method)
  - 16-bit fixed length instructions (basic instructions)
  - Execution speed of instructions : 1 instruction per cycle
  - Memory-to-memory transfer, bit handling, barrel shift instructions, etc. : Instructions suitable for embedded applications
  - Function entry/exit instructions, multiple-register load/store instructions : Instructions adapted for C-language
  - Register interlock function : Facilitates coding in assembler.
  - Built-in multiplier with instruction-level support
    - 32-bit multiplication with sign : 5 cycles
    - 16-bit multiplication with sign : 3 cycles
  - Interrupt (PC, PS save) : 6 cycles, 16 priority levels
  - Harvard architecture allowing program access and data access to be executed simultaneously
  - Instruction compatible with FR family

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

FUJITSU

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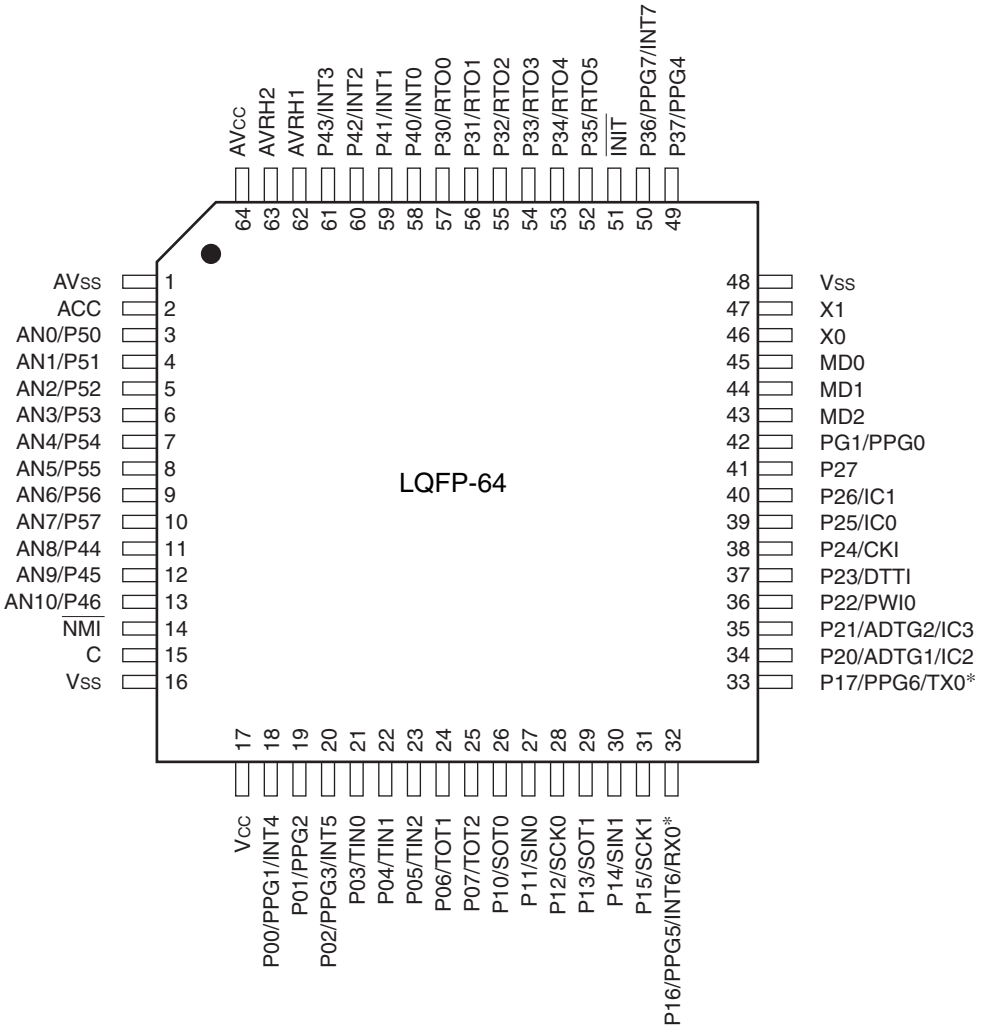
• Internal peripheral functions

	MB91V265A	MB91F267A	MB91F267NA	MB91267A	MB91267NA
	Evaluation product	**Flash memory product**		**MASK ROM product**	
Package	PGA-401 (Lead pitch 2.54 mm interstitial)	LQFP-64 (Lead pitch 0.65 mm)			
ROM/Flash size	External SRAM	128 Kbytes			
RAM size	24 Kbytes	4 Kbytes			
C-CAN	1 channel	No	1 channel	No	1 channel

- A/D converter (sequential comparison type)
  Resolution : 8/10 bits : 4 channels × 1 unit, 7 channels × 1 unit
  Conversion time : 1.2 μs (Minimum conversion time system clock at 33 MHz)
  1.35 μs (Minimum conversion time system clock at 20 MHz)
- External interrupt input : 8 channels
- Bit search module (for REALOS)
  Function for searching the MSB (upper bit) in each word for the first 1-to-0 inverted bit position
- C-CAN 32MSB : 1 channel (loaded in MB91267NA/F267NA)
- UART (Full-duplex double buffer) : 2 channels
  Selectable parity On/Off
  Asynchronous (start-stop synchronized) or clock-synchronous communications selectable
  Internal timer for dedicated baud rate (U-TIMER) on each channel
  External clock can be used as transfer clock
  Error detection function for parity, frame, and overrun errors
- 8/16-bit PPG timer : 8 channels (at 8-bit) / 4 channels (at 16-bit)
- Timing generator
- 16-bit reload timer : 3 channels (with cascade mode, without output of reload timer 0)
- 16-bit free-run timer : 3 channels
- 16-bit PWC timer : 1 channel
- Input capture : 4 channels (interface with free-run timer)
- Output compare : 6 channels (interface with free-run timer)
- Waveform generator
  Various waveforms which are generated by using output compare, 16-bit PPG timer 0, and 16-bit dead timer
- SUM of products macro
  RAM : instruction RAM (I-RAM) 256 × 16-bit
  coefficient RAM (X-RAM) 64 × 16-bit
  variable RAM (Y-RAM) 64 × 16-bit
  Execution of 1 cycle MAC (16-bit × 16-bit + 40 bits)
  Operation results are extracted rounded from 40 to 16 bits
- DMAC (DMA Controller) : 5 channels
  Operation of transfer and activation by internal peripheral interrupts and software
- Watchdog timer
- Low-power consumption mode
  Sleep/stop function
- Package : LQFP-64
- Technology : CMOS 0.35 μm
- Power supply : 1-power supply (Vcc = 4.0 V to 5.5 V)

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M23)

* : C-CAN pin is loaded in MB91267NA/F267NA.

■ PIN DESCRIPTION

Pin no.	Pin name	I/O Circuit type*1	Description
3	AN0	G	Analog input terminal of A/D converter 1. This function becomes valid when set the corresponding AICR1 register to analog input.
	P50		General purpose input/output port. This function becomes valid when analog input is set to disabled.
4	AN1	G	Analog input terminal of A/D converter 1. This function becomes valid when set the corresponding AICR1 register to analog input.
	P51		General purpose input/output port. This function becomes valid when analog input is set to disabled.
5	AN2	G	Analog input terminal of A/D converter 1. This function becomes valid when set the corresponding AICR1 register to analog input.
	P52		General purpose input/output port. This function becomes valid when analog input is set to disabled.
6	AN3	G	Analog input terminal of A/D converter 1. This function becomes valid when set the corresponding AICR1 register to analog input.
	P53		General purpose input/output port. This function becomes valid when analog input is set to disabled.
7	AN4	G	Analog input terminal of A/D converter 2. This function becomes valid when set the corresponding AICR2 register to analog input.
	P54		General purpose input/output port. This function becomes valid when analog input is set to disabled.
8	AN5	G	Analog input terminal of A/D converter 2. This function becomes valid when set the corresponding AICR2 register to analog input.
	P55		General purpose input/output port. This function becomes valid when analog input is set to disabled.
9	AN6	G	Analog input terminal of A/D converter 2. This function becomes valid when set the corresponding AICR2 register to analog input.
	P56		General purpose input/output port. This function becomes valid when analog input is set to disabled.
10	AN7	G	Analog input terminal of A/D converter 2. This function becomes valid when set the corresponding AICR2 register to analog input.
	P57		General purpose input/output port. This function becomes valid when analog input is set to disabled.
11	AN8	G	Analog input terminal of A/D converter 2. This function becomes valid when set the corresponding AICR2 register to analog input.
	P44		General purpose input/output port. This function becomes valid when analog input is set to disabled.
12	AN9	G	Analog input terminal of A/D converter 2. This function becomes valid when set the corresponding AICR2 register to analog input.
	P45		General purpose input/output port. This function becomes valid when analog input is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
13	AN10	G	Analog input terminal of A/D converter 2. This function becomes valid when set the corresponding AICR2 register to analog input.
	P46		General purpose input/output port. This function becomes valid when analog input is set to disabled.
14	$\overline{\text{NMI}}$	H	NMI (Non Maskable Interrupt) input terminal.
18	INT4	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	PPG1		Output terminal of PPG timer 1. This function becomes valid when output of PPG timer 1 is set to enabled.
	P00		General purpose input/output port. This function becomes valid when output of PPG timer 1 and external interrupt input are set to disabled.
19	PPG2	D	Output terminal of PPG timer 2. This function becomes valid when output of PPG timer 2 is set to enabled.
	P01		General purpose input/output port. This function becomes valid when output of PPG timer 2 is set to disabled.
20	INT5	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	PPG3		Output terminal of PPG timer 3. This function becomes valid when output of PPG timer 3 is set to enabled.
	P02		General purpose input/output port. This function becomes valid when output of PPG timer 3 and external interrupt input are set to disabled.
21	TIN0	D	External trigger input terminal of reload timer 0. Since this input is used as required while the trigger input is enabled, the port output must remain off unless intentionally used.
	P03		General purpose input/output port. This function becomes valid when external clock input of reload timer 0 is set to disabled.
22	TIN1	D	External trigger input terminal of reload timer 1. Since this input is used as required while the trigger input is enabled, the port output must remain off unless intentionally used.
	P04		General purpose input/output port. This function becomes valid when external clock input of reload timer 1 is set to disabled.
23	TIN2	D	External trigger input terminal of reload timer 2. Since this input is used as required while the trigger input is enabled, the port output must remain off unless intentionally used.
	P05		General purpose input/output port. This function becomes valid when external clock input of reload timer 2 is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
24	TOT1	D	Output terminal of reload timer 1. This function becomes valid when output of reload timer 1 is set to enabled.
	P06		General purpose input/output port. This function becomes valid when output of reload timer 1 is set to disabled.
25	TOT2	D	Output terminal of reload timer 2. This function becomes valid when output of reload timer 2 is set to enabled.
	P07		General purpose input/output port. This function becomes valid when output of reload timer 2 is set to disabled.
26	SOT0	D	UART0 data output terminal. This function becomes valid when data output of UART0 is set to enabled.
	P10		General purpose input/output port. This function becomes valid when data output of UART0 is set to disabled.
27	SIN0	D	UART0 data input terminal. Since this input is used as required while the UART0 input is enabled, the port output must remain off unless intentionally used.
	P11		General purpose input/output port. This function becomes valid when data input of UART0 is set to disabled.
28	SCK0	D	UART0 clock input/output terminal. This function becomes valid when clock output of UART0 is set to enabled.
	P12		General purpose input/output port. This function becomes valid when clock output of UART0 is set to disabled.
29	SOT1	D	UART1 data output terminal. This function becomes valid when data output of UART1 is set to enabled.
	P13		General purpose input/output port. This function becomes valid when data output of UART1 is set to disabled.
30	SIN1	D	UART1 data input terminal. Since this input is used as required while the UART1 input is enabled, the port output must remain off unless intentionally used.
	P14		General purpose input/output port. This function becomes valid when data input of UART1 is set to disabled.
31	SCK1	D	UART1 clock input/output terminal. This function becomes valid when clock output of UART1 is set to enabled.
	P15		General purpose input/output port. This function becomes valid when clock output of UART1 is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
32	INT6	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	PPG5		Output terminal of PPG timer 5. This function becomes valid when output of PPG timer 5 is set to enabled.
	RX0		RX0 input terminal of C-CAN0 (MB91267NA/F267NA) . Since this input is used as required while the RX0 input is enabled, port output must remain off unless intentionally used.
	P16		General purpose input/output port. This function becomes valid when output of PPG timer 5 and RX0 input*2 of C-CAN0 are set to disabled.
33	PPG6	D	Output terminal of PPG timer 6. This function becomes valid when output of PPG timer 6 is set to enabled.
	TX0		TX0 output terminal of C-CAN0 (MB91267NA/F267NA) . This function becomes valid when TX0 output of C-CAN0 is set to enabled.
	P17		General purpose input/output port. This function becomes valid when output of PPG timer 6 and TX0 output*2 of C-CAN0 are set to disabled.
34	ADTG1	D	External trigger input terminal of A/D converter 1. Since this input is used as required while it selects as A/D activation trigger cause, the port output must remain off unless intentionally used.
	IC2		Trigger input terminal of input capture 2. The port can serve as an input when set for input with the setting of the input capture trigger input. When the port is used for input capture input, this input is used as required. The port output must therefore remain off unless intentionally used.
	P20		General purpose input/output port. This function becomes valid when the setting of the external trigger input of A/D converter 1 or the setting of the input capture trigger input is set to disabled.
35	ADTG2	D	External trigger input terminal of A/D converter 2. Since this input is used as required while it selects as A/D activation trigger cause, the port output must remain off unless intentionally used.
	IC3		Trigger input terminal of input capture 3. The port can serve as an input when set for input with the setting of the input capture trigger input. When the port is used for input capture input, this input is used as required. The port output must therefore remain off unless intentionally used.
	P21		General purpose input/output port. This function becomes valid when the setting of the external trigger input of A/D converter 2 or the setting of the input capture trigger input is set to disabled.
36	PWI0	D	Pulse width counter input of PWC timer 0 This function becomes valid when pulse width counter input of PWC timer 0 is set to enabled.
	P22		General purpose input/output port. This function becomes valid when pulse width counter input of PWC timer 0 is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
37	DTTI	D	Control input signal of multi-function timer waveform generator output RTO0 to RTO5. This function becomes valid when DTTI input is set to enabled.
	P23		General purpose input/output port. This function becomes valid when input of DTTI is set to disabled.
38	CKI	D	External clock input terminal of free-run timer. Since this input is used as required while the port is used for external clock input terminal of free-run timer, the port output must remain off unless intentionally used.
	P24		General purpose input/output port. This function becomes valid when external clock input of free-run timer is set to disabled.
39	IC0	D	Trigger input terminal of input capture 0. The port can serve as an input when set for input with the setting of the trigger input of input capture 0. When the port is used for input capture input, this input is used as required. The port output must therefore remain off unless intentionally used.
	P25		General purpose input/output port. This function becomes valid when trigger input of input capture 0 is set to disabled.
40	IC1	D	Trigger input terminal of input capture 1. The port can serve as an input when set for input with the setting of the trigger input of input capture 1. When the port is used for input capture input, this input is used as required. The port output must therefore remain off unless intentionally used.
	P26		General purpose input/output port. This function becomes valid when trigger input of input capture 1 is set to disabled.
41	P27	D	General purpose input/output port.
42	PPG0	D	Output terminal of PPG timer 0. This function becomes valid when output of PPG timer 0 is set to enabled.
	PG1		General purpose input/output port. This function becomes valid when output of PPG timer 0 is set to disabled.
43	MD2	H, K	Mode terminal 2. Setting this pin determines the basic operation mode. Connect to V_{CC} or V_{SS}. The circuit type of flash memory models is K.
44	MD1	H, K	Mode terminal 1. Setting this pin determines the basic operation mode. Connect to V_{CC} or V_{SS}. The circuit type of flash memory models is K.
45	MD0	H	Mode terminal 0. Setting this pin determines the basic operation mode. Connect to V_{CC} or V_{SS}.
46	X0	A	Clock (oscillation) input terminal.
47	X1	A	Clock (oscillation) output terminal.
49	PPG4	D	Output terminal of PPG timer 4. This function becomes valid when output of PPG timer 4 is set to enabled.
	P37		General purpose input/output port. This function becomes valid when output of PPG timer 4 is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
50	INT7	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	PPG7		Output terminal of PPG timer 7. This function becomes valid when output of PPG timer 7 is set to enabled.
	P36		General purpose input/output port. This function becomes valid when output of PPG timer 7 is set to disabled.
51	$\overline{\text{INIT}}$	I	External reset input terminal.
52	RTO5	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P35		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
53	RTO4	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P34		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
54	RTO3	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P33		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
55	RTO2	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P32		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
56	RTO1	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P31		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
57	RTO0	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P30		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
58	INT0	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P40		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
59	INT1	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P41		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.
60	INT2	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P42		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.
61	INT3	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P43		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.

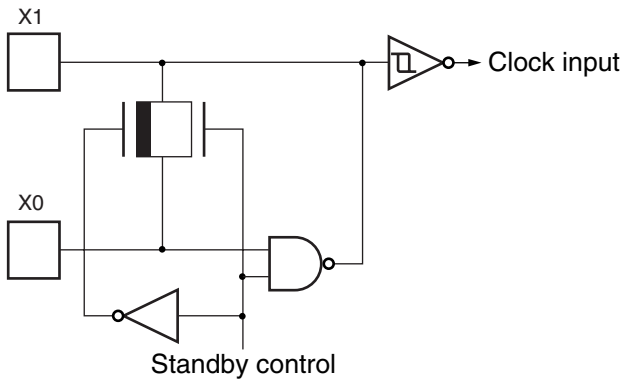
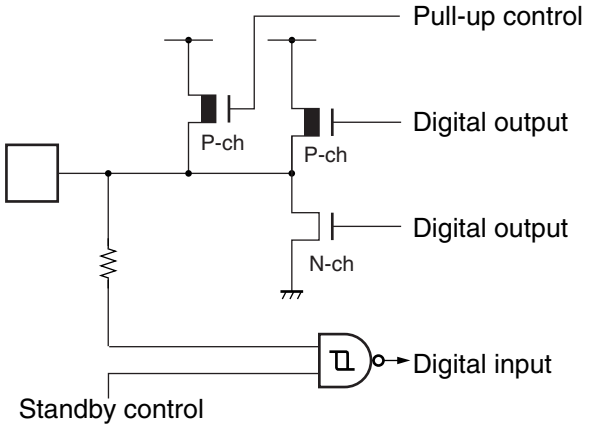
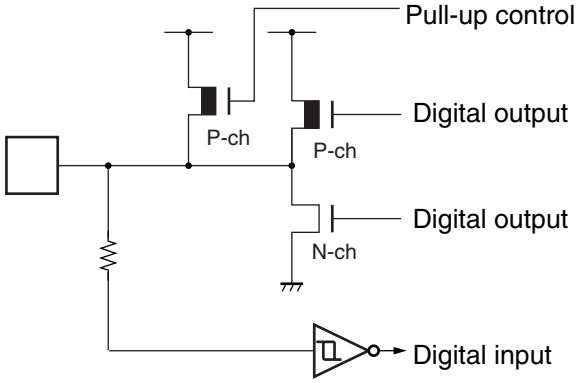
*1 : For the I/O circuit type, refer to " ■ I/O CIRCUIT TYPE "

*2 : C-CAN is set in MB91267NA/F267NA.

• Power supply and GND pins

Pin no.	Pin name	Description
16, 48	Vss	GND pins. Apply equal potential to all of the pins.
17	Vcc	Power supply pin. Apply equal potential to all of the pins.
64	AVcc	Analog power supply pin for A/D converter.
63	AVRH2	Analog reference power supply pin for A/D converter 2.
62	AVRH1	Analog reference power supply pin for A/D converter 1.
1	AVss	Analog GND pin for A/D converter.
15	C	Condenser connection pin for internal regulator.
2	ACC	Condenser connection pin for analog.

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		Oscillation feedback resistance for high speed (main clock oscillation) : approx. 1 MΩ
D		• CMOS level output • CMOS level hysteresis input • With standby control • With Pull-up control • I_{OL} = 4 mA
E		• CMOS level output • CMOS level hysteresis input • Without standby control • With Pull-up control • I_{OL} = 4 mA

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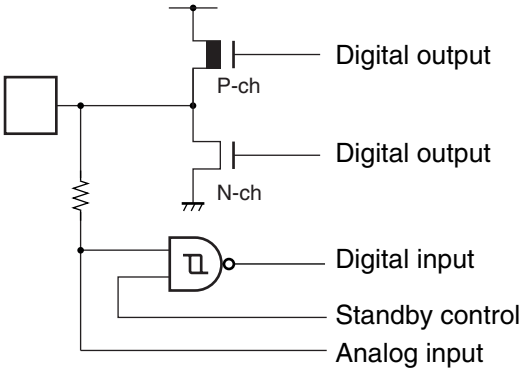
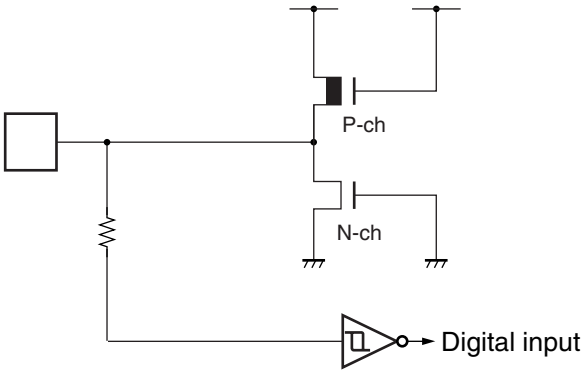
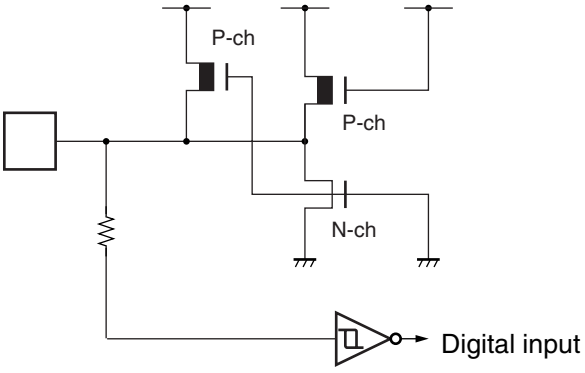
Type	Circuit type	Remarks
G		• Analog/CMOS level hysteresis input/output pin • CMOS level output • CMOS level hysteresis input (attached with standby control) • Analog input (Analog input is enabled when AICR's corresponding bit is set to "1".) • I_{OL} = 4 mA
H		• CMOS level hysteresis input • Without standby control
I		• CMOS level hysteresis input • With pull-up resistor • Without standby control

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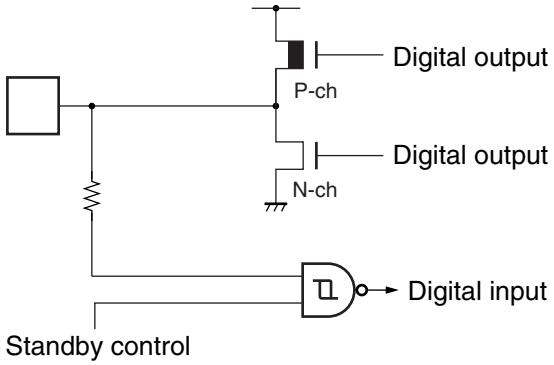
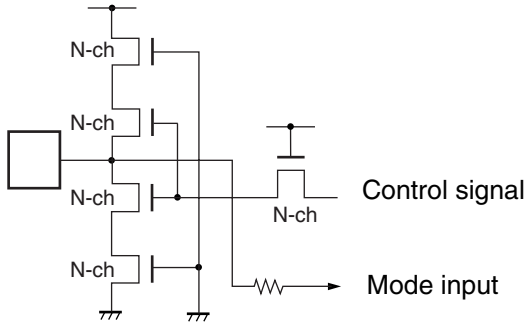
Type	Circuit type	Remarks
J		• CMOS level output • CMOS level hysteresis input • With standby control • I_{OL} = 12 mA
K		Flash memory product only • CMOS level input • High voltage control for test of flash

■ HANDLING DEVICES

Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than V_{CC} pin or less than V_{SS} pin is applied to an input or output pin or if an above-rating voltage is applied between V_{CC} and V_{SS} pins.

A latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the absolute maximum rating.

Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

About Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} pins near this device.

About Crystal Oscillator Circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0 and X1 pins the crystal oscillator (or ceramic oscillator) , and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

About Mode Pins (MD0 to MD2)

These pins should be connected directly to V_{CC} or V_{SS} pins.

To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} pins is as short as possible and the connection impedance is low.

Operation at Start-up

Be sure to execute setting initialized reset (INIT) with $\overline{INIT}$ pin immediately after start-up.

Also, in order to provide the oscillation stabilization wait time for the oscillation circuit immediately after start-up, hold the “L” level input to the $\overline{INIT}$ pin for the required stabilization wait time (For INIT via the $\overline{INIT}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value) .

Order of power turning ON/OFF

Use the following procedure for turning the power on or off.

Note that, even if the A/D converter is not used, keep the following pins connected with the level as described below.

AV_{CC} = V_{CC} level

AV_{SS} = V_{SS} level

- When Powering ON : $V_{CC} \rightarrow AV_{CC} \rightarrow AVRH$
- When Powering OFF : $AVRH \rightarrow AV_{CC} \rightarrow V_{CC}$

About Oscillation Input at Power On

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

Caution for operation during PLL clock mode

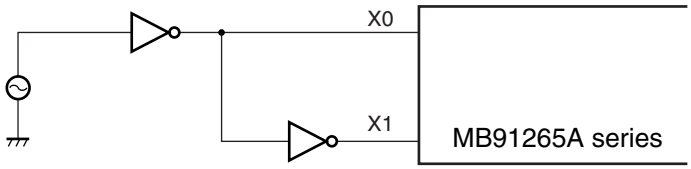
On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

External clock

When external clock is selected, the opposite phase clock to X0 pin must be supplied to X1 pin simultaneously.

If the STOP mode (oscillation stop mode) is used simultaneously, the X1 pin is stopped with the "H" output. So, when STOP mode is specified, approximately 1 kΩ of resistance should be added externally to avoid the collision of output.

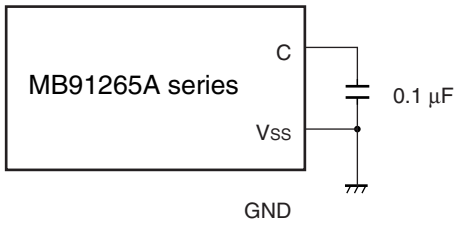
The following figure shows using an external clock.



Using an external clock

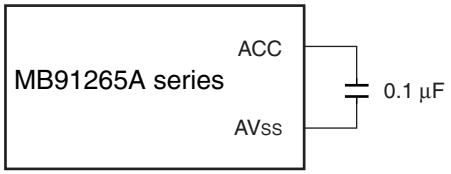
C pin

A bypass capacitor of approximately 0.1 µF should be connected the C pin for built-in regulator.



ACC pin

A capacitor of approximately 0.1 µF should be inserted between the ACC pin and the AVSS pin as this product has built-in A/D converter.



Clock Control Block

Input the “L” signal to the $\overline{INIT}$ pin to assure the clock oscillation stabilization wait time.

Switch Shared Port Function

To switch between the use as a port and the use as a dedicated pin, use the port function register (PFR) .

Low Power Consumption Mode

To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit 8 in the TBCR : timebase counter control register) and be sure to use the following sequence

```
(LDI     #value_of_standby, R0)  : value_of_standby is write data to STCR.
(LDI     #_STCR, R12)            : _STCR is address (481H) of STCR.
STB      R0, @R12                : Writing to standby control register (STCR)
LDUB     @R12, R0                : STCR read for synchronous standby
LDUB     @R12, R0                : Dummy re-read of STCR
NOP                              : NOP × 5 for arrangement of timing
NOP
NOP
NOP
NOP
```

In addition, please set I flag, ILM, and ICR to diverge to the interruption handler that is the return factor after the standby returns.

- Please do not do the following when the monitor debugger is used.
- Break point setting for above instruction lines
- Step execution for above instruction lines

Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

- The following operations may be performed when the instruction immediately followed by a DIVOU/DIVOS instruction is (a) acceptance of a user interrupt, (b) single-stepped, or (c) breaks in response to a data event or emulator menu :

  1) The D0 and D1 flags are updated in advance.

  2) An EIT handling routine (user interrupt or emulator) is executed.

  3) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed, and the D0 and D1 flags are updated to the same values as in 1).

- The following operations are performed when the ORCCR/STILM/MOVRi and PS instructions are executed to allow the interrupt.

  1) The PS register is updated in advance.

  2) An EIT handling routine (user interrupt) is executed.

  3) Upon returning from the EIT, the above instructions are executed, and the PS register is updated to the same value as in 1).

Watchdog Timer

The watchdog timer built in this model monitors a program that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on operating programs until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.

For those conditions to which this exception applies, refer to “ ■ NOTE ON DEBUGGER”.

■ NOTE ON DEBUGGER

• Step execution of RETI command

If an interrupt occurs frequently during step execution, the corresponding interrupt handling routine is executed repeatedly after step execution.

This will prevent the main routine and low-interrupt-level programs from being executed.

Do not execute step of RETI instruction for escape.

Disable the corresponding interrupt and execute debugger when the corresponding interrupt handling routine no longer needs debugging.

• Operand break

Do not apply a data event break to access to the area containing the address of a system stack pointer.

• Execution in an unused area of flash memory

Accidentally executing an instruction in an unused area of flash memory (with data placed at 0xFFFF) prevents breaks from being accepted.

To prevent this, the code event address mask function of the debugger should be used to cause a break when accessing an instruction in an unused area.

• Power-on debugging

All of the following three conditions must be satisfied when the power supply is turned off by power-on debugging.

(1) The time for the user power to fall from 0.9 V_{CC} to 0.5 V_{CC} is 25 µs or longer.
Note : In a dual-power system, V_{CC} indicates the external I/O power supply voltage.

(2) CPU operating frequency must be higher than 1 MHz.

(3) During execution of user program

• Interrupt handler for NMI request (tool)

Add the following program to the interrupt handler to prevent the device from malfunctioning in case the factor flag to be set only in response to a break request from the ICE is set, for example, by an adverse effect of noise to the DSU pin while the ICE is not connected. Enable to use the ICE while adding this program.

Additional location

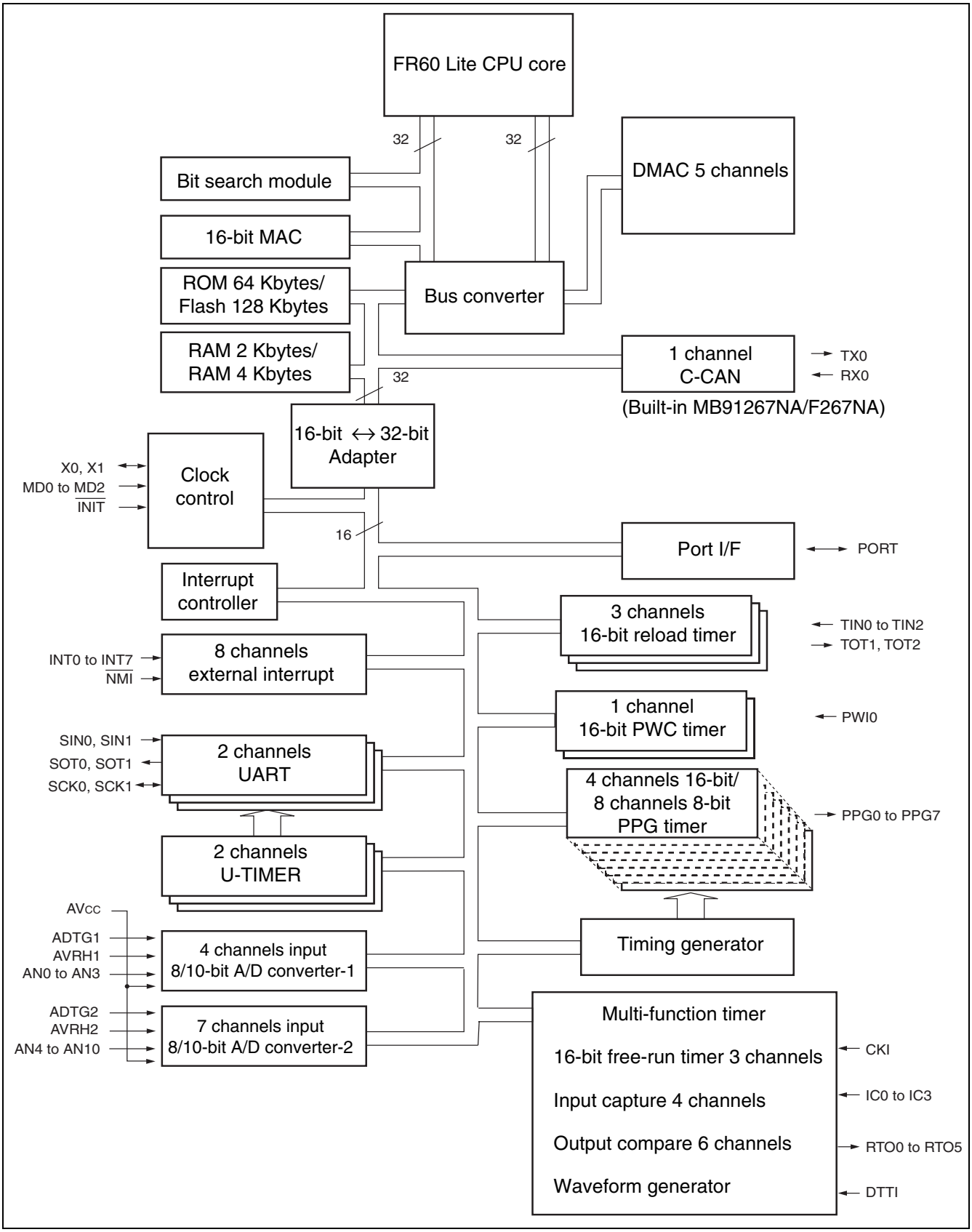
Next interrupt handler

Interrupt source	: NMI request (tool)
Interrupt number	: #13 (decimal) , 0D (hexadecimal)
Offset	: $3C8_H$
Address TBR is default	: $000FFFC8_H$

Additional program

```
STM     (R0, R1)
LDI     #B00H, R0;    : B00H is the address of DSU break factor register.
LDI     #0, R1
STB     R1, @R0       : Clear the break factor register.
LDM     (R0, R1)
RETI
```

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

- Direct Addressing Areas

The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

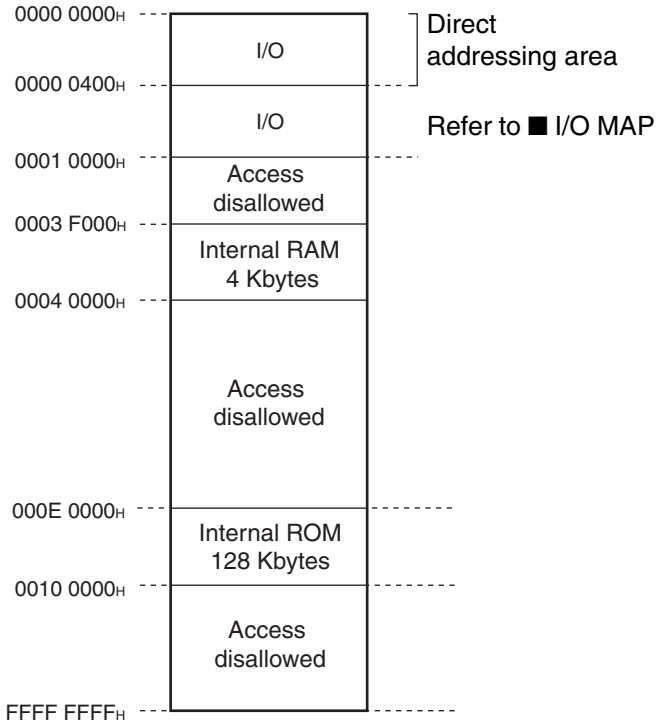
The size of directly addressable areas depends on the data size to be being accessed as follows.

→ byte data access : 000_H to $0FF_H$
→ half word data access : 000_H to $1FF_H$
→ word data access : 000_H to $3FF_H$

2. Memory Map

MB91267A/267NA/F267A/F267NA

Single chip mode



■ MODE SETTINGS

The FR family uses mode pins (MD2 to MD0) and a mode data to set the operation mode.

- Mode Pins

The MD2 to MD0 pins specify how the mode vector fetch and reset vector fetch is performed.

Setting is prohibited other than that shown in the following table.

Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	Not supported by this model.

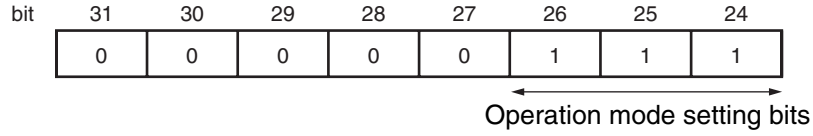
- Mode data

Data written to the internal mode register (MODR) by a mode vector fetch is called mode data.

After an operation mode has been set in the mode register, the device operates in the operation mode.

The mode data is set by all reset source. User programs cannot set data to the mode register.

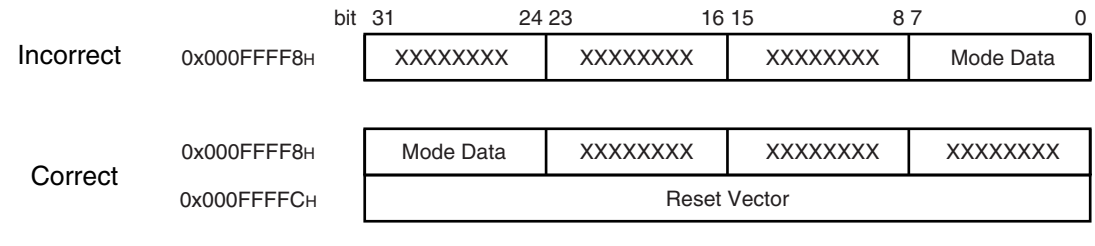
Details of mode data description



Bit31 to bit24 are all reserved bits.

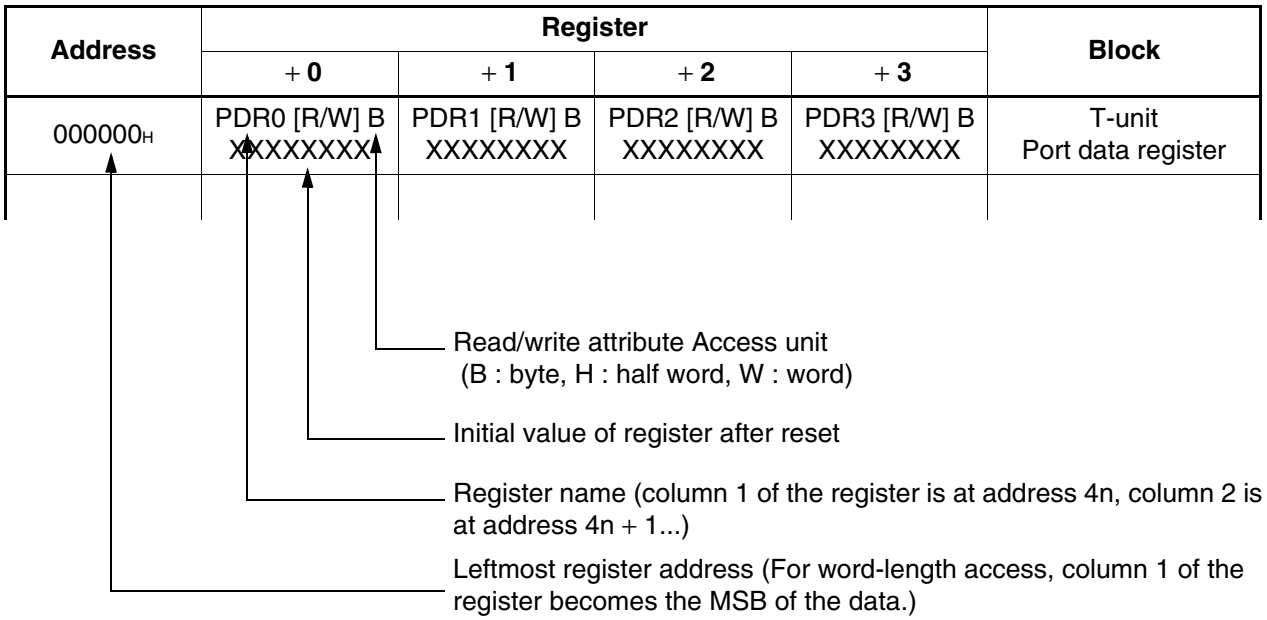
Be sure to set this bit to “00000111”.
Operation is not guaranteed when any value other than “00000111” is set.

Note : Mode data set in the mode vector must be placed as byte data at 0x000FFFF8H.
Use the highest byte from bit31 to bit24 for placement as the FR family uses the big endian for byte endian.



■ I/O MAP

[How to read the table]



Note : Initial values of register bits are represented as follows :

" 1 " : Initial Value " 1 "
" 0 " : Initial Value " 0 "
" X " : Initial Value " undefined"
" - " : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] B, H, W XXXXXXXX	PDR1 [R/W] B, H, W XXXXXXXX	PDR2 [R/W] B, H, W XXXXXXXX	PDR3 [R/W] B, H, W XXXXXXXX	Port data register
000004H	PDR4 [R/W] B, H, W -XXXXXXX	PDR5 [R/W] B, H, W XXXXXXXX	—		
000008H, 00000CH	—				
000010H	PDRG [R/W] B, H, W ------X-	—			
000014H to 00003CH	—				Reserved
000040H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt (INT0 to INT7)
000044H	DICR [R/W] B, H, W -------0	HRCL [R/W, R] B, H, W 0--11111	—		Delay interrupt/ Hold request
000048H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 0
00004CH	—		TMCSR0 [R/W, R] B, H, W ---00000 00000000		
000050H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 1
000054H	—		TMCSR1 [R/W, R] B, H, W ---00000 00000000		
000058H	TMRLR2 [W] H, W XXXXXXXX XXXXXXXX		TMR2 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 2
00005CH	—		TMCSR2 [R/W, R] B, H, W ---00000 00000000		
000060H	SSR0 [R/W, R] B, H, W 00001000	SIDR0 [R]/SODR0[W] B, H, W XXXXXXXX	SCR0 [R/W] B, H, W 00000100	SMR0 [R/W, W] B, H, W 00--0-0-	UART0
000064H	UTIM0 [R] H / UTIMR0 [W] H 00000000 00000000		DRCL0 [W] B --------	UTIMC0 [R/W] B 0--00001	U-TIMER 0
000068H	SSR1 [R/W, R] B, H, W 00001000	SIDR1 [R]/SODR1[W] B, H, W XXXXXXXX	SCR1 [R/W] B, H, W 00000100	SMR1 [R/W] B, H, W 00--0-0-	UART1
00006CH	UTIM1 [R] H / UTIMR1 [W] H 00000000 00000000		DRCL1 [W] B --------	UTIMC1 [R/W] B 0--00001	U-TIMER 1
000070H to 00007CH	—				Reserved
000080H	ADCH1 [R/W] B, H, W XXXX0XX0	ADMD1 [R/W] B, H, W 00001111	ADCD11 [R] B, H, W XXXXXXXX	ADCD10 [R] B, H, W XXXXXXXX	A/D converter 1/ AICR1
000084H	ADCS1 [R/W, W] B, H, W 00000X00	—	AICR1 [R/W] B, H, W ----0000	—	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000088H	ADCH2 [R/W] B, H, W XXXX0XX0	ADMD2 [R/W] B, H, W 00001111	ADCD21 [R] B, H, W XXXXXXXX	ADCD20 [R] B, H, W XXXXXXXX	A/D converter 2/ AICR2
00008CH	ADCS2 [R/W, W] B, H, W 00000X00	—	AICR2 [R/W] B, H, W -0000000	—	
000090H	OCCPBH0, OCCPBL0[W] / OCCPH0, OCCPL0[R] H, W 00000000 00000000		OCCPBH1, OCCPBL1[W] / OCCPH1, OCCPL1 [R] H, W 00000000 00000000		16-bit output compare
000094H	OCCPBH2, OCCPBL2[W] / OCCPH2, OCCPL2 [R] H, W 00000000 00000000		OCCPBH3, OCCPBL3[W] / OCCPH3, OCCPL3 [R] H, W 00000000 00000000		
000098H	OCCPBH4, OCCPBL4[W] / OCCPH4, OCCPL4 [R] H, W 00000000 00000000		OCCPBH5, OCCPBL5[W] / OCCPH5, OCCPL5 [R] H, W 00000000 00000000		
00009CH	OCSH1 [R/W] B, H, W X1100000	OCSL0 [R/W] B, H, W 00001100	OCSH3 [R/W] B, H, W X1100000	OCSL2 [R/W] B, H, W 00001100	
0000A0H	OCSH5 [R/W] B, H, W X1100000	OCSL4 [R/W] B, H, W 00001100	OCMOD [R/W] B, H, W XX000000	—	
0000A4H	CPCLRBH0, CPCLRBL0[W]/ CPCLRH0, CPCLRL0[R] H, W 11111111 11111111		TCDTH0, TCDTL0 [R/W] H, W 00000000 00000000		16-bit free-run timer 0
0000A8H	TCCSH0 [R/W] B, H, W 00000000	TCCSL0 [R/W] B, H, W 01000000	—	ADTRGC [R/W] B, H, W XXXX0000	
0000ACH	IPCPH0, IPCPL0 [R] H, W XXXXXXXX XXXXXXXX		IPCPH1, IPCPL1 [R] H, W XXXXXXXX XXXXXXXX		16-bit input capture
0000B0H	IPCPH2, IPCPL2 [R] H, W XXXXXXXX XXXXXXXX		IPCPH3, IPCPL3 [R] H, W XXXXXXXX XXXXXXXX		
0000B4H	PICSH01 [W] B, H, W 00000000	PICSL01 [R/W] B, H, W 00000000	ICSH23 [R] B, H, W XXXXXX00	ICSL23 [R/W]B, H, W 00000000	
0000B8H	—				Reserved
0000BCH	TMRRH0, TMRRL0 [R/W] H, W XXXXXXXX XXXXXXXX		TMRRH1, TMRRL1 [R/W] H, W XXXXXXXX XXXXXXXX		Waveform generator
0000C0H	TMRRH2, TMRRL2 [R/W] H, W XXXXXXXX XXXXXXXX		—		
0000C4H	DTCR0 [R/W] B, H, W 00000000	DTCR1 [R/W] B, H, W 00000000	DTCR2 [R/W] B, H, W 00000000	—	
0000C8H	—	SIGCR1 [R/W] B, H, W 00000000	—	SIGCR2 [R/W] B, H, W XXXXXXX1	
0000CCH	—		ADCOMP1 [R/W] H, W 00000000 00000000		A/D COMP
0000D0H	ADCOMP2 [R/W] H, W 00000000 00000000		ADCOMPC2 [R/W] B, H, W XX0000XX	ADCOMPC1 [R/W] B, H, W XXXXX00X	
0000D4H to 0000DCH	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000E0H	PWCSR0 [R/W, R] B, H, W 00000000 00000000		PWCR0 [R] H, W 00000000 00000000		16-bit PWC timer
0000E4H	—				
0000E8H	—	PDIVR0 [R/W] B, H, W XXXXX000	—		
0000ECH to 0000FCH	—				Reserved
000100H	PRLH0 [R/W] B, H, W XXXXXXXX	PRLL0 [R/W] B, H, W XXXXXXXX	PRLH1 [R/W] B, H, W XXXXXXXX	PRLL1 [R/W] B, H, W XXXXXXXX	8/16-bit PPG timer 0 to 7
000104H	PRLH2 [R/W] B, H, W XXXXXXXX	PRLL2 [R/W] B, H, W XXXXXXXX	PRLH3 [R/W] B, H, W XXXXXXXX	PRLL3 [R/W] B, H, W XXXXXXXX	
000108H	PPGC0 [R/W] B, H, W 00000000	PPGC1 [R/W] B, H, W 00000000	PPGC2 [R/W] B, H, W 00000000	PPGC3 [R/W] B, H, W 00000000	
00010CH	PRLH4 [R/W] B, H, W XXXXXXXX	PRLL4 [R/W] B, H, W XXXXXXXX	PRLH5 [R/W] B, H, W XXXXXXXX	PRLL5 [R/W] B, H, W XXXXXXXX	
000110H	PRLH6 [R/W] B, H, W XXXXXXXX	PRLL6 [R/W] B, H, W XXXXXXXX	PRLH7 [R/W] B, H, W XXXXXXXX	PRLL7 [R/W] B, H, W XXXXXXXX	
000114H	PPGC4 [R/W] B, H, W 00000000	PPGC5 [R/W] B, H, W 00000000	PPGC6 [R/W] B, H, W 00000000	PPGC7 [R/W] B, H, W 00000000	
000118H to 00012CH	—				Reserved
000130H	TRG [R/W] B, H, W -------- 00000000		—	GATEC [R/W] B, H, W XXXXXX00	8/16-bit PPG timer 0 to 7
000134H	REVC [R/W] B, H, W -------- 00000000		—		
000138H to 000140H	—				Reserved
000144H	TTCR0 [R/W] B, H, W 00000000	—		TSTPR0 [R] B, H, W 00000000	Timing generator
000148H	COMP0 [R/W] B, H, W 00000000	COMP2 [R/W] B, H, W 00000000	COMP4 [R/W] B, H, W 00000000	COMP6 [R/W] B, H, W 00000000	
00014CH, 000150H	—				
000154H	CPCLRBH1, CPCLRBL1 [W] / CPCLRH1, CPCLRL1 [R] H, W 11111111 11111111		TCDTH1, TCDTL1 [R/W] H, W 00000000 00000000		16-bit free-run timer 1
000158H	TCCSH1 [R/W] B, H, W 00000000	TCCSL1 [R/W] B, H, W 01000000	—		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00015CH	CPCLRBH2, CPCLRBL2 [W] / CPCLRH2, CPCLRL2 [R] H, W 11111111 11111111		TCDTH2, TCDTL2 [R/W] H, W 00000000 00000000		16-bit free-run timer 2
000160H	TCCSH2 [R/W] B, H, W 00000000	TCCSL2 [R/W] B, H, W 01000000	—		
000164H	—				Reserved
000168H	—	FSR2 [R/W] B, H, W 00000000	FSR1 [R/W] B, H, W ----0000	FSR0 [R/W] B, H, W 00000000	FRT selector
00016CH to 0001A4H	—				Reserved
0001A8H	CANPRE [R, R/W] B, H, W 00000000	—			C-CAN*1 prescaler
0001ACH to 0001FCH	—				Reserved
000200H	DMACA0 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] B, H, W*2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	—				Reserved
000240H	DMACR [R/W] B 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 000398H	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00039CH	—				16-bit MAC
0003A0H	DSP-PC [R/W] XXXXXXXX	DSP-CSR [R/W, R, W] 00000000	DSP-LY [R/W] XXXXXXXX XXXXXXXX		
0003A4H	DSP-OT0 [R] XXXXXXXX XXXXXXXX		DSP-OT1 [R] XXXXXXXX XXXXXXXX		
0003A8H	DSP-OT2 [R] XXXXXXXX XXXXXXXX		DSP-OT3 [R] XXXXXXXX XXXXXXXX		
0003ACH	—				
0003B0H	DSP-OT4 [R] XXXXXXXX XXXXXXXX		DSP-OT5 [R] XXXXXXXX XXXXXXXX		
0003B4H	DSP-OT6[R] XXXXXXXX XXXXXXXX		DSP-OT7 [R] XXXXXXXX XXXXXXXX		
0003B8H	—				
0003BCH to 0003ECH	—				Reserved
0003F0H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDR0 [R/W] B, H, W 00000000	DDR1 [R/W] B, H, W 00000000	DDR2 [R/W] B, H, W 00000000	DDR3 [R/W] B, H, W 00000000	Data direction register
000404H	DDR4 [R/W] B, H, W -0000000	DDR5 [R/W] B, H, W 00000000	—		
000408H, 00040CH	—				
000410H	DDRG [R/W] B, H, W ------0-	—			
000414H to 00041CH	—				Reserved
000420H	PFR0 [R/W] B, H, W 00------	PFR1 [R/W] B, H, W 0-0-00-0	—		Port function register
000424H to 00042CH	—				
000430H	—			PTFR0 [R/W] B, H, W 00000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000434H to 00043CH	—				Reserved
000440H	ICR00 [R/W, R] B, H, W ----1111	ICR01 [R/W, R] B, H, W ----1111	ICR02 [R/W, R] B, H, W ----1111	ICR03 [R/W, R] B, H, W ----1111	Interrupt control unit
000444H	ICR04 [R/W, R] B, H, W ----1111	ICR05 [R/W, R] B, H, W ----1111	ICR06 [R/W, R] B, H, W ----1111	ICR07 [R/W, R] B, H, W ----1111	
000448H	ICR08 [R/W, R] B, H, W ----1111	ICR09 [R/W, R] B, H, W ----1111	ICR10 [R/W, R] B, H, W ----1111	ICR11 [R/W, R] B, H, W ----1111	
00044CH	ICR12 [R/W, R] B, H, W ----1111	ICR13 [R/W, R] B, H, W ----1111	ICR14 [R/W, R] B, H, W ----1111	ICR15 [R/W, R] B, H, W ----1111	
000450H	ICR16 [R/W, R] B, H, W ----1111	ICR17 [R/W, R] B, H, W ----1111	ICR18 [R/W, R] B, H, W ----1111	ICR19 [R/W, R] B, H, W ----1111	
000454H	ICR20 [R/W, R] B, H, W ----1111	ICR21 [R/W, R] B, H, W ----1111	ICR22 [R/W, R] B, H, W ----1111	ICR23 [R/W, R] B, H, W ----1111	
000458H	ICR24 [R/W, R] B, H, W ----1111	ICR25 [R/W, R] B, H, W ----1111	ICR26 [R/W, R] B, H, W ----1111	ICR27 [R/W, R] B, H, W ----1111	
00045CH	ICR28 [R/W, R] B, H, W ----1111	ICR29 [R/W, R] B, H, W ----1111	ICR30 [R/W, R] B, H, W ----1111	ICR31 [R/W, R] B, H, W ----1111	
000460H	ICR32 [R/W, R] B, H, W ----1111	ICR33 [R/W, R] B, H, W ----1111	ICR34 [R/W, R] B, H, W ----1111	ICR35 [R/W, R] B, H, W ----1111	
000464H	ICR36 [R/W, R] B, H, W ----1111	ICR37 [R/W, R] B, H, W ----1111	ICR38 [R/W, R] B, H, W ----1111	ICR39 [R/W, R] B, H, W ----1111	
000468H	ICR40 [R/W, R] B, H, W ----1111	ICR41 [R/W, R] B, H, W ----1111	ICR42 [R/W, R] B, H, W ----1111	ICR43 [R/W, R] B, H, W ----1111	
00046CH	ICR44 [R/W, R] B, H, W ----1111	ICR45 [R/W, R] B, H, W ----1111	ICR46 [R/W, R] B, H, W ----1111	ICR47 [R/W, R] B, H, W ----1111	
000470H to 00047CH	—				Reserved
000480H	RSRR [R/W] B, H, W 10000000	STCR [R/W] B, H, W 00110011	TBCR [R/W] B, H, W 00XXXX00	CTBR [W] B, H, W XXXXXXXX	Clock control
000484H	CLKR [R/W] B, H, W 00000000	WPR [W] B, H, W XXXXXXXX	DIVR0 [R/W] B, H, W 00000011	DIVR1 [R/W] B, H, W 00000000	
000488H to 000490H	—				
000494H to 0005FCH	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000600H	PCR0 [R/W] B, H, W 00000000	PCR1 [R/W] B, H, W 00000000	PCR2 [R/W] B, H, W 00000000	PCR3 [R/W] B, H, W 00------	Pull-up Control Unit
000604H	PCR4 [R/W] B, H, W ----0000	—			
000608H, 00060CH	—				
000610H	PCRG [R/W] B, H, W ------0-	—			
000614H to 000FFCH	—				Reserved
001000H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 006FFCH	—				Reserved
007000H	FLCR [R/W] B 01101000	—			Flash
007004H	FLWC [R/W] B 00000011	—			
007008H to 007010H	—				
007014H to 00BFFCH	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C000H to 00C07CH	X-RAM (coefficient RAM) [R/W] 64 × 16-bit				16-bit MAC
00C080H to 00C0FCH	Y-RAM (variable RAM) [R/W] 64 × 16-bit				
00C100H to 00C2FCH	I-RAM (instruction RAM) [R/W] 256 × 16-bit				
00C300H to 00FFFCH	—				Reserved
020000H	CTRLR0 [R, R/W] 00000000 00000001		STATR0 [R, R/W] 00000000 00000000		C-CAN*1
020004H	ERRCNT0 [R] 00000000 00000000		BTR0 [R, R/W] 00100011 00000001		
020008H	INTR0 [R] 00000000 00000000		TESTR0 [R, R/W] 00000000 X0000000		
02000CH	BRPER0 [R, R/W] 00000000 00000000		—		
020010H	IF1CREQ0 [R, R/W] 00000000 00000000		IF1CMSK0 [R, R/W] 00000000 00000000		
020014H	IF1MSK20 [R, R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
020018H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
02001CH	IF1MCTR0 [R, R/W] 00000000 00000000		—		
020020H	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
020024H	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
020030H	Reserved (IF1 data mirror, little endian byte ordering)				
020040H	IF2CREQ0 [R, R/W] 00000000 00000000		IF2CMSK0 [R, R/W] 00000000 00000000		
020044H	IF2MSK20 [R, R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
020048H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
02004CH	IF2MCTR0 [R, R/W] 00000000 00000000		—		
020050H	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
020054H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		C-CAN*1
020060H	Reserved (IF2 data mirror, little endian byte ordering)				
020080H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		
020084H	Reserved (>32..128 Message buffer)				
020090H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
020094H	Reserved (>32..128 Message buffer)				
0200A0H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
0200A4H	Reserved (>32..128 Message buffer)				
0200B0H	MESVAL20 [R] 00000000 00000000		MESVAL10 [R] 00000000 00000000		
0200B4H	Reserved (>32..128 Message buffer)				

*1 : C-CAN is loaded in MB91267NA/F267NA.

*2 : The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed in bytes.

Notes :
- The initial value of FLWC (7004H) is “00010011B” on EVA tool. Writing “00000011B” on the evaluation model has no effect on its operation.
- Do not execute Read Modify Write instructions on registers having a write-only bit.
- Data is undefined in reserved or (-) area.

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Reset	0	00	—	$3FC_H$	$000FFFFC_H$
Mode vector	1	01	—	$3F8_H$	$000FFFF8_H$
System reserved	2	02	—	$3F4_H$	$000FFFF4_H$
System reserved	3	03	—	$3F0_H$	$000FFFF0_H$
System reserved	4	04	—	$3EC_H$	$000FFFEC_H$
System reserved	5	05	—	$3E8_H$	$000FFFE8_H$
System reserved	6	06	—	$3E4_H$	$000FFFE4_H$
Coprocessor absent trap	7	07	—	$3E0_H$	$000FFFE0_H$
Coprocessor error trap	8	08	—	$3DC_H$	$000FFFDC_H$
INTE instruction	9	09	—	$3D8_H$	$000FFFD8_H$
System reserved	10	0A	—	$3D4_H$	$000FFFD4_H$
System reserved	11	0B	—	$3D0_H$	$000FFFD0_H$
Step trace trap	12	0C	—	$3CC_H$	$000FFFCC_H$
NMI request (tool)	13	0D	—	$3C8_H$	$000FFFC8_H$
Undefined instruction exception	14	0E	—	$3C4_H$	$000FFFC4_H$
NMI request	15	0F	15 (F_H) fixed	$3C0_H$	$000FFFC0_H$
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$
External interrupt 4	20	14	ICR04	$3AC_H$	$000FFFAC_H$
External interrupt 5	21	15	ICR05	$3A8_H$	$000FFFA8_H$
External interrupt 6/C-CAN wake up*	22	16	ICR06	$3A4_H$	$000FFFA4_H$
External interrupt 7	23	17	ICR07	$3A0_H$	$000FFFA0_H$
Reload timer 0	24	18	ICR08	$39C_H$	$000FFF9C_H$
Reload timer 1	25	19	ICR09	398_H	$000FFF98_H$
Reload timer 2	26	1A	ICR10	394_H	$000FFF94_H$
UART0(Reception completed)	27	1B	ICR11	390_H	$000FFF90_H$
UART0 (RX completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$
DTTI	29	1D	ICR13	388_H	$000FFF88_H$
DMAC0 (end, error)	30	1E	ICR14	384_H	$000FFF84_H$
DMAC1 (end, error)	31	1F	ICR15	380_H	$000FFF80_H$
DMAC2/DMAC3/DMAC4 (end, error)	32	20	ICR16	$37C_H$	$000FFF7C_H$

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
UART1(Reception completed)	33	21	ICR17	378H	000FFF78H
UART1 (RX completed)	34	22	ICR18	374H	000FFF74H
C-CAN0*	35	23	ICR19	370H	000FFF70H
System reserved	36	24	ICR20	36CH	000FFF6CH
16-bit MAC	37	25	ICR21	368H	000FFF68H
PPG0/PPG1	38	26	ICR22	364H	000FFF64H
PPG2/PPG3	39	27	ICR23	360H	000FFF60H
PPG4/PPG5/PPG6/PPG7	40	28	ICR24	35CH	000FFF5CH
System reserved	41	29	ICR25	358H	000FFF58H
Waveform0/1/2 (underflow)	42	2A	ICR26	354H	000FFF54H
Free-run timer 1 (compare clear)	43	2B	ICR27	350H	000FFF50H
Free-run timer 1 (zero detection)	44	2C	ICR28	34CH	000FFF4CH
Free-run timer 2 (compare clear)	45	2D	ICR29	348H	000FFF48H
Free-run timer 2 (zero detection)	46	2E	ICR30	344H	000FFF44H
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H
Free-run timer 0 (compare clear)	48	30	ICR32	33CH	000FFF3CH
Free-run timer 0 (zero detection)	49	31	ICR33	338H	000FFF38H
System reserved	50	32	ICR34	334H	000FFF34H
A/D converter 1	51	33	ICR35	330H	000FFF30H
A/D converter 2	52	34	ICR36	32CH	000FFF2CH
PWC0 (measurement completed)	53	35	ICR37	328H	000FFF28H
System reserved	54	36	ICR38	324H	000FFF24H
PWC0 (overflow)	55	37	ICR39	320H	000FFF20H
System reserved	56	38	ICR40	31CH	000FFF1CH
ICU0 (capture)	57	39	ICR41	318H	000FFF18H
ICU1 (capture)	58	3A	ICR42	314H	000FFF14H
ICU2/3 (capture)	59	3B	ICR43	310H	000FFF10H
OCU0/1 (match)	60	3C	ICR44	30CH	000FFF0CH
OCU2/3 (match)	61	3D	ICR45	308H	000FFF08H
OCU4/5 (match)	62	3E	ICR46	304H	000FFF04H
Delay interrupt source bit	63	3F	ICR47	300H	000FFF00H
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
System reserved	66	42	—	$2F4_H$	$000FFEF4_H$
System reserved	67	43	—	$2F0_H$	$000FFEF0_H$
System reserved	68	44	—	$2EC_H$	$000FFEEC_H$
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$
System reserved	73	49	—	$2D8_H$	$000FFED8_H$
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$

* : C-CAN interrupt is only loaded in MB91267NA/F267NA.

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
  Indicates that the input function can be used.
- Input 0 fixed
  Indicates that the input level has been internally fixed to be 0 to prevent leakage when the input is released.
- Output Hi-Z
- Output is maintained.
  Indicates the output in the output state existing immediately before this mode is established.
  If the device enters this mode with an internal output peripheral operating or while serving as an output port, the output is performed by the internal peripheral or the port output is maintained, respectively.
- State existing immediately before is maintained.
  When the device serves for output or input immediately before entering this mode, the device maintains the output or is ready for the input, respectively.

• List of pin status (single chip mode)

Pin no.	Pin name	Function	At initializing		At sleep mode	At Stop mode	
			$\overline{INIT}$ = L*1	$\overline{INIT}$ = H*2		Hi-Z = 0	Hi-Z = 1
3 to 10	P50 to P57	AN0 to AN7	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed
11 to 13	P44 to P46	AN8 to AN10					
14	$\overline{NMI}$	$\overline{NMI}$	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
18	P00	PPG1/INT4	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled			
19	P01	PPG2			Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed
20	P02	PPG3/INT5			Input enabled	Input enabled	Input enabled
21 to 23	P03 to P05	TIN0 to TIN2			Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed
24, 25	P06, P07	TOT1, TOT2					
26	P10	SOT0					
27	P11	SIN0					
28	P12	SCK0					
29	P13	SOT1					
30	P14	SIN1					
31	P15	SCK1					
32	P16	PPG5/INT6/ RX0*3			Input enabled	Input enabled	Input enabled

(Continued)

(Continued)

Pin no.	Pin name	Function	At initializing		At sleep mode	At Stop mode	
			$\overline{\text{INIT}}$ = L*1	$\overline{\text{INIT}}$ = H*2		Hi-Z = 0	Hi-Z = 1
33	P17	PPG6/TX0*3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed
34	P20	ADTG1/IC2					
35	P21	ADTG2/IC3					
36	P22	PWI0					
37	P23	DTTI					
38	P24	CKI					
39	P25	IC0					
40	P26	IC1					
41	P27	General port					
42	PG1	PPG0					
49	P37	PPG4					
50	P36	PPG7/INT7			Input enabled	Input enabled	Input enabled
52 to 57	P35 to P30	RTO5 to RTO0			Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed
58 to 61	P40 to P43	INT0 to INT3			Input enabled	Input enabled	Input enabled

*1 : $\overline{\text{INIT}}$ = L : Indicates the pin status with $\overline{\text{INIT}}$ remaining at the “L” level.

*2 : $\overline{\text{INIT}}$ = H : Indicates the pin status existing immediately after $\overline{\text{INIT}}$ transition from “L” to “H” level.

*3 : C-CAN terminal is loaded in MB91267NA/F267NA.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.5	V_{SS} + 6.0	V	
Analog power supply voltage*1	AV_{CC}	V_{SS} – 0.5	V_{SS} + 6.0	V	*2
Analog reference voltage*1	AVRHn*6	V_{SS} – 0.5	V_{SS} + 6.0	V	*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS} – 0.3	AVcc + 0.3	V	
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	60	mA	
“L” level total average output current	ΣI_{OLAV}	—	30	mA	*5
“H” level maximum output current	I_{OH}	—	– 10	mA	*3
“H” level average output current	I_{OHAV}	—	– 4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	– 30	mA	
“H” level total average output current	ΣI_{OHAV}	—	– 12	mA	*5
Power consumption	P_D	—	600	mW	
Operating temperature	Ta	– 40	+ 105	°C	At single chip operating
Storage temperature	Tstg	– 55	+ 125	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0$ V.

*2 : Be careful not to exceed V_{CC} + 0.3 V, for example, when the power is turned on.
Be careful not to let AV_{CC} exceed V_{CC}, for example, when the power is turned on.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output current is the average current for a single pin over a period of 100 ms.

*5 : The total average output current is the average current for all pins over a period of 100 ms.

*6 : AVRHn = AVRH1, AVRH2

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(Vss = AVss = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.0	5.5	V	At normal operating
Analog power supply voltage	AV_{CC}	V_{SS} + 4.0	V_{SS} + 5.5	V	
Analog reference voltage	AVRH1	AV_{SS}	AV_{CC}	V	For A/D converter 1
	AVRH2	AV_{SS}	AV_{CC}	V	For A/D converter 2
Operating temperature	Ta	− 40	+ 105	°C	At single chip operating

Note : Upon power up, it takes approx. 100 µs for stabilization of internal power supply after the V_{CC} power supply is stabilized. Keep applying “L” to $\overline{INIT}$ pin signal during that period.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	Hysteresis input pin	—	Vcc × 0.8	—	Vcc + 0.3	V	
"L" level input voltage	V_{ILS}	Hysteresis input pin	—	Vss – 0.3	—	Vss × 0.2	V	
"H" level output voltage	V_{OH}	Other than P30 to P35	V_{CC} = 5.0 V, I_{OH} = 4.0 mA	Vcc – 0.5	—	—	V	
	V_{OH2}	P30 to P35	V_{CC} = 5.0 V, I_{OH} = 8.0 mA	Vcc – 0.7	—	—	V	
"L" level output voltage	V_{OL}	Other than P30 to P35	V_{CC} = 5.0 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P30 to P35	V_{CC} = 5.0 V, I_{OL} = 12 mA	—	—	0.6	V	
Input leak current	I_{LI}	—	V_{CC} = 5.0 V, V_{SS} < V_I < V_{CC}	– 5	—	+ 5	µA	
Pull-up resistance	R_{PULL}	$\overline{INIT}$, Pull-up pin	—	—	50	—	kΩ	
Power supply current	I_{CC}	V_{CC}	V_{CC} = 5.0 V, 33 MHz	—	90	100	mA	
	I_{CCS}	V_{CC}	V_{CC} = 5.0 V, 33 MHz	—	60	80	mA	At SLEEP
	I_{CCH}	V_{CC}	V_{CC} = 5.0 V, Ta = + 25 °C	—	300	—	µA	At STOP
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, AVRH1, AVRH2	—	—	5	15	pF	

4. Flash Memory Write/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	Ta = + 25 °C, Vcc = 5.0 V	—	0.2	0.5	s	Not including time for internal writing before deletion.
Byte write time	Ta = + 25 °C, Vcc = 5.0 V	—	32	3600	µs	Not including system-level overhead time.
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average Ta = + 85 °C	20	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

5. AC Characteristics

(1) Clock Timing Ratings

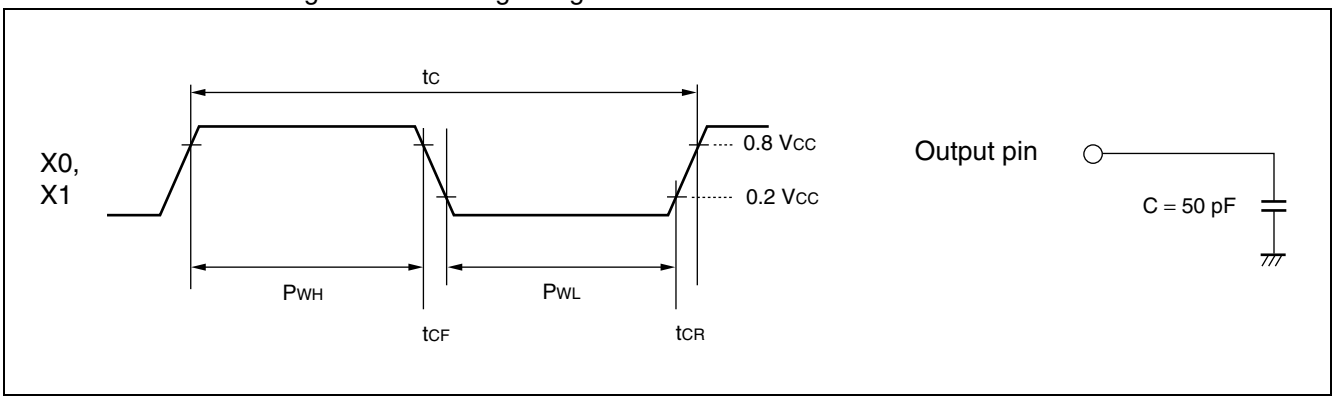
(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0, X1	—	3.6*2	—	12	MHz	For using the PLL within the self-oscillation enabled range, set the multiplier for the internal clock not to let the operating frequency exceed 33 MHz.
Clock cycle time	t_C	X0, X1	—	83.3	—	278*2	ns	
Input clock pulse width	P_{WH}, P_{WL}	X0	—	100	—	—	ns	The standard of the duty ratio is 40 % to 60 %.
Input clock rising, falling time	t_{CF}, t_{CR}	X0	—	—	—	5	ns	At external clock
Internal operating clock frequency	f_{CP}	—	When 4.125 MHz is input as the X0 clock frequency and ×8 multiplication is set for the PLL of the oscillator circuit.	2.06*1	—	33	MHz	CPU
	f_{CPP}			2.06*1	—	33	MHz	Peripheral
Internal operating clock cycle time	t_{CP}	—		30.3	—	485*1	ns	CPU
	t_{CPP}			30.3	—	485*1	ns	Peripheral

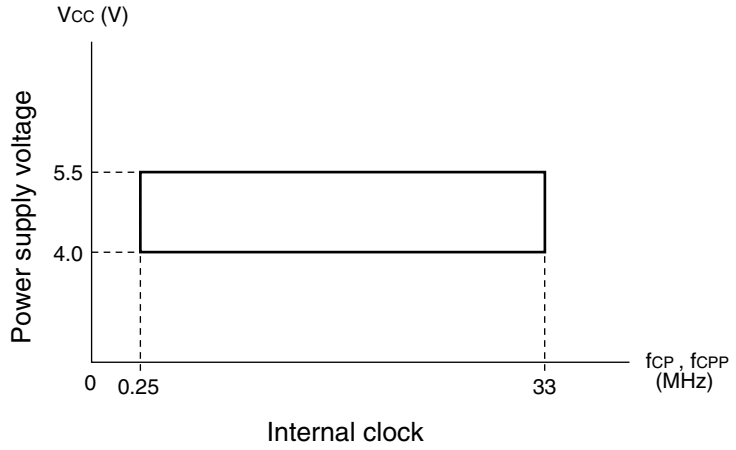
*1 : The values assume a gear cycle of 1/16.

*2 : When the PLL is used, the lower-limit frequency of the input clock to the X0 and X1 pins determines depending on the PLL multiplication.
At × 1 multiplication : more than 8 MHz
At × 2 to × 8 multiplication : more than 4 MHz

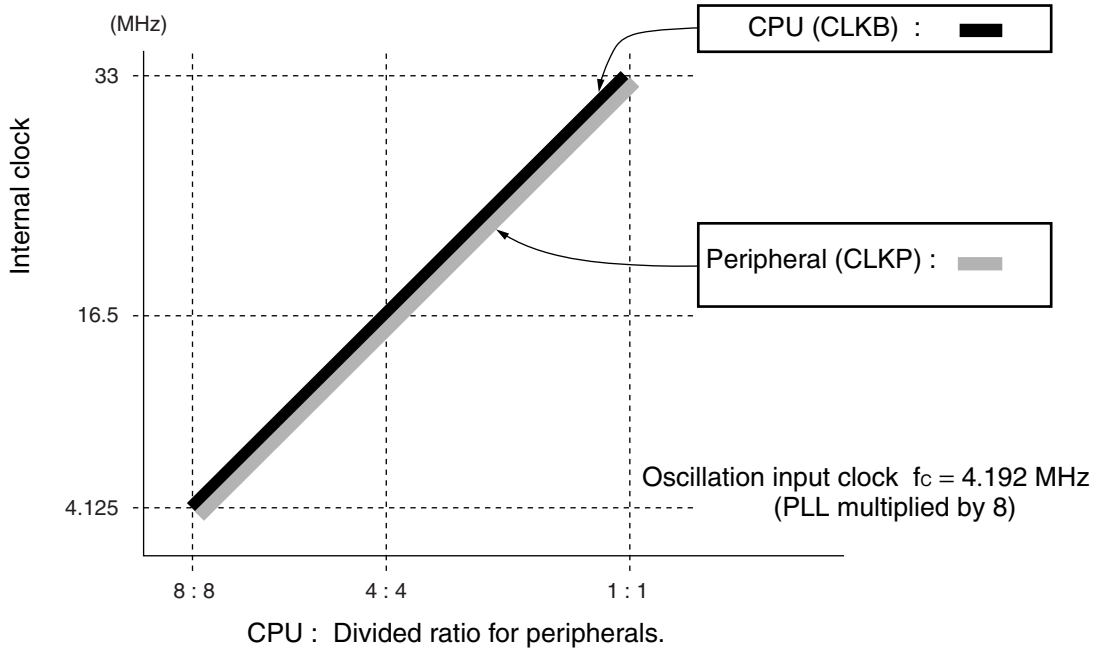
• Conditions for measuring the clock timing ratings



• Operation Assurance Range



• Internal clock setting range



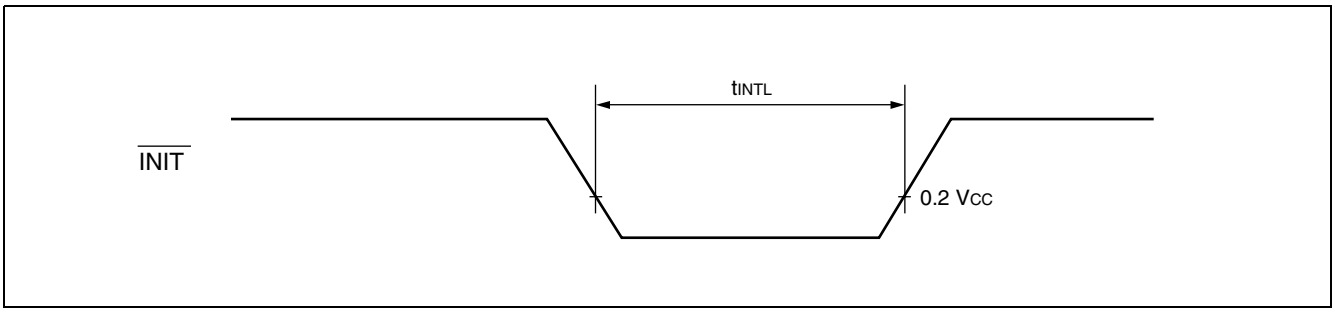
Notes : • Oscillation stabilization time of PLL > 600 µs
• The internal clock gear setting should be within the value shown in clock timing ratings table.

(2) Reset Input Ratings

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{INIT}$ input time (at power-on and STOP mode)	t_{INTL}	$\overline{INIT}$	—	Oscillation time of oscillator + $t_C \times 10$	—	ns	*
$\overline{INIT}$ input time (other than the above)				$t_C \times 10$	—	ns	

* : After the power is stable, L level is kept inputting to $\overline{INIT}$ pin for the duration of approximately 100 µs until the internal power is stabilized.



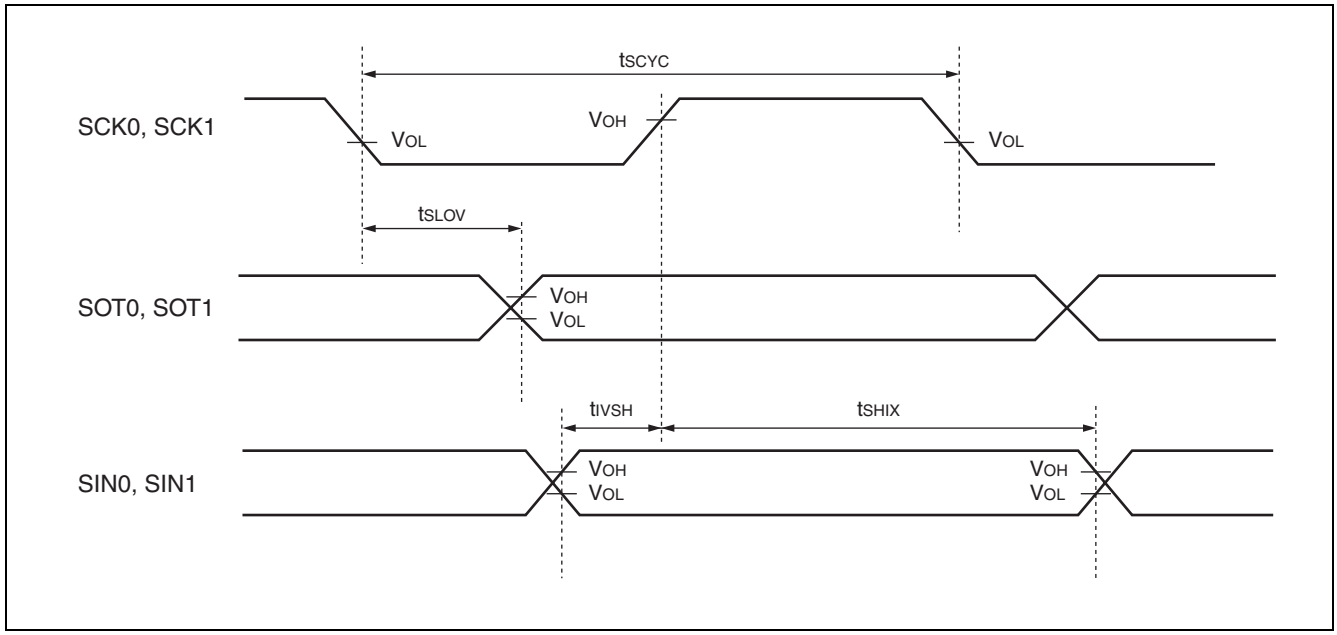
(3) UART Timing

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

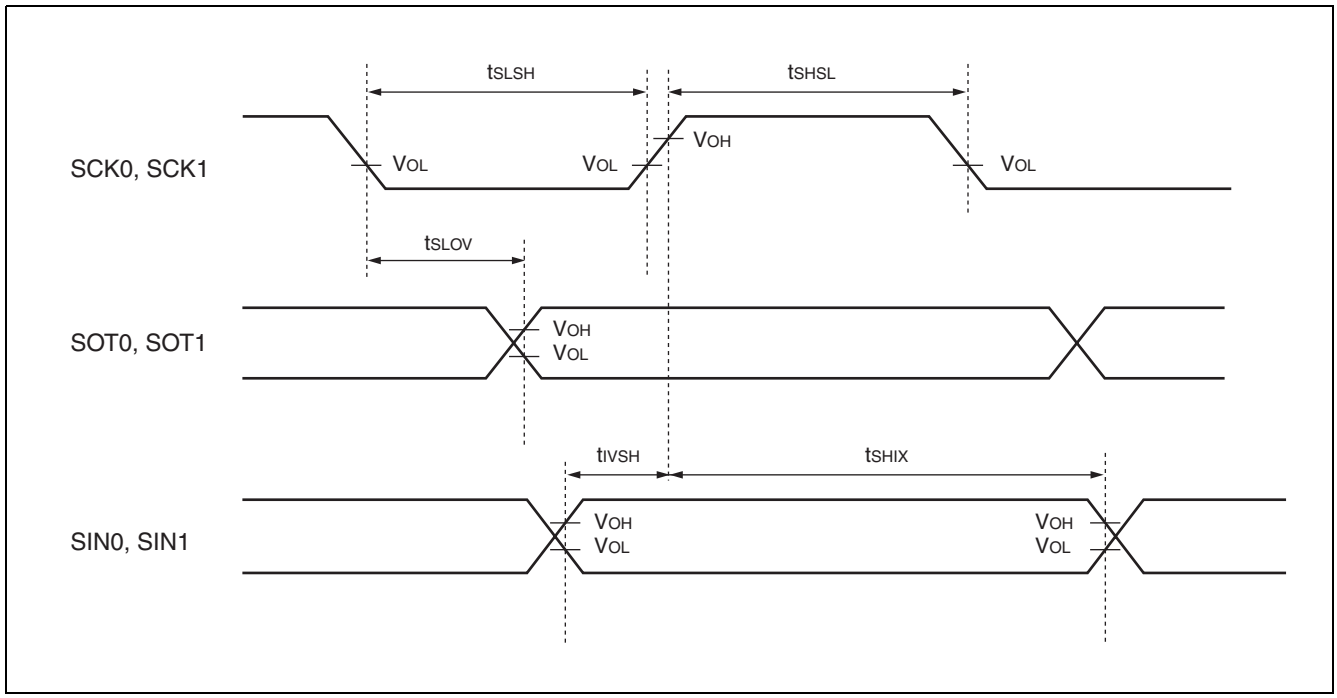
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode	8 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1, SOT0, SOT1		– 80	+ 80	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1, SIN0, SIN1		100	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1, SIN0, SIN1		60	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode	4 t_{CYCP}	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1		4 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1, SOT0, SOT1		—	150	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1, SIN0, SIN1		60	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1, SIN0, SIN1		60	—	ns

Notes : • The above ratings are the values for clock synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.

• Internal shift clock mode



• External shift clock mode

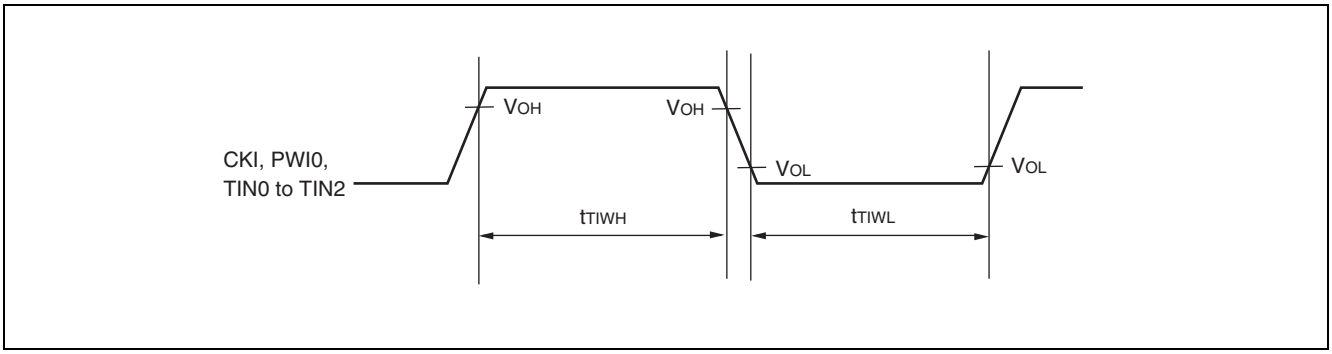


(4) Free-run Timer Clock, PWC Input, and Reload Timer Trigger Timing

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKI, PWI0, TIN0 to TIN2	—	4 t_{CYCP}	—	ns

Note : t_{CYCP} indicates the peripheral clock cycle time.

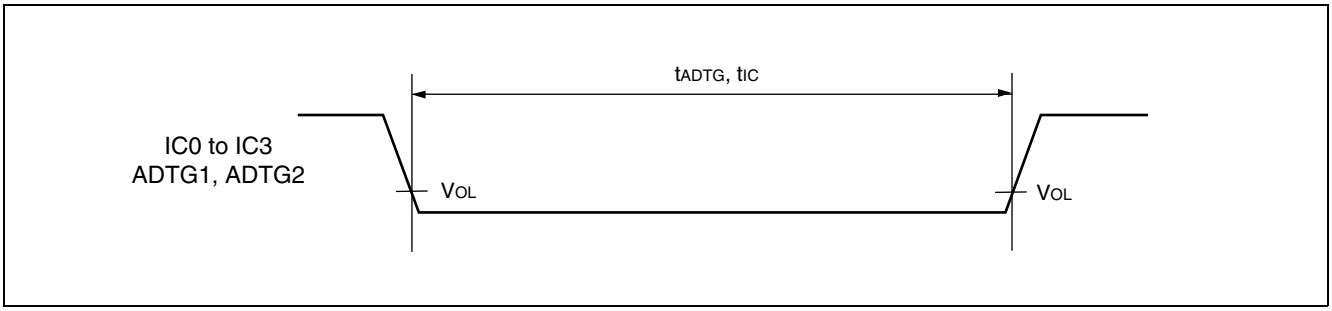


(5) Trigger Input Timing

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input capture trigger input	t_{IC}	IC0 to IC3	—	5 t_{CYCP}	—	ns
A/D Converter activation trigger input	t_{ADTG}	ADTG1, ADTG2	—	5 t_{CYCP}	—	ns

Note : t_{CYCP} indicates the peripheral clock cycle time.



6. Electrical Characteristics for the A/D Converter

(V_{CC} = AVcc = 5.0 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error*1	—	—	– 4	—	+ 4	LSB	At AVRHn*4 = 5.0 V
Linearity error*1	—	—	– 3.5	—	+ 3.5	LSB	
Differential linearity error*1	—	—	– 3	—	+ 3	LSB	
Zero transition voltage*1	V_{OT}	AN0 to AN10	AVss – 3.5LSB	AVss + 0.5LSB	AVss + 4.5LSB	V	
Full transition voltage*1	V_{FST}	AN0 to AN10	AVRH – 5.5LSB	AVRH – 1.5LSB	AVRH + 2.5LSB	V	
Conversion time	—	—	1.2*2	—	—	µs	
Analog port Input current	I_{AIN}	AN0 to AN10	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN10	AVss	—	AVRH	V	
Reference voltage	—	AVRHn*4	AVss	—	AVcc	V	
Analog power supply current (analog + digital)	I_A	AVcc	—	2	—	mA	Per 1 unit
	I_{AH}*3		—	—	100	µA	Per 1 unit
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRHn*4	—	1	—	mA	Per 1 unit AVRHn*4 = 5.0 V, at AV_{SS} = 0 V
	I_{RH}*3		—	—	100	µA	Per 1 unit at STOP
Analog input capacitance	—	—	—	10	—	pF	
Inter-channel disparity	—	AN0 to AN10	—	—	4	LSB	

*1 : Measured in the CPU sleep state

*2 : Vcc = AVcc = 5.0 V, machine clock at 33 MHz

*3 : The current when the CPU is in stop mode and the A/D converter is not operating (at Vcc = AVcc = AVRHn = 5.0 V)

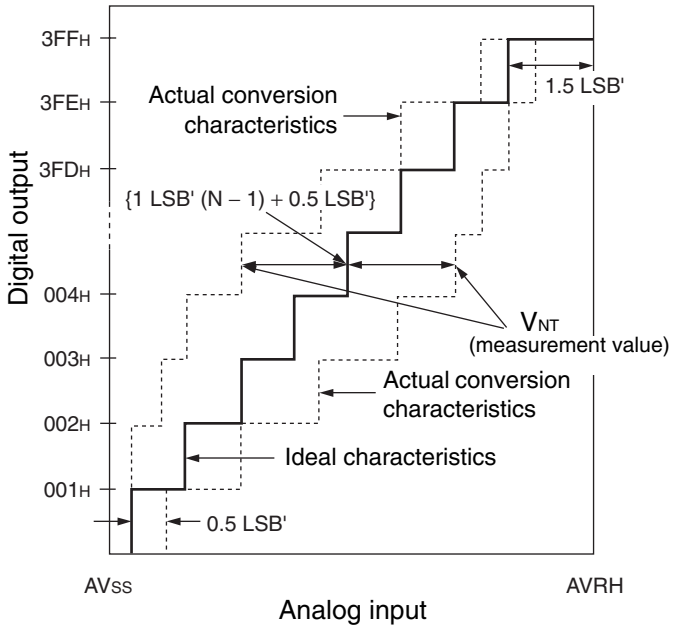
*4: AVRHn = AVRH1, AVRH2

Note : The above does not guarantee the inter-unit accuracy.
Set the output impedance of the external circuit ≤ 2 kΩ.

Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Zero transition point (00 0000 0000 ⟷ 00 0000 0001) and full-scale transition point. Difference between the line connected (11 1111 1110 ⟷ 11 1111 1111) and actual conversion characteristics.
- Differential linearity error : Deviation of input voltage, that is required for changing output code by 1 LSB, from an ideal value.
- Total error : This error indicates the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error..

Total error



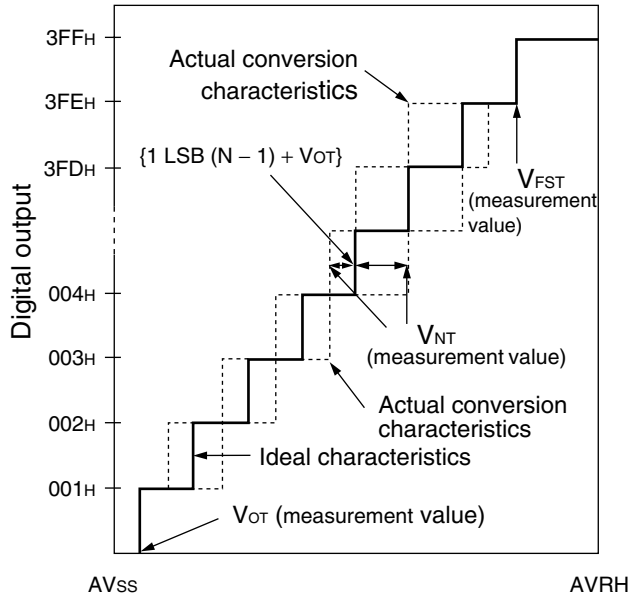
$$1\text{LSB'}\ (\text{Ideal value}) = \frac{AVRH - AV_{SS}}{1024}\ [V] \qquad \text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (N - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from $(N + 1)_H$ to N_H.
V_{OT}' (Ideal value) = AV_{SS} + 0.5LSB' [V]
V_{FST}' (Ideal value) = AVRH – 1.5 LSB' [V]

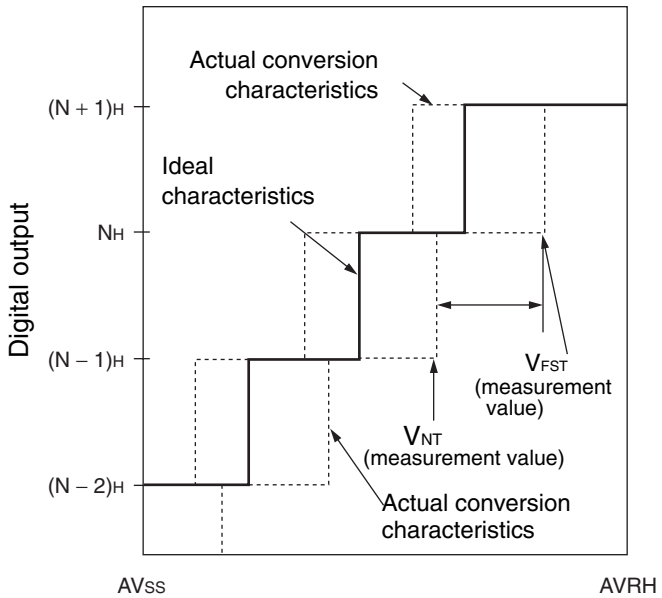
(Continued)

(Continued)

Linearity error



Differential linearity error



$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{ 1\ \text{LSB} \times (N - 1) + V_{OT} \}}{1\ \text{LSB}}\ [\text{LSB}]$$

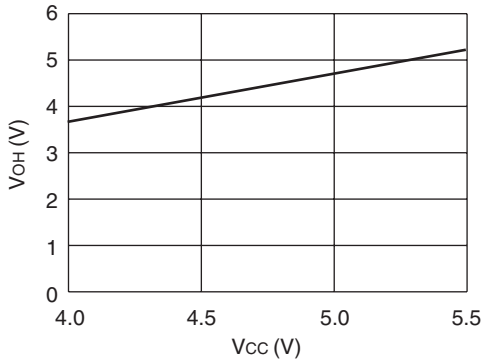
$$\text{Differential linearity error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

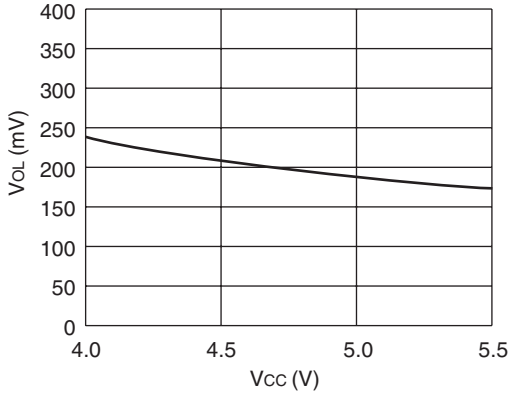
N : A/D converter digital output value
V_{OT} : A voltage at which digital output transits from 000_H to 001_H.
V_{FST} : A voltage at which digital output transits from $3FE_H$ to $3FF_H$.

■ EXAMPLE CHARACTERISTICS

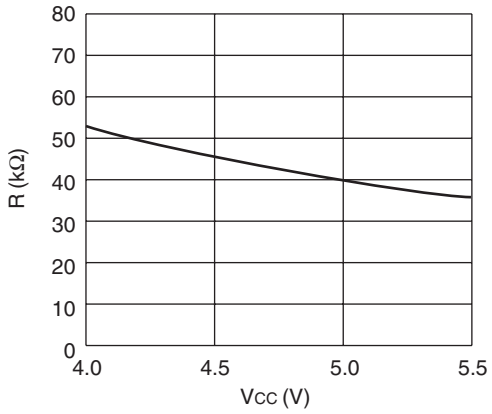
"H" Level Output Voltage vs. Power Supply Voltage



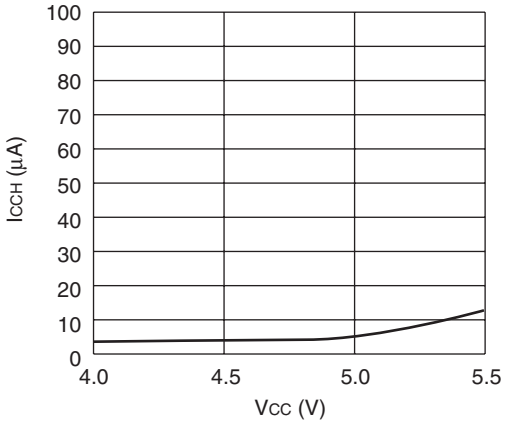
"L" Level Output Voltage vs. Power Supply Voltage



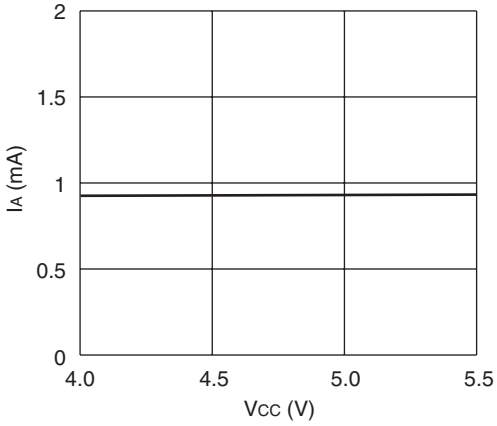
Pull-up Resistor vs. Power Supply Voltage



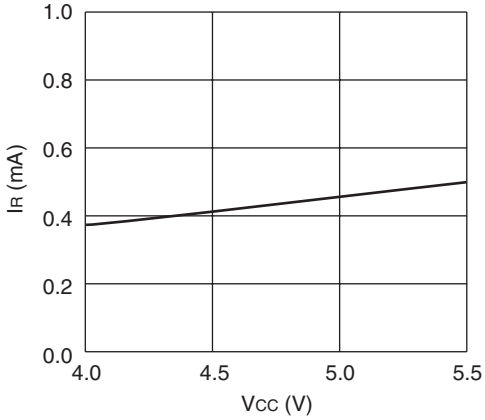
Power Supply Current (at stop) vs. Power Supply Voltage



A/D Conversion Block Per 1 Unit (33 MHz) Analog Power Supply Current vs. Power Supply Voltage



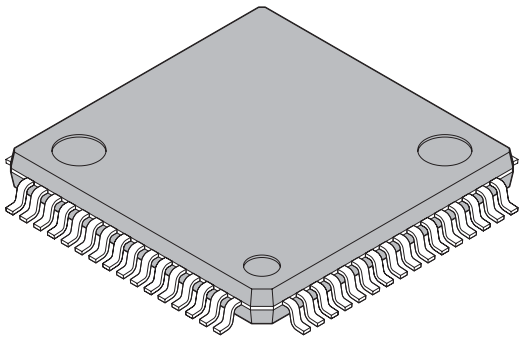
A/D Conversion Block Per 1 Unit (33 MHz) Reference Power Supply Current vs. Power Supply Voltage



■ ORDERING INFORMATION

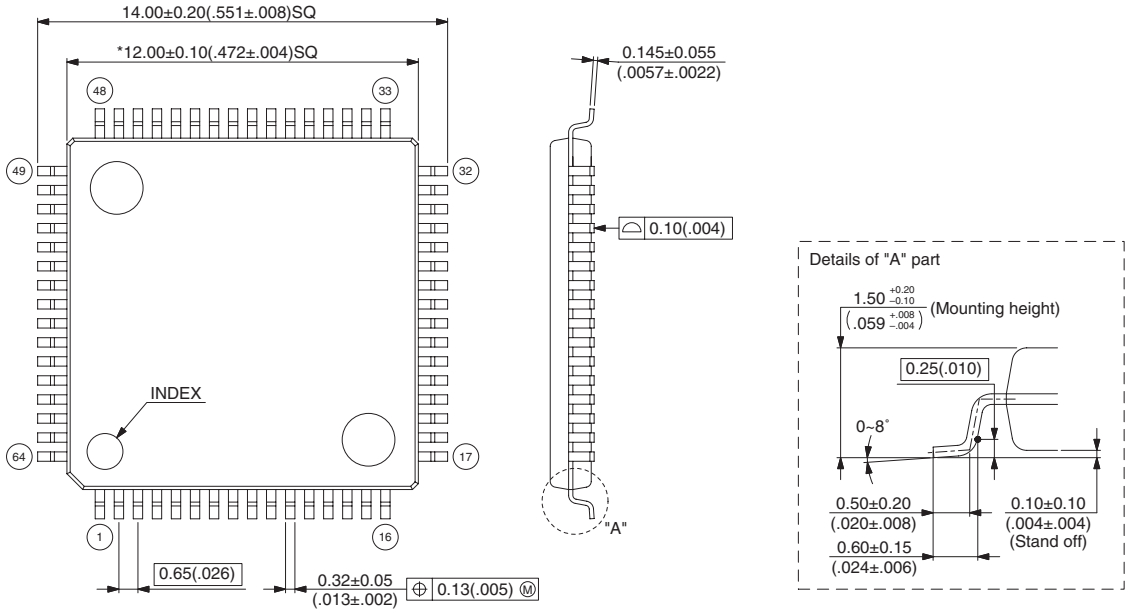
Part number	Package	Remarks
MB91267APMC	64-pin plastic LQFP (FPT-64P-M23)	
MB91267NAPMC		Package loaded C-CAN
MB91F267APMC		
MB91F267NAPMC		Package loaded C-CAN
MB91V265ACR-ES	401-pin ceramic PGA (PGA-401C-A02)	

■ PACKAGE DIMENSION

64-pin plastic LQFP		
 (FPT-64P-M23)	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Deleted the MB91266A (MASK ROM Product) Added the MB91267A and MB91267NA (MASK ROM Product)

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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