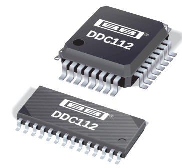
Burr-Brown Products from Texas Instruments

DDC112



SBAS085B – JANUARY 2000 – REVISED OCTOBER 2004

Dual Current Input 20-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **MONOLITHIC CHARGE MEASUREMENT A/D CONVERTER**
- **DIGITAL FILTER NOISE REDUCTION: 3.2ppm, rms**
- **INTEGRAL LINEARITY: ±0.005% Reading ±0.5ppm FSR**
- **HIGH PRECISION, TRUE INTEGRATING FUNCTION**
- **PROGRAMMABLE FULL-SCALE**
- **SINGLE SUPPLY**
- **CASCADABLE OUTPUT**

APPLICATIONS

- **DIRECT PHOTOSENSOR DIGITIZATION**
- **CT SCANNER DAS**
- **INFRARED PYROMETER**
- **PRECISION PROCESS CONTROL**
- **LIQUID/GAS CHROMATOGRAPHY**
- **BLOOD ANALYSIS**

Protected by US Patent #5841310

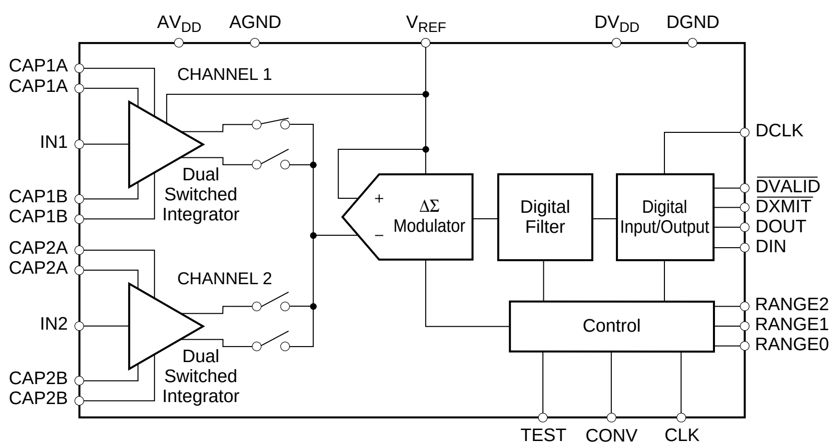
DESCRIPTION

The DDC112 is a dual input, wide dynamic range, charge-digitizing analog-to-digital (A/D) converter with 20-bit resolution. Low-level current output devices, such as photosensors, can be directly connected to its inputs. Charge integration is continuous as each input uses two integrators; while one is being digitized, the other is integrating.

For each of its two inputs, the DDC112 combines current-to-voltage conversion, continuous integration, programmable full-scale range, A/D conversion, and digital filtering to achieve a precision, wide dynamic range digital result. In addition to the internal programmable full-scale ranges, external integrating capacitors allow an additional user-settable full-scale range of up to 1000pC.

To provide single-supply operation, the internal A/D converter utilizes a differential input, with the positive input tied to V_{REF}. When the integration capacitor is reset at the beginning of each integration cycle, the capacitor charges to V_{REF}. This charge is removed in proportion to the input current. At the end of the integration cycle, the remaining voltage is compared to V_{REF}.

The high-speed serial shift register which holds the result of the last conversion can be configured to allow multiple DDC112 units to be cascaded, minimizing interconnections. The DDC112 is available in an SO-28 or TQFP-32 package and is offered in two performance grades.



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ABSOLUTE MAXIMUM RATINGS(1)

AV_{DD} to DV_{DD}	–0.3V to +6V
AV_{DD} to AGND	–0.3V to +6V
DV_{DD} to DGND	–0.3V to +6V
AGND to DGND	±0.3V
V_{REF} Voltage to AGND	–0.3V to AV_{DD} + 0.3V
Digital Input Voltage to DGND	–0.3V to DV_{DD} + 0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} + 0.3V
Package Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum Junction Temperature (T_{JMAX})	+150°C
Thermal Resistance, SO, θ_{JA}	+150°C/W
Thermal Resistance, TQFP, θ_{JA}	+100°C/W
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR	SPECIFICATION TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER(2)	TRANSPORT MEDIA
DDC112U	±0.025% Reading ±1.0ppm FSR	–40°C to +85°C	SO-28	DW	DDC112U	Rails
"	"	"	"	"	DDC112U/1K	Tape and Reel
DDC112UK	±0.025% Reading ±1.0ppm FSR	0°C to +70°C	SO-28	DW	DDC112UK	Rails
"	"	"	"	"	DDC112UK/1K	Tape and Reel
DDC112Y	±0.025% Reading ±1.0ppm FSR	–40°C to +85°C	TQFP-32	PJT	DDC112Y/250	Tape and Reel
"	"	"	"	"	DDC112Y/2K	Tape and Reel
DDC112YK	±0.025% Reading ±1.0ppm FSR	0°C to +70°C	TQFP-32	PJT	DDC112YK/250	Tape and Reel
"	"	"	"	"	DDC112YK/2K	Tape and Reel

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (**/1K** indicates 1000 devices per reel). Ordering 1000 pieces of *DDC112U/1K* will get a single 1000-piece Tape and Reel.

ELECTRICAL CHARACTERISTICS

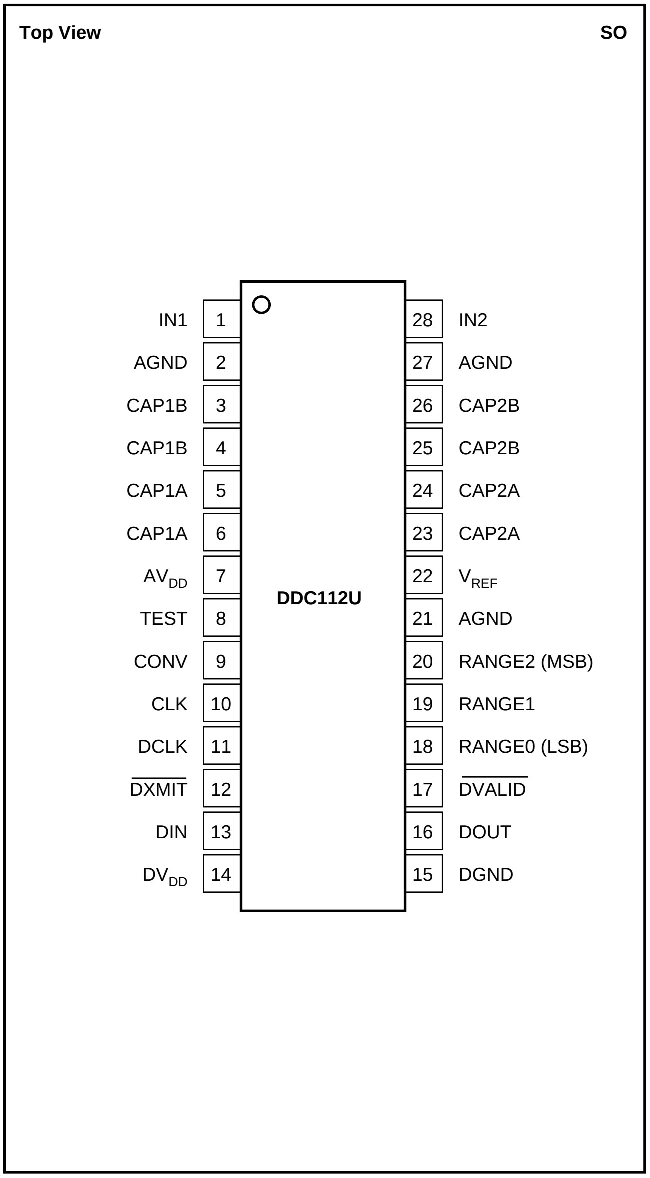
At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, DDC112U, Y: T_{INT} = 500µs, CLK = 10MHz, DDC112UK, YK: T_{INT} = 333.3µs, CLK = 15MHz, V_{REF} = +4.096V, continuous mode operation, and internal integration capacitors, unless otherwise noted.

		DDC112U, Y			DDC112UK, YK			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG INPUTS								
External, Positive Full-Scale								
Range 0	C_{EXT} = 250pF			1000			*	pC
Internal, Positive Full-Scale								
Range 1		47.5	50	52.5	*	*	*	pC
Range 2		95	100	105	*	*	*	pC
Range 3		142.5	150	157.5	*	*	*	pC
Range 4		190	200	210	*	*	*	pC
Range 5		237.5	250	262.5	*	*	*	pC
Range 6		285	300	315	*	*	*	pC
Range 7		332.5	350	367.5	*	*	*	pC
Negative Full-Scale Input			–0.4% of Positive FS			*		pC
DYNAMIC CHARACTERISTICS								
Conversion Rate				2			3	kHz
Integration Time, T_{INT}	Continuous Mode	500		1,000,000	333.3		*	µs
Integration Time, T_{INT}	Non-Continuous Mode	50			*			µs
System Clock Input (CLK)		1	10	12	*	*	15	MHz
Data Clock (DCLK)				12			15	MHz
ACCURACY								
Noise, Low-Level Current Input(1)	C_{SENSOR}(2) = 0pF, Range 5 (250pC)		3.2			*		ppm of FSR(3), rms
	C_{SENSOR} = 25pF, Range 5 (250pC)		3.8			*		ppm of FSR, rms
	C_{SENSOR} = 50pF, Range 5 (250pC)		4.2	6.0		*	7	ppm of FSR, rms
Differential Linearity Error			±0.005% Reading ±0.5ppm FSR (max)				*	
Integral Linearity Error(4)			±0.005% Reading ±0.5ppm FSR (typ)			*		
			±0.025% Reading ±1.0ppm FSR (max)				*	
No Missing Codes			20			*		Bits
Input Bias Current	T_A = +25°C		0.1	10		*	*	pA
Range Error	Range 5 (250pC)			5			*	% of FSR
Range Error Match(5)	All Ranges		0.1	0.5		*	*	% of FSR
Range Sensitivity to V_{REF}	V_{REF} = 4.096 ±0.1V		1:1			*		
Offset Error	Range 5, (250pC)		±200			*	±600	ppm of FSR
Offset Error Match(5)			±100			*		ppm of FSR
DC Bias Voltage(6) (Input V_{OS})			±0.05	±2		*	*	mV
Power-Supply Rejection Ratio			±25	±200		*	*	ppm of FSR/V
Internal Test Signal			13			*		pC
Internal Test Accuracy			±10			*		%
PERFORMANCE OVER TEMPERATURE								
Offset Drift			±0.5				±3(10)	ppm of FSR/°C
Offset Drift Stability			±0.2			*	±0.7(10)	ppm of FSR/minute
DC Bias Voltage Drift	Applied to Sensor Input		3			±1		µV/°C
Input Bias Current Drift	+25°C to +45°C		0.01	1(10)		*	*	pA/°C
Input Bias Current	T_A = +75°C		2	50(10)		*	*	pA
Range Drift(7)	Range 5 (250pC)		25		0	25	50(10)	ppm/°C
Range Drift Match(5)	Range 5 (250pC)		±0.05			*		ppm/°C
REFERENCE								
Voltage		4.000	4.096	4.200	*	*	*	V
Input Current(8)	T_{INT} = 500µs		150			225	275	µA
DIGITAL INPUT/OUTPUT								
Logic Levels								
V_{IH}		4.0		DV_{DD} + 0.3	*		*	V
V_{IL}		–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –500µA	4.5			*			V
V_{OL}	I_{OL} = 500µA			0.4			*	V
Input Current, I_{IN}		–10		+10	*		*	µA
Data Format(9)			Straight Binary			*		
POWER-SUPPLY REQUIREMENTS								
Power-Supply Voltage	AV_{DD} and DV_{DD}	4.75		5.25	*		*	V
Supply Current								
Analog Current	AV_{DD} = +5V		14.8			15.2		mA
Digital Current	DV_{DD} = +5V		1.2			1.8		mA
Total Power Dissipation			80	100		85	130	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	0		+70	°C
Storage		–60		+100	*		*	°C

* Specifications same as DDC112U, Y.

NOTES: (1) Input is less than 1% of full scale. (2) C_{SENSOR} is the capacitance seen at the DDC112 inputs from wiring, photodiode, etc. (3) FSR is Full-Scale Range. (4) A best-fit line is used in measuring linearity. (5) Matching between side A and side B, not input 1 to input 2. (6) Voltage produced by the DDC112 at its input which is applied to the sensor. (7) Range drift does not include external reference drift. (8) Input reference current decreases with increasing T_{INT} (see the *Voltage Reference* section). (9) Data format is Straight Binary with a small offset (see the *Data Retrieval* section). (10) Ensured by design but not production tested.

PIN CONFIGURATION



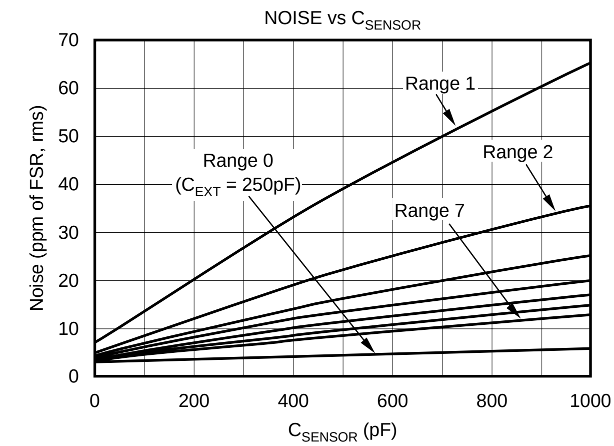
PIN DESCRIPTIONS

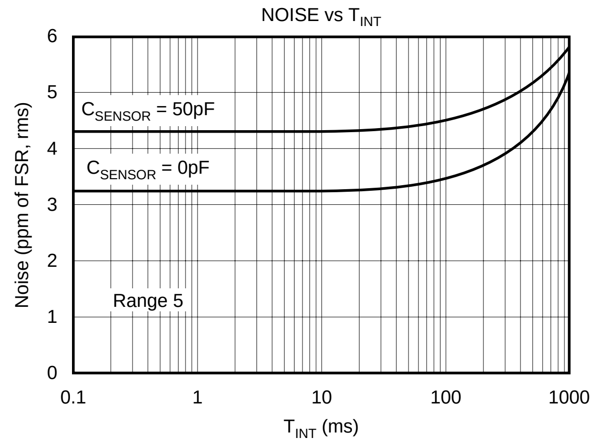
PIN	LABEL	DESCRIPTION
1	IN1	Input 1: analog input for Integrators 1A and 1B. The integrator that is active is set by the CONV input.
2	AGND	Analog Ground
3	CAP1B	External Capacitor for Integrator 1B
4	CAP1B	External Capacitor for Integrator 1B
5	CAP1A	External Capacitor for Integrator 1A
6	CAP1A	External Capacitor for Integrator 1A
7	AV_{DD}	Analog Supply, +5V Nominal
8	TEST	Test Control Input. When HIGH, a test charge is applied to the A or B integrators on the next CONV transition.
9	CONV	Controls which side of the integrator is connected to input. In continuous mode; CONV HIGH $\rightarrow$ side A is integrating, CONV LOW $\rightarrow$ side B is integrating. CONV must be synchronized with CLK (see Figure 2).
10	CLK	System Clock Input, 10MHz Nominal
11	DCLK	Serial Data Clock Input. This input operates the serial I/O shift register.
12	$\overline{\text{DXMIT}}$	Serial Data Transmit Enable Input. When LOW, this input enables the internal serial shift register.
13	DIN	Serial Digital Input. Used to cascade multiple DDC112s.
14	DV_{DD}	Digital Supply, +5V Nominal
15	DGND	Digital Ground
16	DOUT	Serial Data Output, Hi-Z when $\overline{\text{DXMIT}}$ is HIGH
17	$\overline{\text{DVALID}}$	Data Valid Output. A LOW value indicates valid data is available in the serial I/O register.
18	RANGE0	Range Control Input 0 (least significant bit)
19	RANGE1	Range Control Input 1
20	RANGE2	Range Control Input 2 (most significant bit)
21	AGND	Analog Ground
22	V_{REF}	External Reference Input, +4.096V Nominal
23	CAP2A	External Capacitor for Integrator 2A
24	CAP2A	External Capacitor for Integrator 2A
25	CAP2B	External Capacitor for Integrator 2B
26	CAP2B	External Capacitor for Integrator 2B
27	AGND	Analog Ground
28	IN2	Input 2: analog input for Integrators 2A and 2B. The integrator that is active is set by the CONV input.

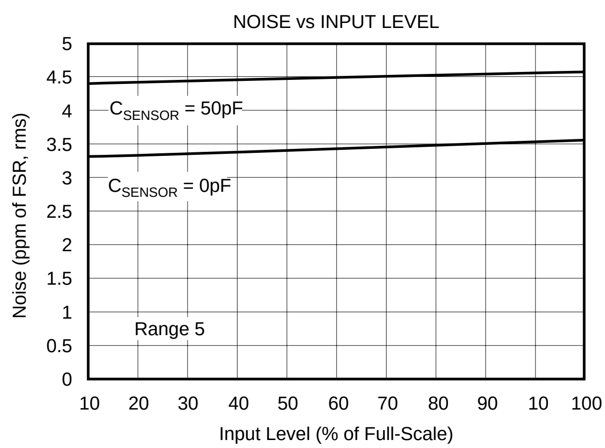
CAP1ACAP1AAVDDNCNCTESTCONVCLKCAP2ACAP2AVREFAGNDNCNCRANGE2 (MSB)RANGE11234567824232221201918l7**DDC11lY**CAP1

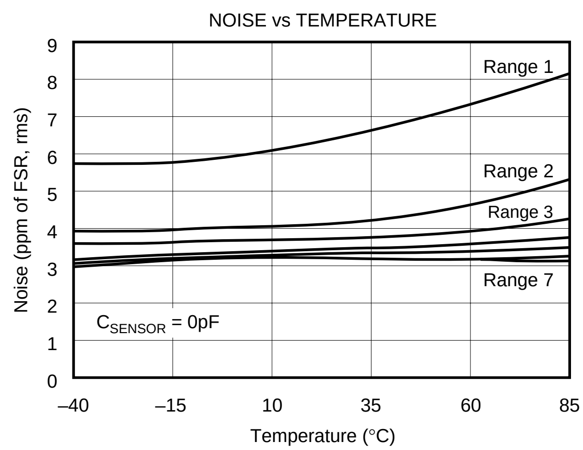
TYPICAL CHARACTERISTICS

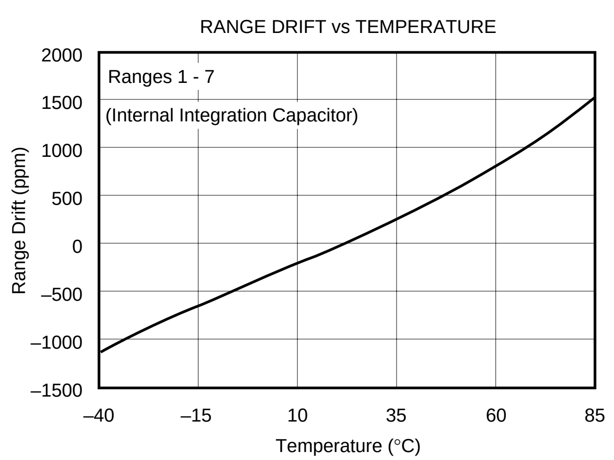
At T_A = +25°C, characterization done with Range 5 (250pC), T_{INT} = 500µs, V_{REF} = +4.096, AV_{DD} = DV_{DD} = +5V, and CLK = 10MHz, unless otherwise noted.

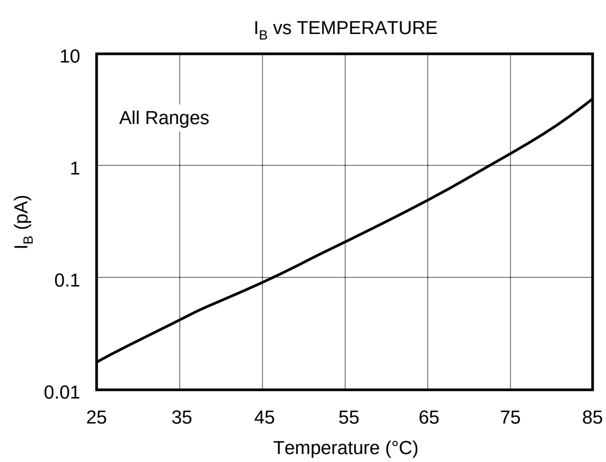












THEORY OF OPERATION

The basic operation of the DDC112 is illustrated in Figure 1. The device contains two identical input channels where each performs the function of current-to-voltage integration followed by a multiplexed analog-to-digital (A/D) conversion. Each input has two integrators so that the current-to-voltage integration can be continuous in time. The output of the four integrators are switched to one delta-sigma ($\Delta\Sigma$) converter via a four input multiplexer. With the DDC112 in the continuous integration mode, the output of the integrators from one side of both of the inputs will be digitized while the other two integrators are in the integration mode as illustrated in the timing diagram in Figure 2. This integration and A/D conversion process is controlled by the system clock, CLK. With a 10MHz system clock, the integrator combined with the delta-sigma converter accomplishes a single 20-bit conversion in approximately 220µs. The results from side A and side B of each signal input are stored in a serial output shift register. The $\overline{\text{DVALID}}$ output goes LOW when the shift register contains valid data.

The digital interface of the DDC112 provides the digital results via a synchronous serial interface consisting of a data clock (DCLK), a transmit enable pin ($\overline{\text{DXMIT}}$), a valid data pin ($\overline{\text{DVALID}}$), a serial data output pin (DOUT), and a serial data input pin (DIN). The DDC112 contains only one A/D converter, so the conversion process is interleaved between the two inputs, as shown in Figure 2. The integration and conversion process is fundamentally independent of the data retrieval process. Consequently, the CLK frequency and DCLK frequencies need not be the same. DIN is only used when multiple converters are cascaded and should be tied to DGND otherwise. Depending on T_{INT}, CLK, and DCLK, it is possible to daisy-chain over 100 converters. This greatly simplifies the interconnection and routing of the digital outputs in cases where a large number of converters are needed.

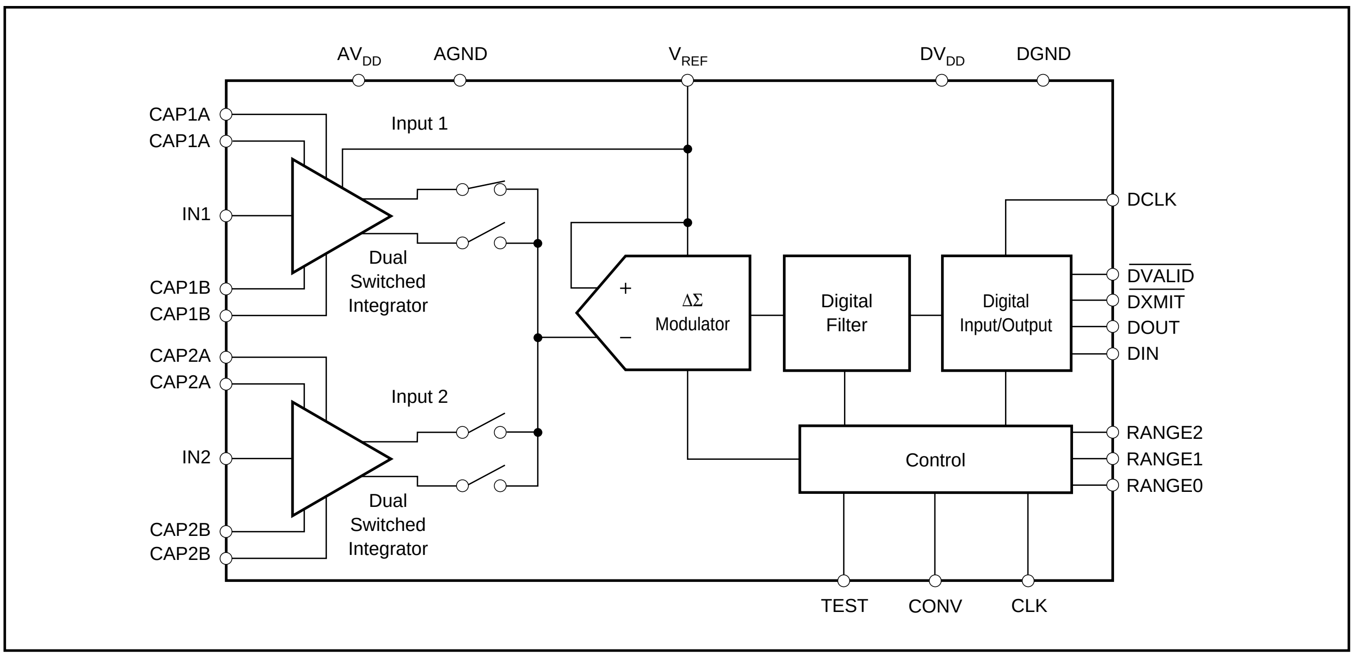


FIGURE 1. Block Diagram.

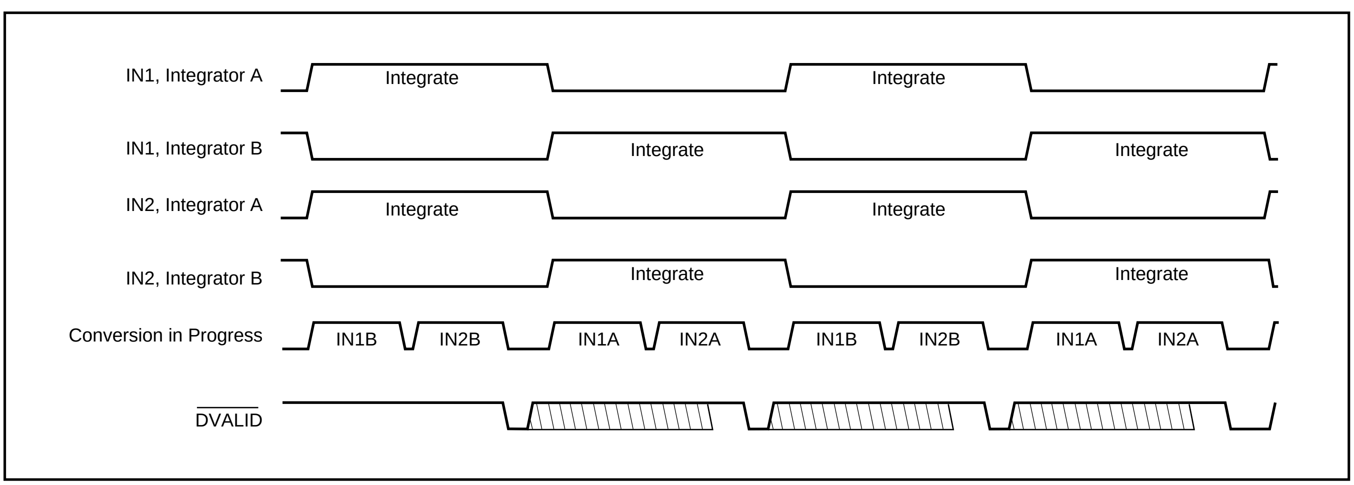


FIGURE 2. Basic Integration and Conversion Timing for the DDC112 (continuous mode).

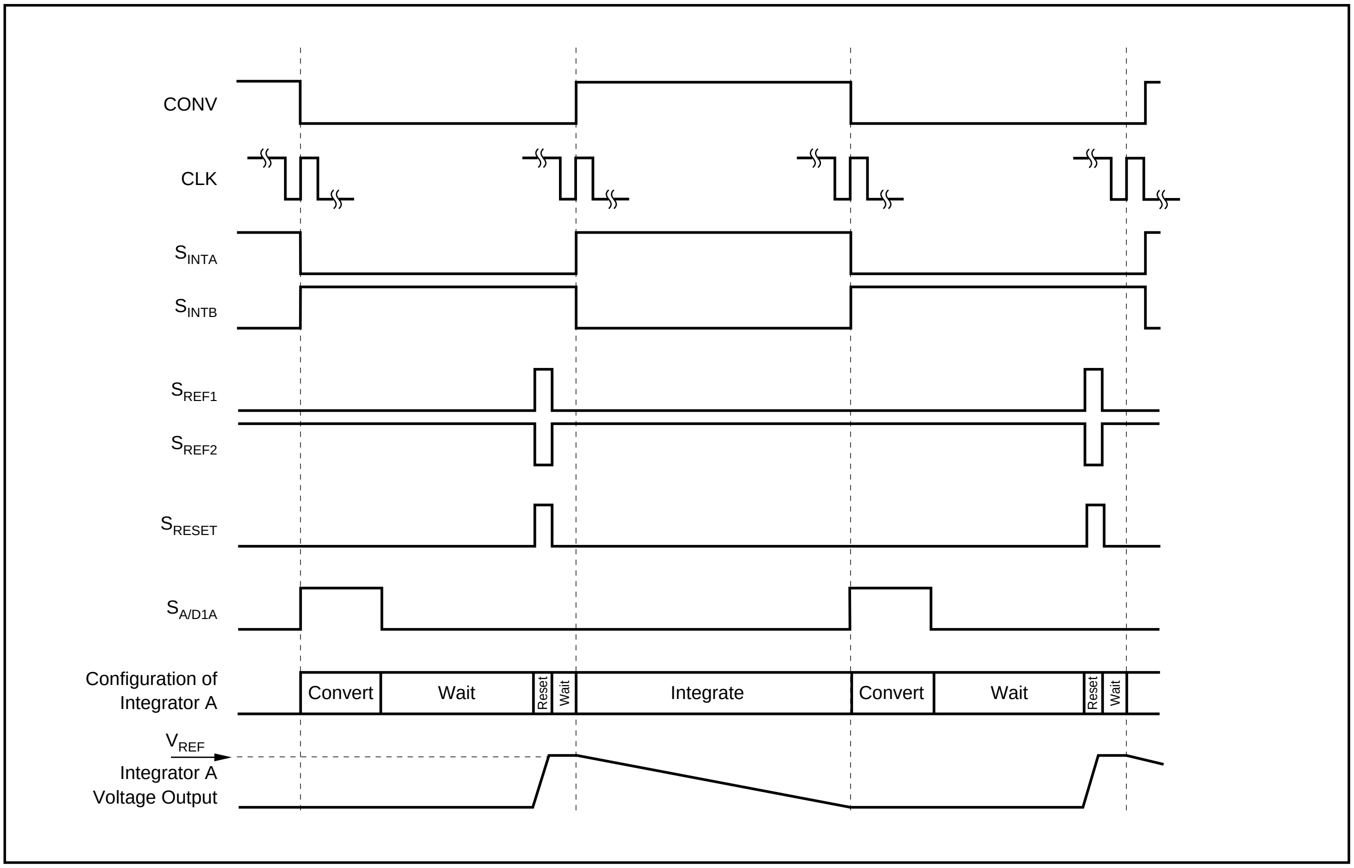


FIGURE 4. Basic Integrator Timing Diagram as Illustrated in Figure 3.

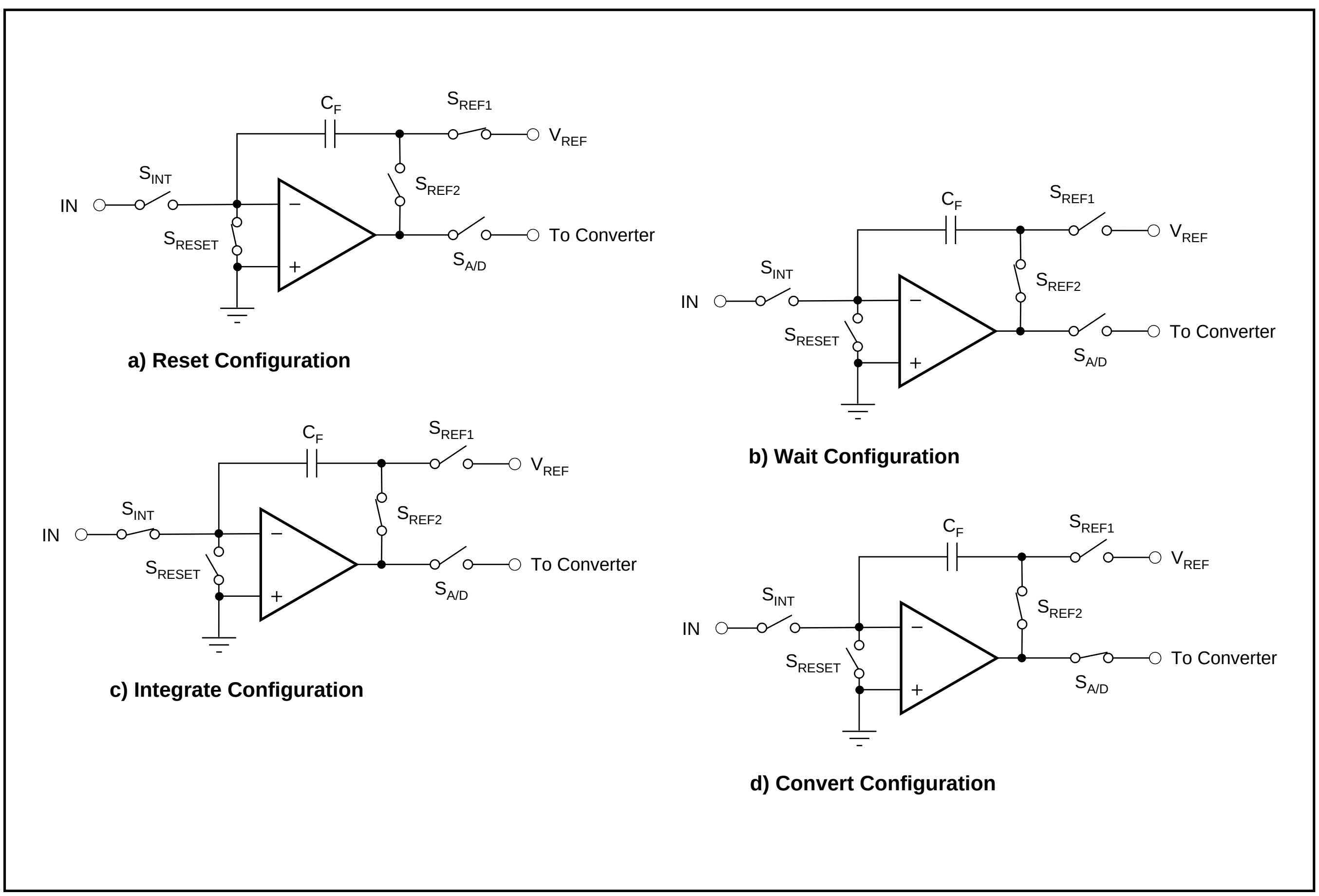


FIGURE 5. Diagrams for the Four Configurations of the Front End Integrators of the DDC112.

SBAS085Bwww.ti.comDetermining the Integration Capacitor (CF) ValueThe value of the integrator's feedback capacitor, the integra-tion period, and the reference voltag

A low-pass filter to reduce noise connects it to an operational amplifier configured as a buffer. This amplifier should have a unity-gain bandwidth greater than 4MHz, low noise, and input/output common-mode ranges that support V_{REF}. Following the buffer are capacitors placed close to the DDC112 V_{REF} pin. Even though the circuit in Figure 6 might appear to be unstable due to the large output capacitors, it works well for most operational amplifiers. It is NOT recommended that series resistance be placed in the output lead to improve stability since this can cause droop in V_{REF} which produces large offsets.

DDC112 Frequency Response

The frequency response of the DDC112 is set by the front end integrators and is that of a traditional continuous time integrator, as shown in Figure 7. By adjusting T_{INT}, the user can change the 3dB bandwidth and the location of the notches in the response. The frequency response of the $\Delta\Sigma$ converter that follows the front end integrator is of no consequence because the converter samples a held signal from the integrators. That is, the input to the $\Delta\Sigma$ converter is always a DC signal. Since the output of the front end integrators are sampled, aliasing can occur. Whenever the frequency of the input signal exceeds one-half of the sampling rate, the signal will *fold* back down to lower frequencies.

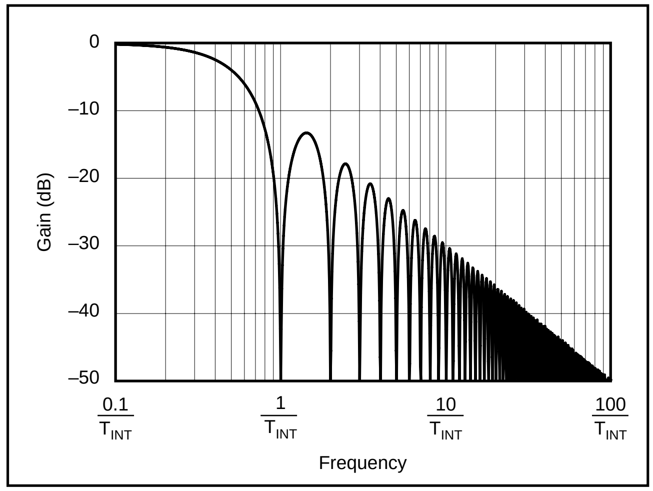


FIGURE 7. Frequency Response of the DDC112.

Test Mode

When TEST is used, pins IN1 and IN2 are grounded and *packets* of approximately 13pC charge are transferred to the integration capacitors of both Input 1 and Input 2. This fixed charge can be transferred to the integration capacitors either once during an integration cycle or multiple times. In the case where multiple packets are transferred during one integration period, the 13pC charge is additive. This mode can be used in both the continuous and noncontinuous mode timing. The timing diagrams for test mode are shown in Figure 8. The top three lines in Figure 8 define the timing when one packet of 13pC is sent to the integration capacitors. The bottom three lines define the timing when multiple packets are sent to the integration capacitors.

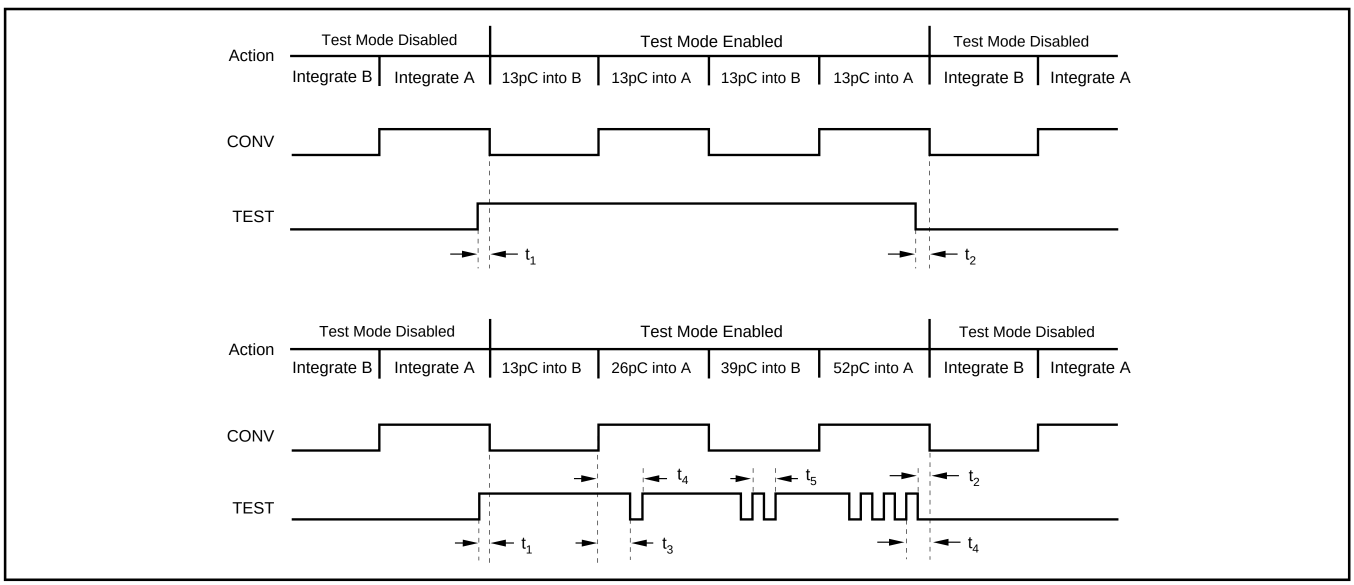


FIGURE 8. Timing Diagram of the Test Mode of the DDC112.

SYMBOL	DESCRIPTION	CLK = 10MHz			CLK = 15MHz			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_1	Setup Time for Test Mode Enable	100			100			ns
t_2	Setup Time for Test Mode Disable	100			100			ns
t_3	Hold Time for Test Mode Enable	100			100			ns
t_4	From Rising Edge of TEST to the Edge of CONV while Test Mode Enabled	5.4			3.6			µs
t_5	Rising Edge to Rising Edge of TEST	5.4			3.6			µs

TABLE III. Timing for the DDC112 in the Test Mode.

During the cont mode, mbsy is not active when CONV toggles. The non-integrating side is always ready to begin integrating when the other side finishes its integration. Consequently, keeping track of the current status of CONV is all that is needed to know the current state. Cont mode operation corresponds to states 3-6. Two of the states, 3 and 6, only perform an integration (no m/r/az cycle).

mbsy becomes important when operating in the ncont mode; states 1, 2, 7, and 8. Whenever CONV is toggled while mbsy is active, the DDC112 will enter or remain in either ncont state 1 (or 8). After mbsy goes inactive, state 2 (or 7) is entered. This state prepares the appropriate side for integration. As mentioned above, in the ncont states, the inputs to the DDC112 are grounded.

One interesting observation from the state diagram is that the integrations always alternate between sides A and B. This relationship holds for any CONV pattern and is independent of the mode. States 2 and 7 insure this relationship during the ncont mode.

When power is first applied to the DDC112, the beginning state is either 1 or 8, depending on the initial level of CONV. For CONV held HIGH at power-up, the beginning state is 1. Conversely, for CONV held LOW at power-up, the beginning state is 8. In general, there is a symmetry in the state diagram between states 1-8, 2-7, 3-6, and 4-5. Inverting CONV results in the states progressing through their symmetrical match.

TIMING EXAMPLES

Cont Mode

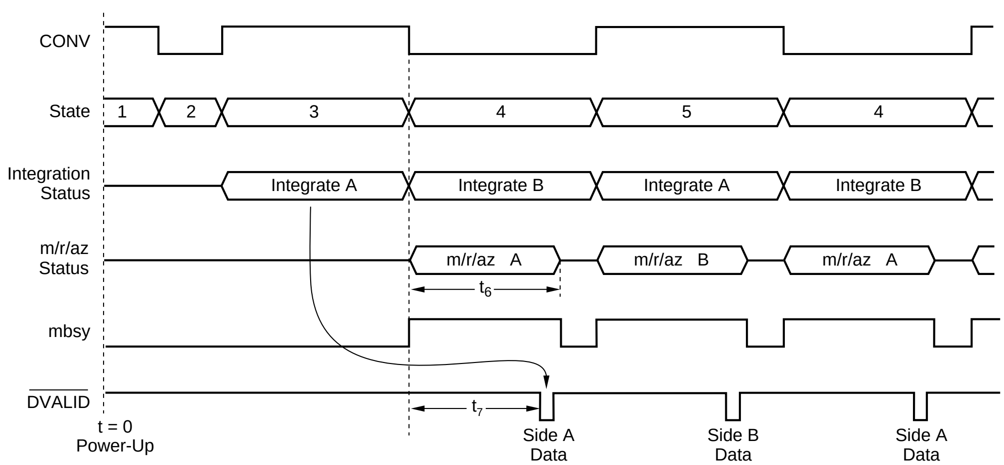
A few timing diagrams will now be discussed to help illustrate the operation of the state machine. These are shown in Figures 10 through 19. Table V gives generalized timing specifications in units of CLK periods. Values in µs for Table V can be easily found for a given CLK. For example, if CLK = 10MHz, then a CLK period = 0.1µs. t_6 in Table V would then be 479.4µs.

SYMBOL	DESCRIPTION	VALUE (CLK periods)	
t_6	Cont mode m/r/az cycle.	4794	
t_7	Cont mode data ready.	4212	(t_{INT} > 4794)
		4212 ±3	(t_{INT} = 4794)
t_8	1st ncont mode data ready.	4212 ±3	
t_9	2nd ncont mode data ready.	4548	
t_{10}	Ncont mode m/r/az cycle.	9108	

TABLE V. Timing Specifications Generalized in CLK Periods.

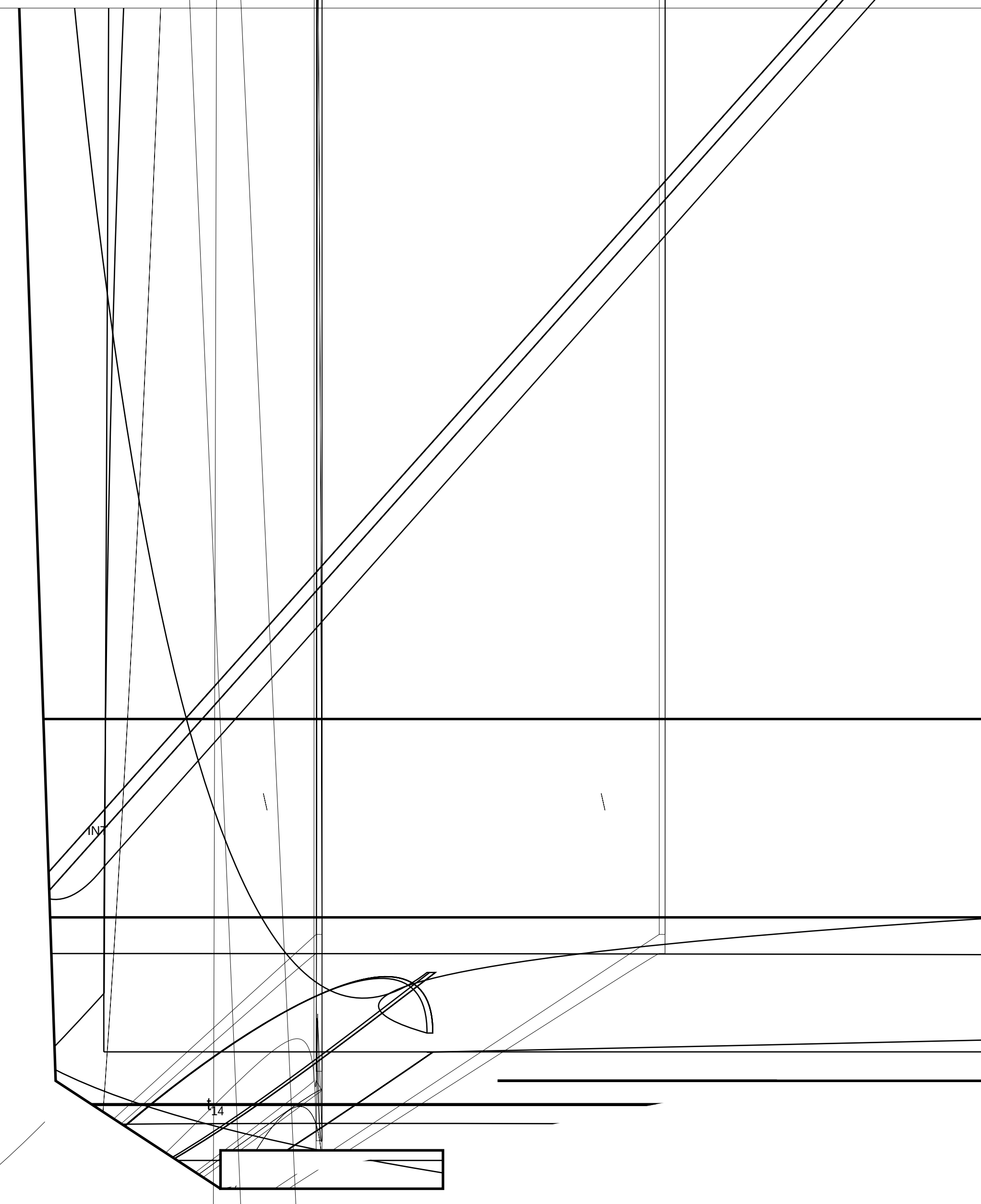
Figure 10 shows a few integration cycles beginning with initial power-up for a cont mode example. The top signal is CONV and is supplied by the user. The next line indicates the current state in the state diagram. The following two traces show when integrations and measurement cycles are underway. The internal signal mbsy is shown next. Finally, $\overline{\text{DVALID}}$ is given. As described in the data sheet, $\overline{\text{DVALID}}$ goes active LOW when data is ready to be retrieved from the DDC112. It stays LOW until $\overline{\text{DXMIT}}$ is taken LOW by the user. In Figure 10 and the following timing diagrams, it is assumed that $\overline{\text{DXMIT}}$ it taken LOW soon after $\overline{\text{DVALID}}$ goes LOW. The text below the $\overline{\text{DVALID}}$ pulse indicates the side of the data and arrows help match the data to the corresponding integration. The signals shown in Figures 10 through 19 are drawn at approximately the same scale.

In Figure 10, the first state is ncont state 1. The DDC112 always powers up in the ncont mode. In this case, the first state is 1 because CONV is initially HIGH. After the first two states, cont mode operation is reached and the states begin toggling between 4 and 5. From now on, the input is being continuously integrated, either by side A or side B. The time needed for the m/r/az cycle, t_6, is the same time that



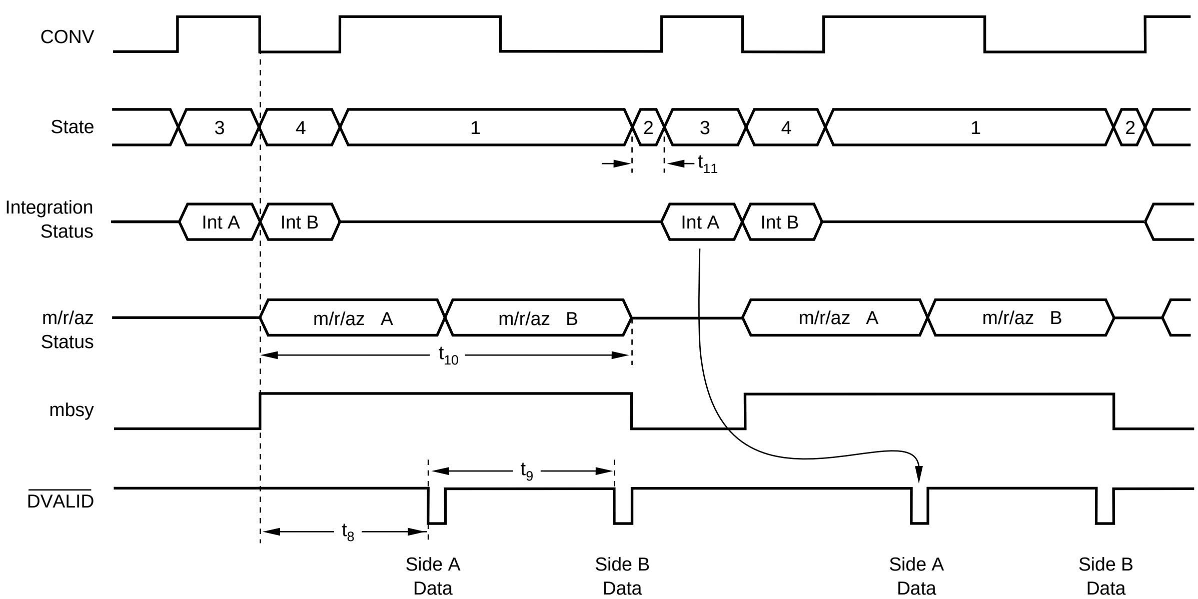
SYMBOL	DESCRIPTION	VALUE (CLK = 10MHz)		VALUE (CLK = 15MHz)	
t_6	Cont mode m/r/az cycle.	479.4µs		319.6µs	
t_7	Cont mode data ready.	421.2µs	(T_{INT} > 479.4µs)	280.8µs	(T_{INT} > 319.6µs)
		421.2 ±0.3µs	(T_{INT} = 479.4µs)	280.8 ±0.2µs	(T_{INT} = 319.6µs)

FIGURE 10. Continuous Mode Timing (CONV HIGH at power-up).


t14

Ncont Mode

Figure 13 illustrates operation in the ncont mode. The integrations come in pairs (that is, sides A/B or sides B/A) followed by a time during which no integrations occur. During that time, the previous integrations are being measured, reset and auto-zeroed. Before the DDC112 can advance to states 3 or 6, both sides A and B must be finished with the m/r/az cycle which takes time t_{10}. When the m/r/az cycles are completed, time t_{11} is needed to prepare the next side for integration. This time is required for the ncont mode because the m/r/az cycle of the ncont mode is slightly different from that of the cont mode. After the first integration ends, $\overline{\text{DVALID}}$ goes LOW in time t_8. This is the same time as in the cont mode. The second data will be ready in time t_9 after the first data is ready. One result of the naming convention used in this application bulletin is that when the DDC112 is operating in the *ncont mode*, it passes through both *ncont mode states* and *cont mode states*. For example, in Figure 13, the state pattern is 3, 4, 1, 2, 3, 4, 1, 2, 3, 4...where 3 and 4 are cont mode states. *Ncont mode* by definition means that for some portion of the time, neither side A nor B is integrating. States that perform an integration are labeled *cont mode states* while those that do not are called *ncont mode states*. Since integrations are performed in the ncont mode, just not continuously, some cont mode states must be used in an ncont mode state pattern.



SYMBOL	DESCRIPTION	VALUE (CLK = 10MHz)	VALUE (CLK = 15MHz)
t_8	1st ncont mode data ready.	421.2 ±0.3µs	280.8 ±0.2µs
t_9	2nd ncont mode data ready.	454.8µs	303.2µs
t_{10}	Ncont mode m/r/az cycle.	910.8µs	607.2µs
t_{11}	Prepare side for integration.	≥ 24.0µs	≥ 24.0µs

FIGURE 13. Non-Continuous Mode Timing.

[redacted]

Looking at the state diagram, one can see that the CONV pattern needed to generate a given state progression is not unique. Upon entering states 1 or 8, the DDC112 remains in those states until mbsy goes LOW, independent of CONV. As long as the m/r/az cycle is underway, the state machine ignores CONV (see Figure 9). The top two signals are different CONV patterns that produce the same state. This feature can be a little confusing at first, but it does allow flexibility in generating ncont mode CONV patterns. For example, the DDC112 Evaluation Fixture operates in the ncont mode by generating a square wave with pulse width < t_6. Figure 17 illustrates operation in the ncont mode using a 50% duty cycle CONV signal with T_{INT} = 1620 CLK periods. Care must be exercised when using a square wave to generate CONV. There are certain integration times that must be avoided since they produce very short intervals for state 2 (or state 7 if CONV is inverted). As seen in the state diagram, the state progresses from 2 to 3 as soon as CONV is HIGH. The state machine does not insure that the duration of state 2 is long enough to properly prepare the next side for integration (t_{11}). This must be done by the user with proper timing of CONV. For example, if CONV is a square wave with T_{INT} = 3042 CLK periods, state 2 will only be 18 CLK periods long, therefore, t_{11} will not be met.

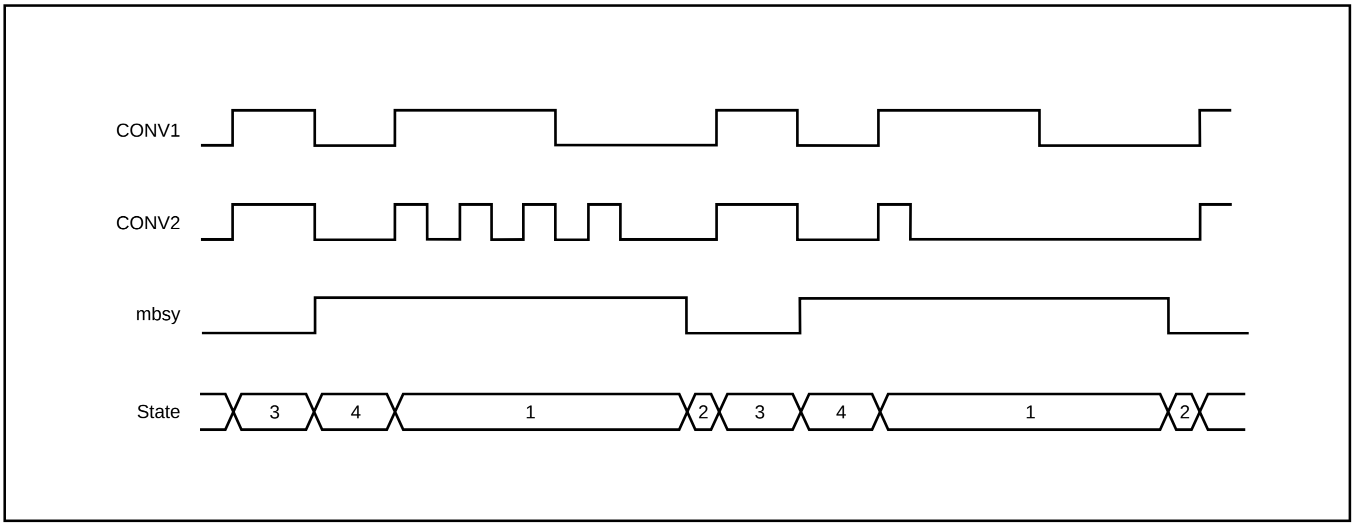


FIGURE 16. Equivalent CONV Signals in Non-Continuous Mode.

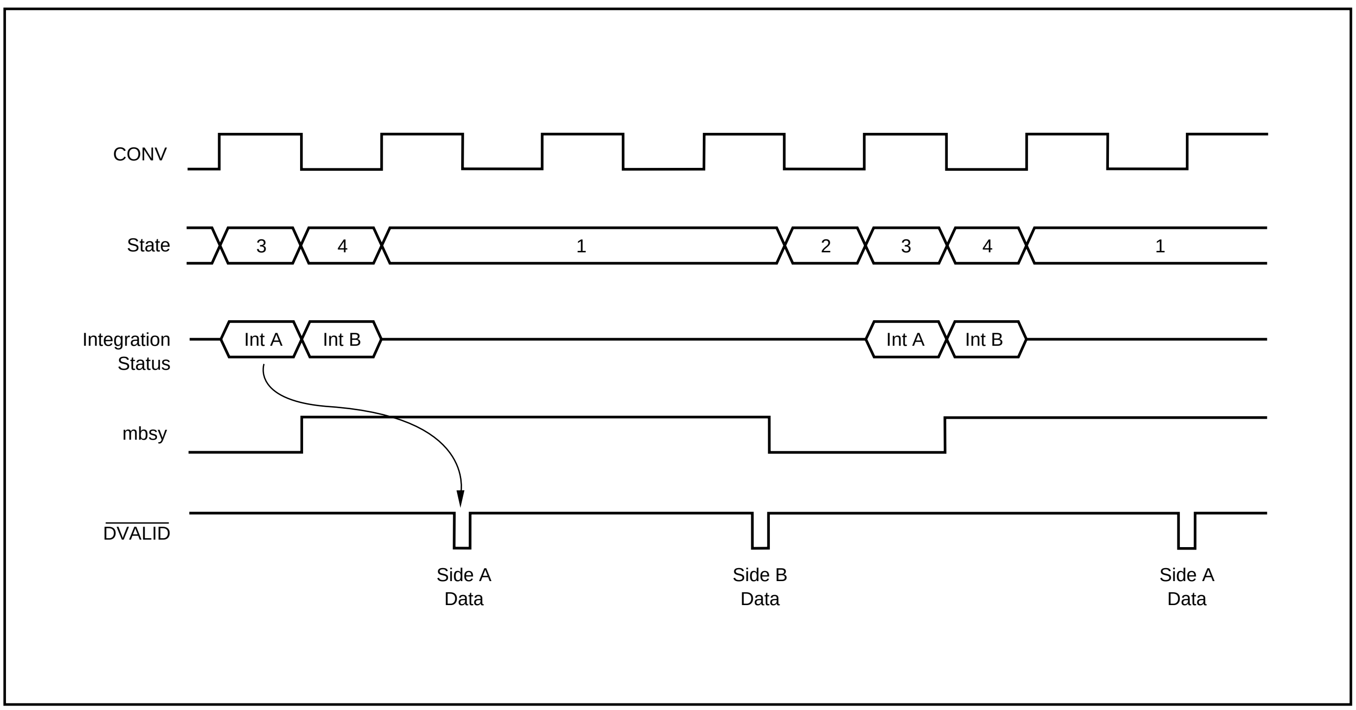


FIGURE 17. Non-Continuous Mode Timing with a 50% Duty Cycle CONV Signal.

SPECIAL CONSIDERATIONS

NCONT MODE INTEGRATION TIME

The DDC112 uses a relatively fast clock. For CLK = 10MHz, this allows T_{INT} to be adjusted in steps of 100ns since CONV should be synchronized to CLK. However, for the internal measurement, reset and auto-zero operations, a slower clock is more efficient. The DDC112 divides CLK by six and uses this slower clock with a period of 600ns to run the m/r/az cycle and data ready logic.

Because of the divider, it is possible for the integration time to be a non-integer number of slow clock periods. For example, if T_{INT} = 5000 CLK periods (500µs for CLK = 10MHz), there will be 833 1/3 slow clocks in an integration period. This non-integer relationship between T_{INT} and the slow clock period causes the number of rising and falling slow clock edges within an integration period to change from integration to integration. The digital coupling of these edges to the integrators will in turn change from integration to integration which produces noise. The change in the clock edges is not random, but will repeat every 3 integrations. The coupling noise on the integrators appears as a tone with a frequency equal to the rate at which the coupling repeats.

To avoid this problem in cont mode, the internal slow clock is shut down after the m/r/az cycle is complete when it is no longer needed. It starts up again just after the next integration begins. Since the slow clock is always off when CONV toggles, the same number of slow clock edges fall within an integration period regardless of its length. Therefore, $T_{INT} \geq 4794$ CLK periods will not produce the coupling problem described above.

For the ncont mode however, the slow clock must always be left running. The m/r/az cycle is not completed before an integration ends. It is then possible to have digital coupling to the integrators. The digital coupling noise depends heavily on the layout of the printed circuit board used for the DDC112. For solid grounds and power supplies with good bypassing, it is possible to greatly reduce the coupling. However, for ensuring the best performance in the ncont mode, the integration time should be chosen to be an integer multiple of $1/(2f_{SLOWCLOCK})$. For CLK = 10MHz, the integration time should be an integer multiple of 300ns—T_{INT} = 100µs is not. A better choice would be T_{INT} = 99µs.

DATA READY

The $\overline{\text{DVALID}}$ signal which indicates that data is ready is generated using the internal slow clock. The phase relationship between this clock and CLK is set when power is first applied and is random. Since CONV is synchronized with CLK, it will have a random phase relationship with respect to the slow clock. When $T_{INT} > t_6$, the slow clock will temporarily shut down as described above. This shutdown process synchronizes the internal clock with CONV so that the time between when CONV toggles to when $\overline{\text{DVALID}}$ goes LOW (t_7 and t_8) is fixed.

For $T_{INT} \leq t_6$, the internal slow clock, is not allowed to shut down and the synchronization never occurs. Therefore, the time between CONV toggling and $\overline{\text{DVALID}}$ indicating data is ready has uncertainty due to the random phase relationship between CONV and the slow clock. This variation is $\pm 1/(2f_{SLOWCLOCK})$ or $\pm 3/f_{CLK}$. The timing to the second $\overline{\text{DVALID}}$ in the ncont mode will not have a variation since it is triggered off the first data ready (t_9) and both are derived from the slow clock.

Polling $\overline{\text{DVALID}}$ to determine when data is ready eliminates any concern about the variation in timing since the readback is automatically adjusted as needed. If the data readback is triggered off the toggling of CONV directly (instead of polling), then waiting the maximum value of t_7 or t_8 insures that data will always be ready before readback occurs.

Data Retrieval

In the continuous and noncontinuous modes of operation, the data from the last conversion is available for retrieval with the falling edge of $\overline{\text{DVALID}}$ (see Figure 22). The falling edge of $\overline{\text{DXMIT}}$ in combination with the data clock (DCLK) will initiate the serial transmission of the data from the DDC112. Typically, data is retrieved from the DDC112 as soon as $\overline{\text{DVALID}}$ falls and completed before the next CONV transition from HIGH to LOW or LOW to HIGH occurs. If this is not the case, care should be taken to stop activity on DCLK and consequently DOUT by at least 10µs around a CONV transition. If this caution is ignored it is possible that the integration that is being initiated by CONV will have additional noise introduced.

The serial output data at DOUT is transmitted in Straight Binary Code per Table VIII. An output offset has been built into the DDC112 to allow for the measurement of input signals near and below zero. Board leakage up to ≈ –0.4% of the positive full-scale can be tolerated before the digital output clips to all zeroes.

CODE	INPUT SIGNAL
1111 1111 1111 1111 1111	FS
1111 1111 1111 1111 1110	FS – 1LSB
0000 0001 0000 0000 0001	+1LSB
0000 0001 0000 0000 0000	Zero
0000 0000 0000 0000 0000	–0.4% FS

TABLE VIII. Straight Binary Code Table.

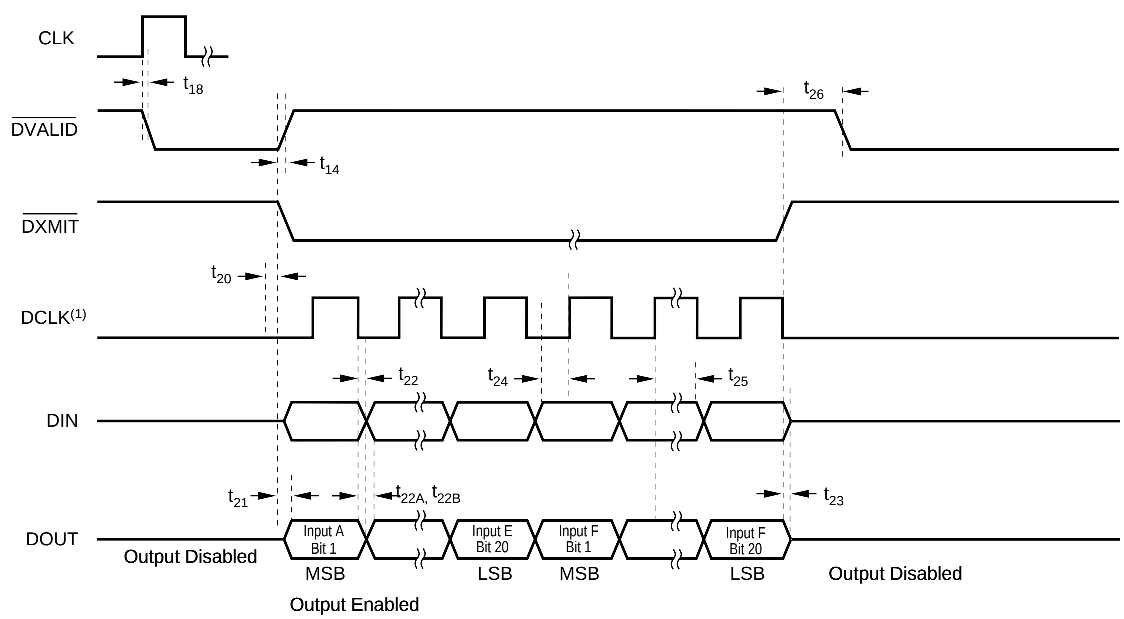
Cascading Multiple Converters

Multiple DDC112 units can be connected in serial or parallel configurations, as illustrated in Figures 20 and 21.

DOUT can be used with DIN to *daisy-chain* several DDC112 devices together to minimize wiring. In this mode of operation, the serial data output is shifted through multiple DDC112s, as illustrated in Figure 20.

R_{PULLUP} prevents DIN from floating when $\overline{\text{DXMIT}}$ is HIGH. Care should be taken to keep the capacitive load on DOUT as low as possible when running CLK=15MHz.

Daisy-Chained DDC112s.IN1IN2DC DXMIT



NOTE: (1) Disable DCLK (preferably LOW) when $\overline{DXMIT}$ is HIGH.

FIGURE 23. Timing Diagram When Using the DIN Function of the DDC112.

SYMBOL	DESCRIPTION	CLK = 10MHz			CLK = 15MHz			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{24}	Set-Up Time From DIN to Rising Edge of DCLK	10			5			ns
t_{25}	Hold Time For DIN After Rising Edge of DCLK	10			10			ns
t_{26}	Hold Time for $\overline{DXMIT}$ HIGH Before Falling Edge of $\overline{DVALID}$	2			1.33			µs

TABLE X. Timing for the DDC112 Data Retrieval Using DIN.

RETRIEVAL *BEFORE* CONV TOGGLES (CONTINUOUS MODE)

This is the most straightforward method. Data retrieval begins soon after $\overline{DVALID}$ goes LOW and finishes before CONV toggles, see Figure 24. For best performance, data retrieval must stop t_{28} before CONV toggles. This method is the most appropriate for longer integration times. The maximum time available for readback is $T_{INT} - t_{27} - t_{28}$. For DCLK and CLK = 10MHz, the maximum number of DDC112s that can be daisy-chained together is:

$$\frac{T_{INT} - 431.2\mu s}{40\tau_{DCLK}}$$

Where τ_{DCLK} is the period of the data clock. For example, if T_{INT} = 1000µs and DCLK = 10MHz, the maximum number of DDC112s is:

$$\frac{1000\mu s - 431.2\mu s}{(40)(100ns)} = 142.2 \rightarrow 142 \text{ DDC112s}$$

RETRIEVAL *AFTER* CONV TOGGLES (CONTINUOUS MODE)

For shorter integration times, more time is available if data retrieval begins after CONV toggles and ends before the new data is ready. Data retrieval must wait t_{29} after CONV toggles before beginning. Figure 25 shows an example of this. The maximum time available for retrieval is $t_{27} - t_{29} - t_{26}$ (421.2µs – 10µs – 2µs for CLK = 10MHz), regardless of T_{INT}. The maximum number of DDC112s that can be daisy-chained together is:

$$\frac{409.2\mu s}{40\tau_{DCLK}}$$

For DCLK = 10MHz, the maximum number of DDC112s is 102.

RETRIEVAL *BEFORE* AND *AFTER* CONV TOGGLES (CONTINUOUS MODE)

For the absolute maximum time for data retrieval, data can be retrieved *before and after* CONV toggles. Nearly all of T_{INT} is available for data retrieval. Figure 26 illustrates how this is done by combining the two previous methods. You must pause the retrieval during CONV toggling to prevent digital noise, as discussed previously, and finish before the next data is ready. The maximum number of DDC112s that can be daisy-chained together is:

$$\frac{T_{INT} - 20\mu s - 2\mu s}{40\tau_{DCLK}}$$

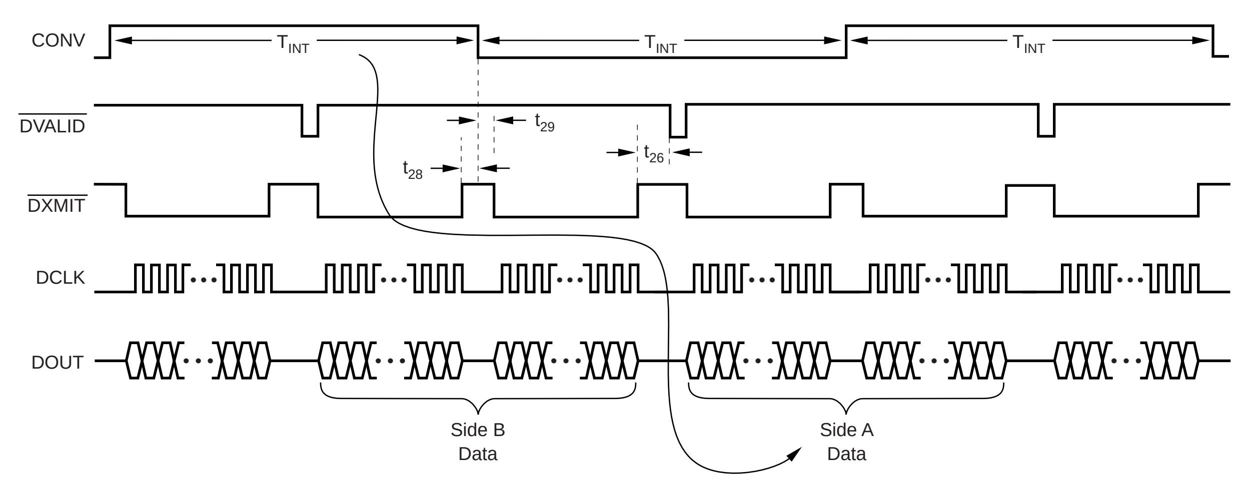
For T_{INT} = 500µs and DCLK = 10MHz, the maximum number of DDC112s is 119.

RETRIEVAL: NONCONTINUOUS MODE

Retrieving in noncontinuous mode is slightly different as compared with the continuous mode. As shown in Figure 27 and described in detail in Application Bulletin SBAA024 (available for download at www.ti.com), $\overline{DVALID}$ goes LOW in time t_{30} after the first integration completes. If T_{INT} is shorter than this time, all of t_{31} is available to retrieve data before the other side's data is ready. For $T_{INT} > t_{30}$, the first integration's data is ready before the second integration completes. Data retrieval must be delayed until the second integration completes leaving less time available for retrieval. The time available is $t_{31} - (T_{INT} - t_{30})$. The second integration's data must be retrieved before the next round of integrations begin. This time is highly dependent on the pattern used to generate CONV. As with the continuous mode, data retrieval must halt before and after CONV toggles (t_{28} and t_{29}) and be completed before new data is ready (t_{26}).

POWER-UP SEQUENCING

Prior to power-up, all digital and analog input pins must be LOW. At the time of power-up, these signal inputs can be biased to a voltage other than 0V, however, they should never exceed AV_{DD} or DV_{DD}. The level of CONV at power-up is used to determine which side (A or B) will be integrated first. Before integrations can begin though, CONV must toggle; see Figure 28.



SYMBOL	DESCRIPTION	CLK = 10MHz			CLK = 15MHz			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{26}	Hold Time for $\overline{DXMIT}$ HIGH Before Falling Edge of $\overline{DVALID}$	2			1.33			µs
t_{28}	Data Retrieval Shutdown Before Edge of CONV	10			10			µs
t_{29}	Data Retrieval Start-Up After dge of CONV	10			10			µs

FIGURE 26. Readback *Before and After* CONV Toggles.

Input shielding practices should be taken into consideration when designing the circuit layout for the DDC112. The inputs to the DDC112 are high impedance and extremely sensitive to extraneous noise. Leakage currents between the PCB traces can exceed the input bias current of the DDC112 if shielding is not implemented. Figure 30 illustrates an acceptable approach to this problem. A PC ground plane is placed around the inputs of the DDC112. This shield helps minimize coupled noise into the input pins. Additionally, the pins that are used for the external integration capacitors should be guarded by a ground plane when the external capacitors are used.

The approach above reduces leakage affects by surrounding these sensitive pins with a low impedance analog ground. Leakage currents from other portions of the circuit will flow harmlessly to the low impedance analog ground rather than into the analog input stage of the DDC112.

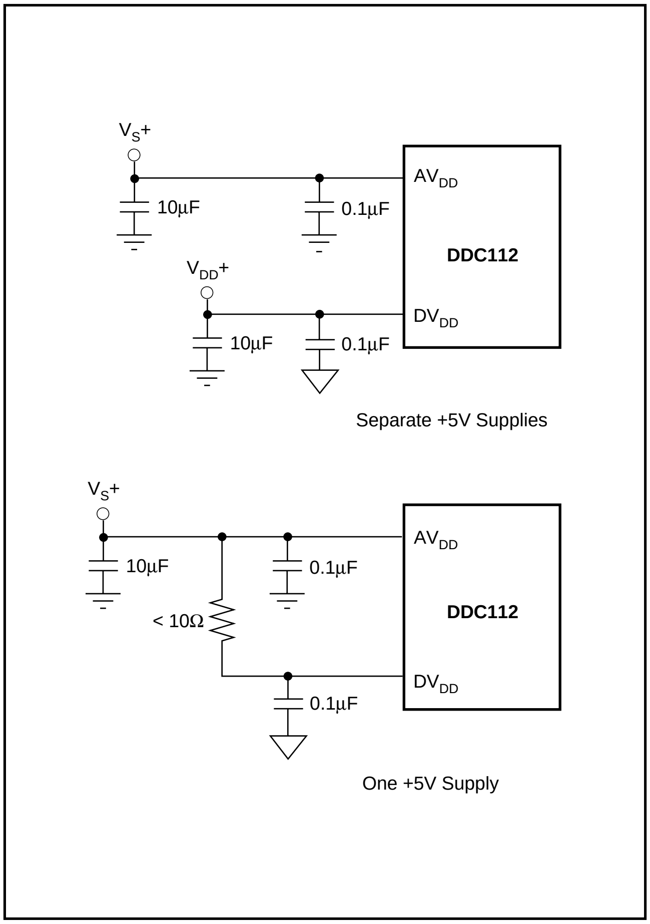


FIGURE 29. Power Supply Connection Options.

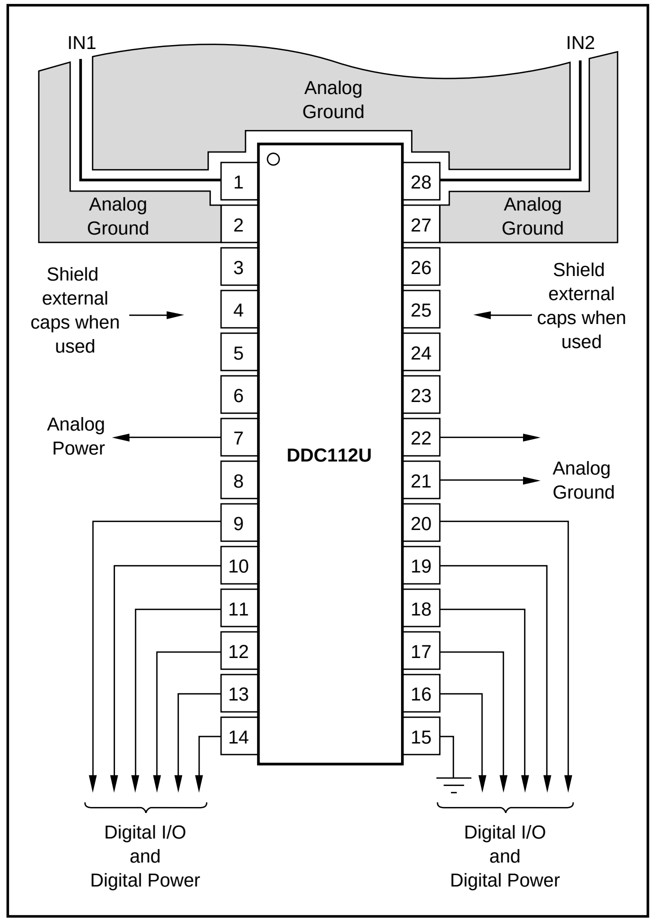


FIGURE 30. Recommended Shield for DDC112U Layout Design.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DDC112U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112U/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112U/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112UG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112UK	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112UK/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112UK/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112UKG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DDC112Y/250	ACTIVE	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DDC112Y/250G4	ACTIVE	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DDC112Y/2K	ACTIVE	TQFP	PJT	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DDC112Y/2KG4	ACTIVE	TQFP	PJT	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DDC112YK/250	ACTIVE	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DDC112YK/250G4	ACTIVE	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DDC112YK/2K	ACTIVE	TQFP	PJT	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DDC112YK/2KG4	ACTIVE	TQFP	PJT	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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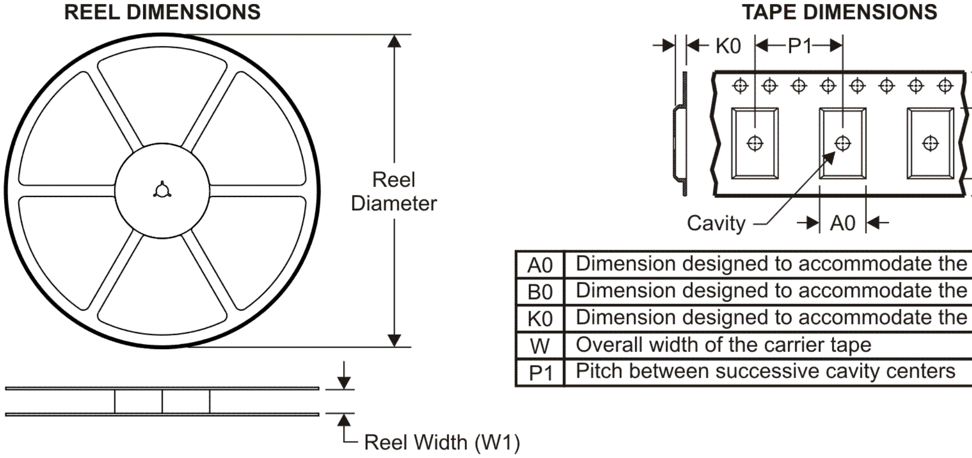
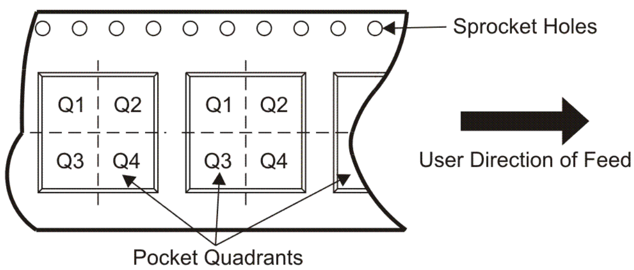
TAPE AND REEL INFORMATION



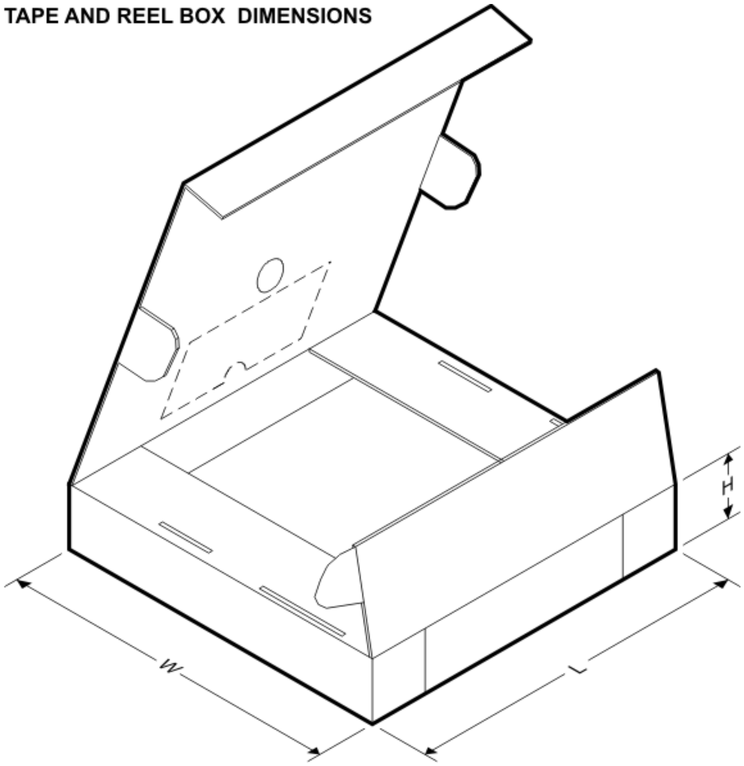
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DDC112U/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
DDC112UK/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
DDC112Y/250	TQFP	PJT	32	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DDC112Y/2K	TQFP	PJT	32	2000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DDC112YK/250	TQFP	PJT	32	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DDC112YK/2K	TQFP	PJT	32	2000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

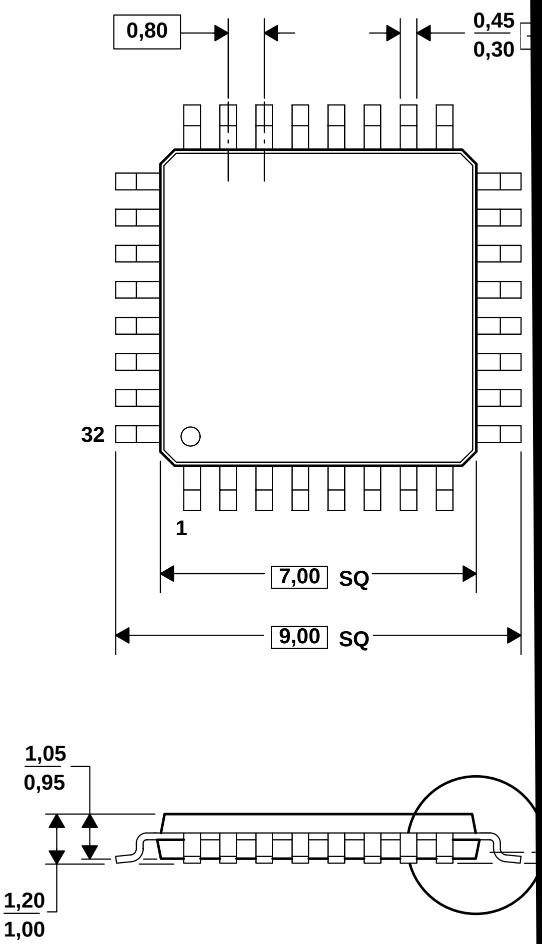


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DDC112U/1K	SOIC	DW	28	1000	346.0	346.0	49.0
DDC112UK/1K	SOIC	DW	28	1000	346.0	346.0	49.0
DDC112Y/250	TQFP	PJT	32	250	346.0	346.0	33.0
DDC112Y/2K	TQFP	PJT	32	2000	346.0	346.0	33.0
DDC112YK/250	TQFP	PJT	32	250	346.0	346.0	33.0
DDC112YK/2K	TQFP	PJT	32	2000	346.0	346.0	33.0

[redacted]

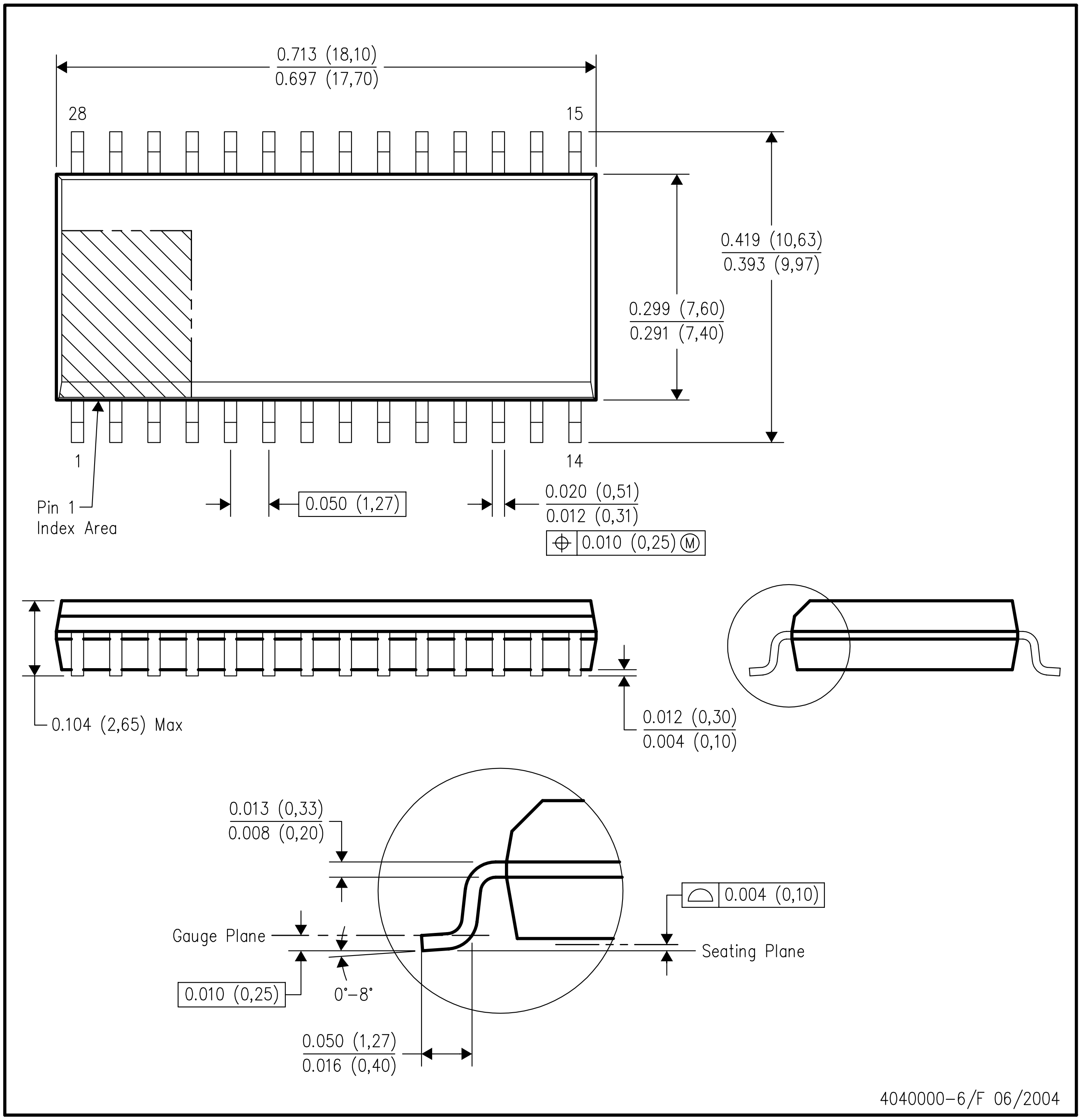
PJT (S-PQFP–N32) [redacted]



[redacted]

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice [redacted]
C. Falls within JEDEC MS-026

DW (R–PDSO–G28) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.