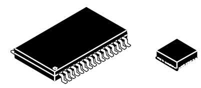


16-CHANNEL LED DRIVER WITH DOT CORRECTION

FEATURES

- **16 Channels**
- **Drive Capability**
  - **– 0 to 80 mA (Constant-Current Sink)**
- **Constant Current Accuracy: ±1% (typical)**
- **Serial Data Interface**
- **Fast Switching Output: T_r / T_f = 10ns (typical)**
- **CMOS Level Input/Output**
- **30 MHz Data Transfer Rate**
- **V_{CC} = 3.0 V to 5.5 V**
- **Operating Temperature = –40°C to 85°C**
- **LED Supply Voltage up to 17 V**
- **32-pin HTSSOP(PowerPAD™) and QFN Packages**
- **Dot Correction**
  - **– 7 bit (128 Steps)**
  - **– individual adjustable for each channel**
- **Controlled In-Rush Current**
- **Error Information**
  - **– LOD: LED Open Detection**
  - **– TEF: Thermal Error Flag**

APPLICATIONS

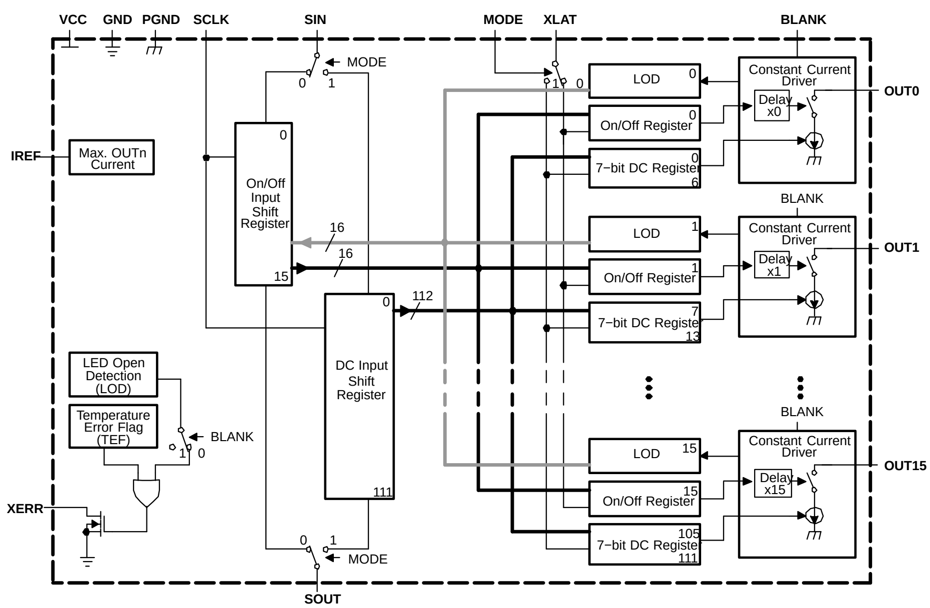
- **Monocolor, Multicolor, Fullcolor LED Display**
- **Monocolor, Multicolor LED Signboard**
- **Display Backlighting**
- **Multicolor LED lighting applications**

DESCRIPTION

The TLC5923 is a 16 channel constant-current sink driver. Each channel has a On/Off state and a 128-step adjustable constant current sink (dot correction). The dot correction adjusts the brightness variations between LED, LED channels and other LED drivers. Both dot correction and On/Off state are accessible via a serial data interface. A single external resistor sets the maximum current of all 16 channels.

The TLC5923 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION (1)

T_A	Package	Part Number (1)
–40°C to 85°C	32-pin, HTSSOP, PowerPAD™	TLC5923DAP
	32-pin, 5 mm x 5 mm QFN	TLC4923RHB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)(2)

			TLC5923	UNIT
V_{CC}	Supply voltage (2)		–0.3 to 6	V
I_O	Output current (dc)	$I_{L(LC)}$	90	mA
V_I	Input voltage range (2)	$V_{(BLANK)}$, $V_{(XLAT)}$, $V_{(SCLK)}$, $V_{(SIN)}$, $V_{(MODE)}$	–0.3 to V_{CC} + 0.3	V
V_O	Output voltage range (2)	$V_{(SOUT)}$, $V_{(XDOWN)}$	–0.3 to V_{CC} + 0.3	V
		$V_{(OUT0)}$– $V_{(OUT15)}$	-0.3 to 18	V
	ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2	kV
		CDM (JEDEC JESD22-C101, Charged Device Model)	500	V
T_{stg}	Storage temperature range		–40 to 150	°C
	Continuous total power dissipation at (or below) T_A = 25°C		3.9	W
	Power dissipation rating at (or above) T_A = 25°C (3)	HTSSOP (DAP)	42.54	mW/°C
		QFN (RHB)	27.86	mW/°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) See SLMA002 for more information about PowerPAD™

RECOMMENDED OPERATING CONDITIONS—DC Characteristics

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_O	Voltage applied to output, (Out0 - Out15)				17	V
V_{IH}	High-level input voltage		0.8 VCC		VCC	V
V_{IL}	Low-level input voltage		GND		0.2 VCC	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT			–1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT, XDOWN			1	mA
I_{OLC}	Constant output current	OUT0 to OUT15			80	mA
T_A	Operating free-air temperature range		-40		85	°C

RECOMMENDED OPERATING CONDITIONS—AC Characteristics

V_{CC} = 3 V to 5.5 V, T_A = -40°C to 85°C (unless otherwise noted)

			MIN	TYP	MAX	UNIT
f_{SCLK}	Clock frequency	SCLK			30	MHz
t_{wh0}/t_{wl0}	CLK pulse duration	SCLK=H/L	16			ns
t_{wh1}	XLAT pulse duration	XLAT=H	20			ns
t_{su0}	Setup time	SIN - SCLK↑	10			ns
t_{su1}		SCLK↑-XLAT↓	10			ns
t_{su2}		MODE↑↓-SCLK↑	10			ns
t_{su3}		MODE↑↓-XLAT↑	10			ns
t_{h0}	Hold time	SCLK↑-SIN	10			ns
t_{h1}		XLAT↓-SCLK↑	10			ns
t_{h2}		SCLK↑-MODE↑↓	10			ns
t_{h3}		XLAT↓-MODE↑↓	10			ns

ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, SOUT	V_{CC}– 0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND, BLANK, XLAT, SCLK, SIN, MODE	–1		1	µA
I_{CC}	Supply current	No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ			6	mA
		No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			15	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			32	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω		36	65(1)	
I_{OLC}	Constant output current	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω	70	80	90	mA
I_{LO0}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15			0.1	µA
I_{LO1}		V_{XERR} = 5.5 V, No TEF and LOD			10	µA
ΔI_{OLC0}	Constant current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±1%	± 4%	
ΔI_{OLC1}	Constant current error	device to device, averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 600 Ω		±4%	±8.5%	
ΔI_{OLC2}	Power supply rejection ratio	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±1	±4	%/V
ΔI_{OLC3}	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±2	±6	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature, rising temperature(2)	150	160	180	°C
$V_{(LOD)}$	LED open detection threshold			0.3	0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{(IREF)}$ = 600 Ω	1.20	1.24	1.28	V

(1) Measured at device start-up temperature. Once the IC is operating (self heating), lower I_{CC} values will be seen. See Figure 15.
(2) Not tested. Specified by design.

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A < 25°C	DERATING FACTOR ABOVE TA = 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
32-pin HTSSOP with PowerPAD(1) soldered	5318 mW	42.54 mW/°C	3403 mW	2765 mW
32-pin HTSSOP with PowerPAD(1) unsoldered	2820 mW	22.56 mW/°C	1805 mW	1466 mW
32-pin QFN	3482 mW	27.86 mW/°C	2228 mW	1811 mW

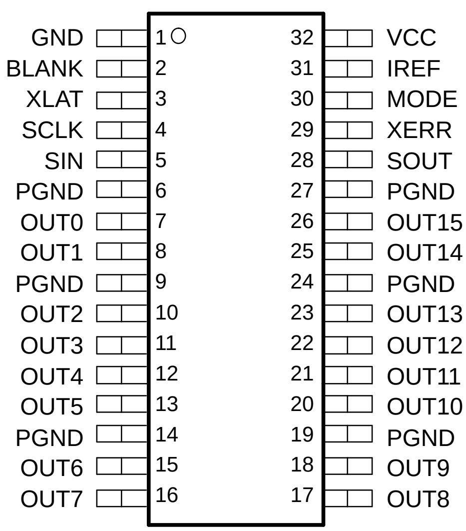
(1) The PowerPAD is soldered to the PCB with a 2 oz. copper trace. See SLMA002 for further information.

SWITCHING CHARACTERISTICS

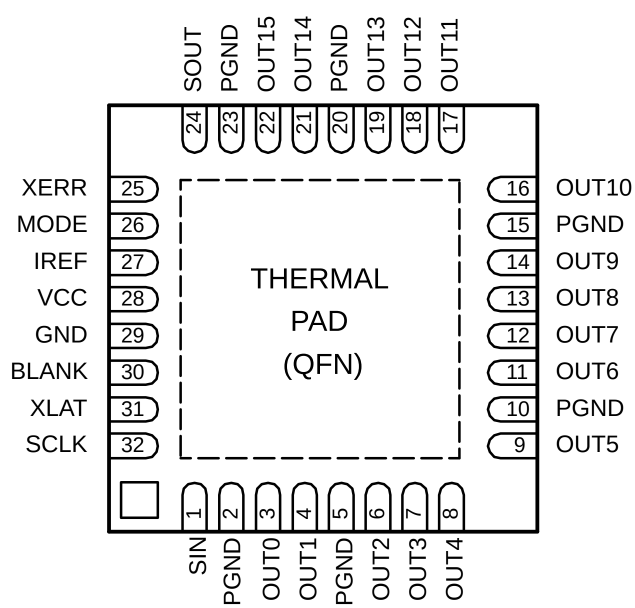
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT(see (1))			16	ns
t_{r1}		OUTx, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_{f0}	Fall time	SOUT (see (1))			16	ns
t_{f1}		OUTx, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_{pd0}	Propagation delay time	SCLK↑ - SOUT↑↓ (see (3))			30	ns
t_{pd1}		MODE↑↓ - SOUT↑↓ (see (3))			30	
t_{pd2}		BLANK↓ - OUT0↑↓ (see (4))			60	
t_{pd3}		XLAT↑ - OUT0↑↓ (see (4))			60	
t_{pd4}		OUTx↑↓-XERR↑↓ (see (5))			1000	
t_{pd5}		XLAT↑-I_{OUT}(dot-correction) (see (6))			1000	
t_d	Output delay time	OUTn↑↓-OUT(n+1)↑↓ (see (4))	14	22	30	ns

(1) See Figure 4. Defined as from 10% to 90%
(2) See Figure 5. Defined as from 10% to 90%
(3) See Figure 4, Figure 11
(4) See Figure 5 and Figure 11
(5) See Figure 5, Figure 6, and Figure 11
(6) See Figure 5

DAP PACKAGE
(TOP VIEW)



RHB PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TSSOP	QFN		
BLANK	2	30	I	Blank (Light OFF). When BLANK=H, All OUTx outputs are forced OFF. When BLANK=L, ON/OFF of OUTx outputs are controlled by input data.
GND	1	29		Ground
IREF	31	27	I/O	Reference current terminal
MODE	30	26	I	Mode select. When MODE=L, SIN, SOUT, SCLK, XLAT are connected to ON/OFF control logic. When MODE=H, SIN, SOUT, SCLK, XLAT are connected to dot-correction logic.
OUT0	7	3	O	Constant current output
OUT1	8	4	O	Constant current output
OUT2	10	6	O	Constant current output
OUT3	11	7	O	Constant current output
OUT4	12	8	O	Constant current output
OUT5	13	9	O	Constant current output
OUT6	15	11	O	Constant current output
OUT7	16	12	O	Constant current output
OUT8	17	13	O	Constant current output
OUT9	18	14	O	Constant current output
OUT10	20	16	O	Constant current output
OUT11	21	17	O	Constant current output
OUT12	22	18	O	Constant current output
OUT13	23	19	O	Constant current output
OUT14	25	21	O	Constant current output
OUT15	26	22	O	Constant current output
PGND	6, 9, 14, 19, 24, 27	2, 5, 10, 15, 20, 23		Power ground
SCLK	4	32	I	Data shift clock. Note that the internal connections are switched by MODE (pin #30). At SCLK↑, the shift-registers selected by MODE shift the data.
SIN	5	1	I	Data input of serial I/F
SOUT	28	24	O	Data output of serial I/F
VCC	32	28		Power supply voltage
XERR	29	25	O	Error output. XERR is open drain terminal. XERR transistions from H to L when LOD or TEF detected.
XLAT	3	31	I	Data latch. Note that the internal connections are switched by MODE (pin #30). At XLAT↑, the latches selected by MODE get new data.

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

(Note: Resistor values are equivalent resistance and not tested).

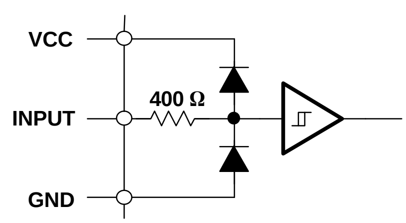


Figure 1. Input Equivalent Circuit (BLANK, XLAT, SCLK, SIN, MODE)

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS (continued)

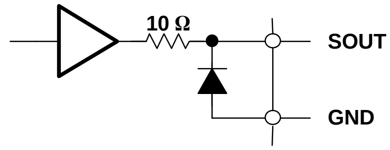


Figure 2. Output Equivalent Circuit

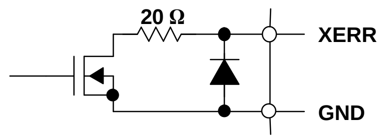


Figure 3. Output Equivalent Circuit (XERR)

PARAMETER MEASUREMENT INFORMATION

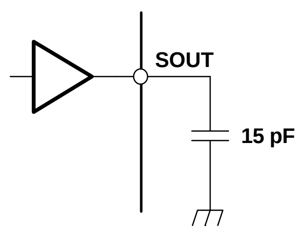


Figure 4. Test Circuit for t_{r0}, t_{f0}, t_{d0}, t_{d1}

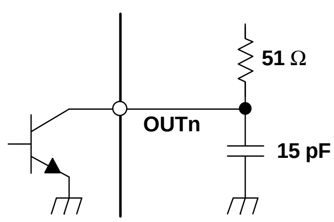


Figure 5. Test Circuit for t_{r1}, t_{f1}, t_{pd2}, t_{pd3}, t_{pd5}, t_{pd6}

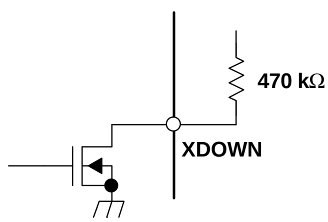


Figure 6. Test Circuit for t_{pd4}

PRINCIPLES OF OPERATION

Setting Maximum Channel Current

The maximum output current per channel is set by a single external resistor, $R_{(IREF)}$, which is placed between IREF and GND. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 40. The maximum output current can be calculated by Equation 1:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 40 \tag{1}$$

where:

V_{IREF} = 1.24V typ.

R_{IREF} = User selected external resistor (R_{IREF} should not be smaller than 600 Ω)

Figure 12 shows the maximum output current, $I_{O(LC)}$, versus $R_{(IREF)}$. In Figure 12, $R_{(IREF)}$ is the value of the resistor between IREF terminal to ground, and $I_{O(LC)}$ is the constant output current of OUT0,.....OUT15.

Setting Dot-Correction

The TLC5923 has the capability to fine adjust the current of each channel, OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LED connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 7-bit word. The channel output can be adjusted in 128 steps from 0% to 100% of the maximum output current I_{MAX}. Equation 2 determines the output current for each OUTn:

$$I_{Outn} = \frac{I_{MAX} \times DC_n}{127} \tag{2}$$

where:

I_{Max} = the maximum programmable current of each output

DCn = the programmed dot-correction value for output n (DCn = 0, 1, 2 ...127)

n = 0, 1, 2 ... 15

Dot correction data are entered for all channels at the same time. The complete dot correction data format consists of 16 x 7-bit words, which forms a 112-bit wide serial data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 7 shows the DC data format.

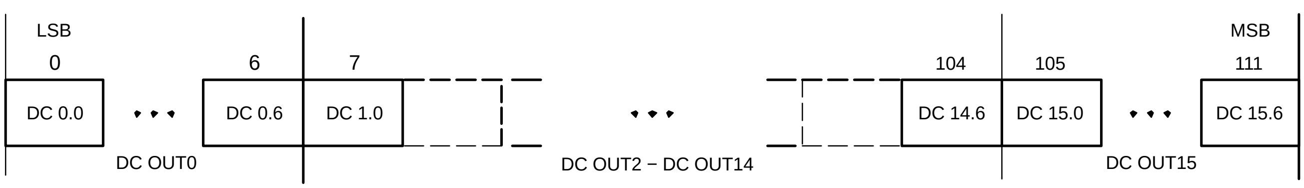


Figure 7. DC Data Format

To input data into dot correction register, MODE must be set to high. The internal input shift register is then set to 112 bit width. After all serial data is clocked in, a rising edge of XLAT latch the data to the dot correction register (Figure 11).

Output Enable

All OUTn channels of TLC5923 can switched off with one signal. When BLANK signal is set to high, all OUTn are disabled, regardless of On/Off status of each OUTn. When BLANK is the to low, all OUTn work under normal conditions.

Table 1. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

Setting Channel On/Off Status

All OUTn channels of TLC5923 can be switched on or off independently. Each of the channels can be programmed with a 1-bit word. On/Off data are entered for all channels at the same time. The complete On/Off data format consists of 16 x 1-bit words, which form a 16-bit wide data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 8 shows the On/Off data format.

LSB 0															MSB 15
On/Off OUT0	On/Off OUT1	On/Off OUT2	On/Off OUT3	On/Off OUT4	On/Off OUT5	On/Off OUT6	On/Off OUT7	On/Off OUT8	On/Off OUT9	On/Off OUT10	On/Off OUT11	On/Off OUT12	On/Off OUT13	On/Off OUT14	On/Off OUT15
On/Off Data															

Figure 8. On/Off Data

To input On/Off data into On/Off register MODE must be set to low. The internal input shift register is then set to 16 bit width. After all serial data is clocked in, a rising edge of XLAT is used to latch data into the On/Off register. Figure 11 shows the On/Off data input timing chart.

With the falling edge of XLAT signal all data in input shift register is replaced with LOD channel data. These data is clocked out to SOUT when new On/Off data is clocked in.

Delay Between Outputs

The TLC5923 has graduated delay circuits between outputs. These delay circuits can be found in the constant current block of the device (see Functional Block Diagram). The fixed delay time is 20 ns (typical), OUT0 has no delay, OUT1 has 20 ns delay, OUT2 has 40 ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before BLANK is pulled high will still turn on and off at the determined delayed time regardless of the state of BLANK. Therefore, every LED will be illuminated for the amount of time BLANK is low.

Serial Interface Data Transfer Rate

The TLC5923 includes a flexible serial interface, which can be connected to microcontroller or digital signal processor. Only 3 pins are in required to input data into the device. The rising edge of SCLK signal shifts the data from SIN pin to internal shift register. After all data is clocked in, a rising edge of XLAT latches the serial data to the internal registers. All data is clocked in with MSB first. Multiple TLC5923 devices can be cascaded by connecting SOUT pin of one device with SIN pin of following device. The SOUT pin can also be connected to controller to receive LOD information from TLC5923.

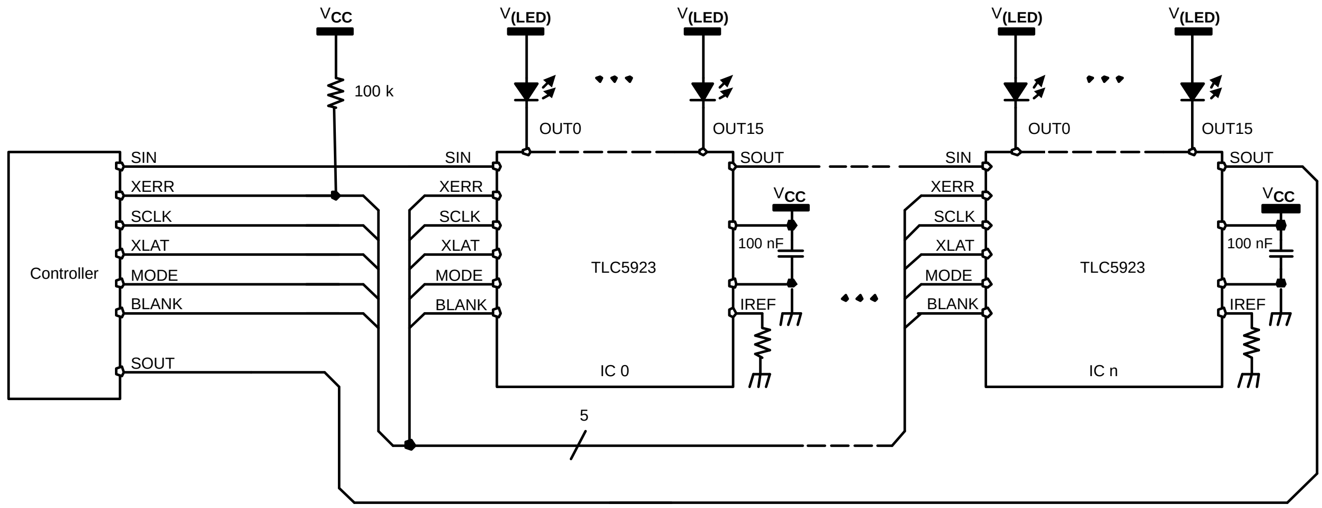


Figure 9. Cascading Devices

Figure 9 shows a example application with *n* cascaded TLC5923 devices connected to a controller. The maximum number of cascaded TLC5923 devices depends on application system and data transfer rate. Equation 3 calculates the minimum data input frequency needed.

$$f\_(SCLK) = 112 \times f\_(update) \times n \quad (3)$$

where:

f_(SCLK): The minimum data input frequency for SCLK and SIN.

f_(update): The update rate of the whole cascaded system.

n: The number of cascaded TLC5923 devices.

Operating Modes

The TLC5923 has different operating modes depending on MODE signal. Table 2 shows the available operating modes.

Table 2. TLC5923 Operating Modes Truth Table

MODE SIGNAL	INPUT SHIFT REGISTER	MODE
LOW	16 bit	On/Off Mode
HIGH	112 bit	Dot Correction Data Input Mode

Error Information Output

The open-drain output XERR is used to report both of the TLC5923 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through a external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Since XERR is an open-drain output, multiple ICs can be OR'ed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error.

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 3. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUNTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	OUTn > $V_{(LOD)}$	L	L	L	H
	OUTn < $V_{(LOD)}$	L	H		L
$T_J > T_{(TEF)}$	OUTn > $V_{(LOD)}$	H	L		L
	OUTn < $V_{(LOD)}$	H	H		L

TEF: Thermal Error Flag

The TLC5923 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature $T_{(TEF)}$ (160°C typical), the TEF circuit trips and pulls XERR to ground.

LOD: LED Open Detection

The TLC5923 provides an LED open-detection circuit (LOD). This circuit reports an error if any one of the 16 LEDs is open or disconnected from the circuit. The LOD circuit trips when the following two conditions are met simultaneously:

1. BLANK is set to LOW
2. When the voltage at OUTn is less than $V_{(LOD)}$ (0.3 V typ.) (Note: the voltage at each OUTn is sampled 1 µs after being turned on).

The LOD circuit also pulls XERR to GND when tripped.

The LOD status of each channel can also be read out from the TLC5923 SOUT pin. When MODE is low and On/Off data is latched with rising edge of XLAT, LOD data is written to the input shift register with the falling edge of XLAT. These LOD data is clocked out to SOUT when new On/Off data is clocked in. These allow to control the LOD status of each OUTn channel. Figure 10 shows the LOD data format.

LSB 0															MSB 15
LOD OUT0	LOD OUT1	LOD OUT2	LOD OUT3	LOD OUT4	LOD OUT5	LOD OUT6	LOD OUT7	LOD OUT8	LOD OUT9	LOD OUT10	LOD OUT11	LOD OUT12	LOD OUT13	LOD OUT14	LOD OUT15
LOD Data															

Figure 10. LOD Data

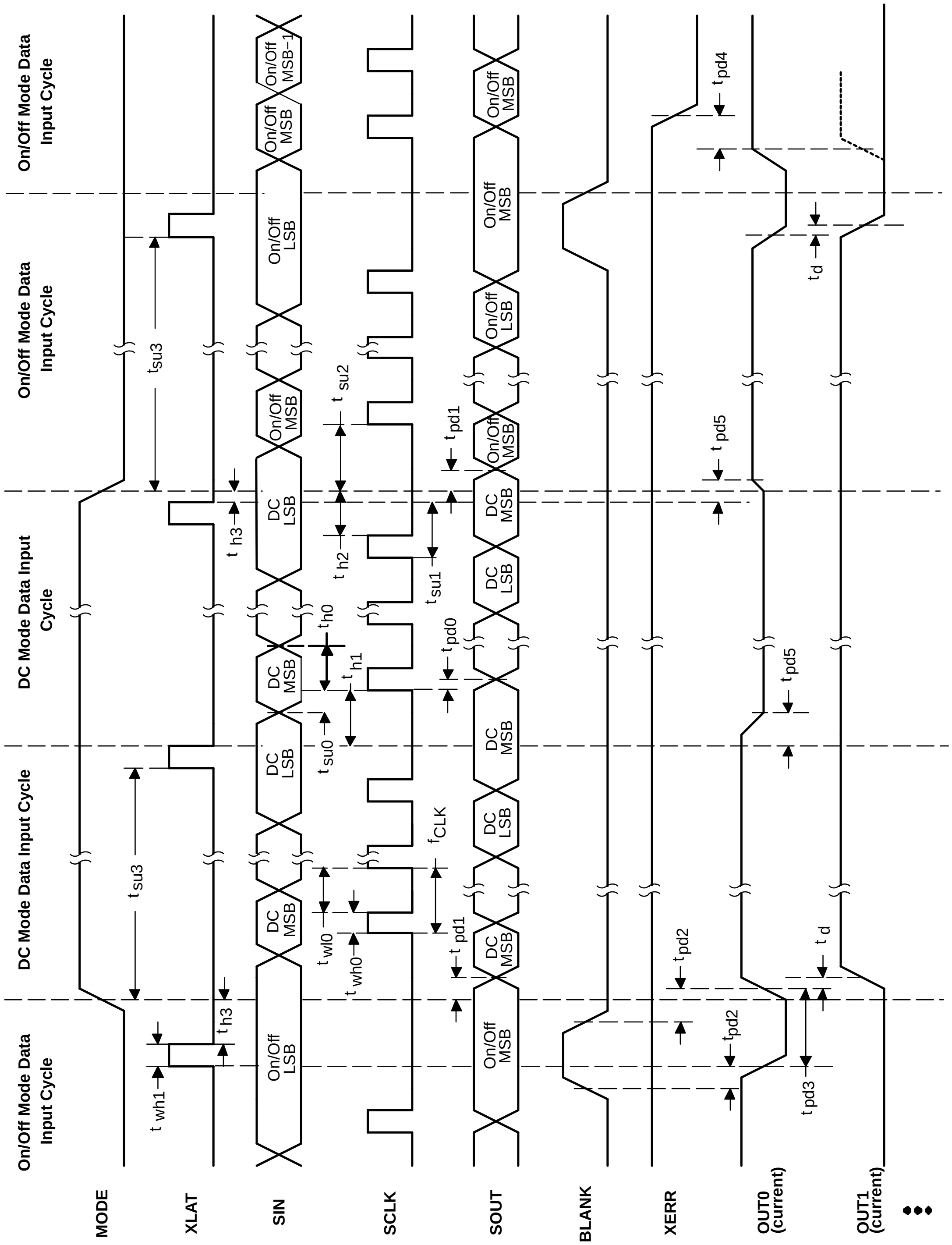


Figure 11. Timing Chart Example for ON/OFF Setting to Dot-Correction

TYPICAL CHARACTERISTICS

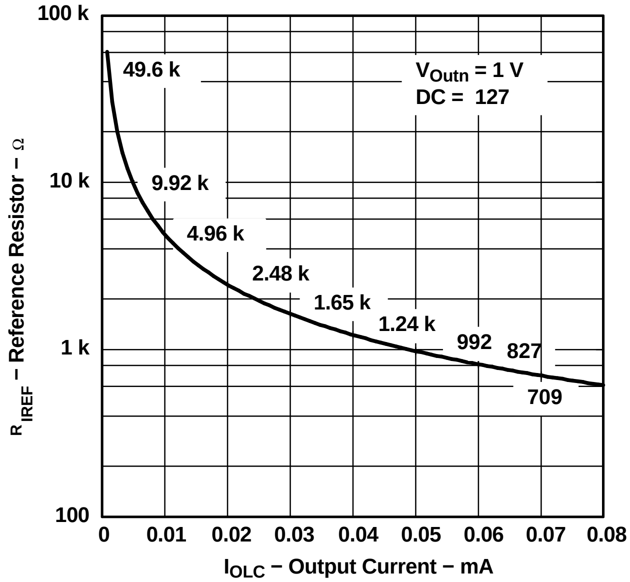


Figure 12. Reference Resistor vs Output Current

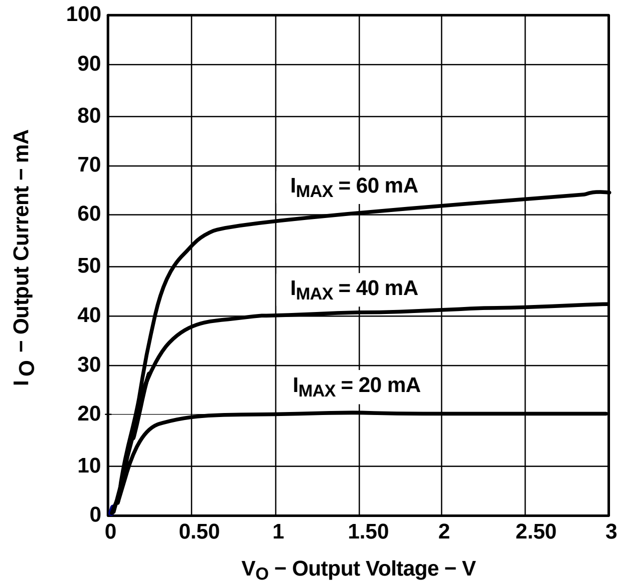


Figure 13. Output Current vs Output Voltage

Power Dissipation vs Temperature

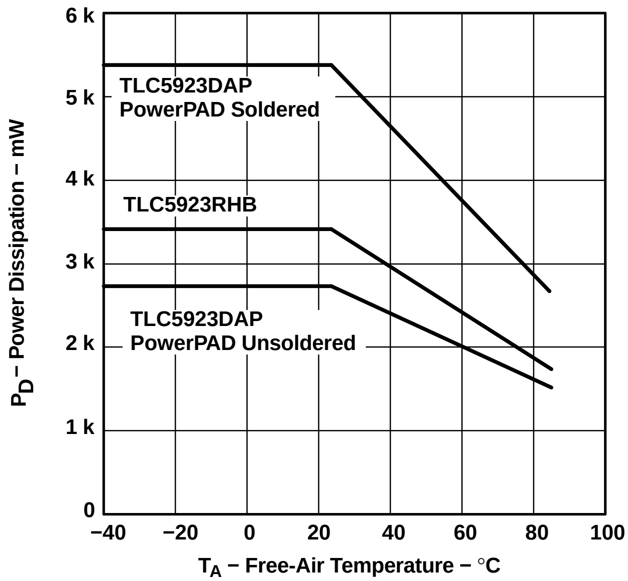
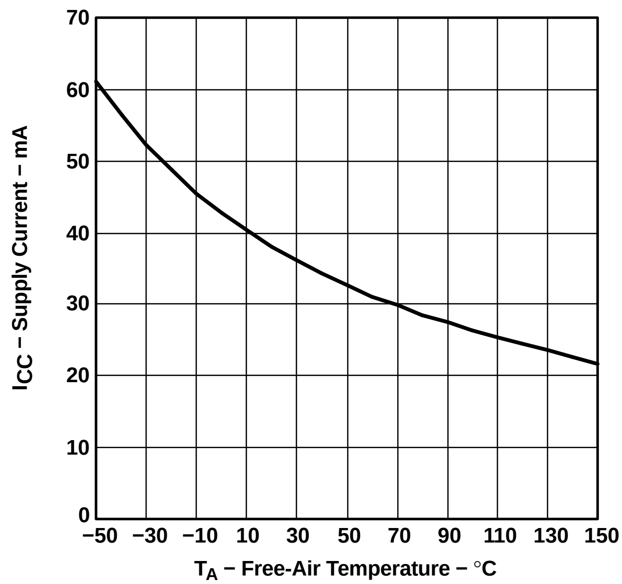


Figure 14.

Supply Current[(A)] vs Free-Air Temperature



A. Data Transfer = 30 MHz / All Outputs, ON/V_O = 1 V / R_{IREF} = 600 Ω / AV_{DD} = 5 V

Figure 15.

Power Rating – Free-Air Temperature

Figure 14 shows total power dissipation. Figure 15 shows supply current versus free-air temperature.

THERMAL PAD MECHANICAL DATA

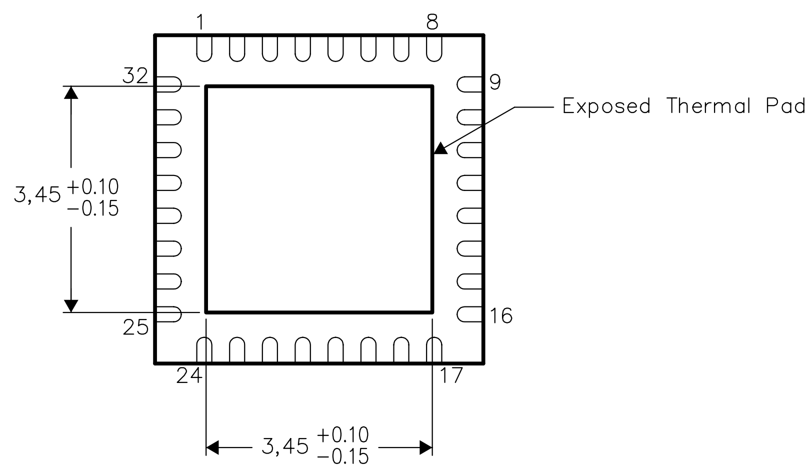
RHB (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC5923DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TLC5923DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TLC5923DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TLC5923DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TLC5923RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5923RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5923RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5923RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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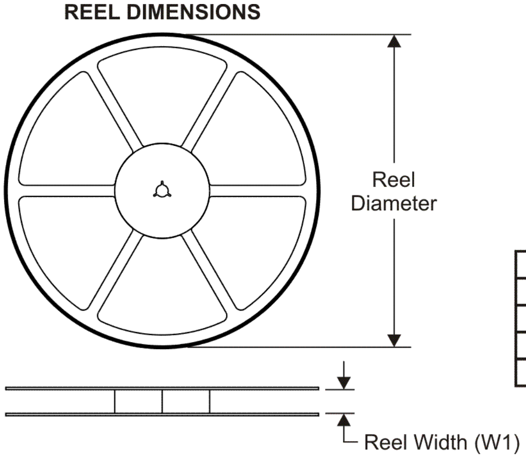
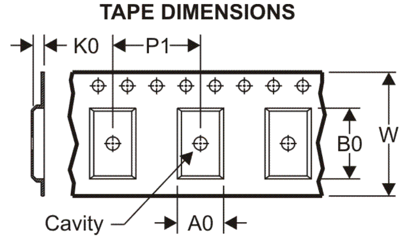
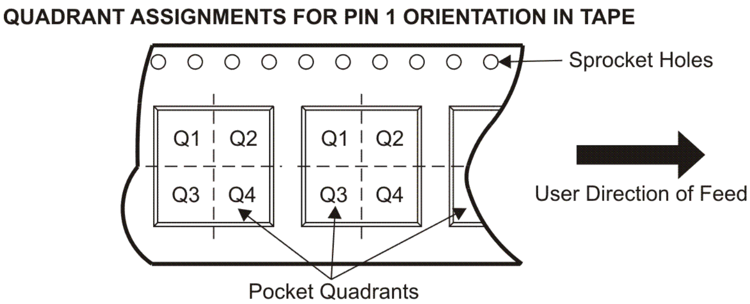
TAPE AND REEL INFORMATION





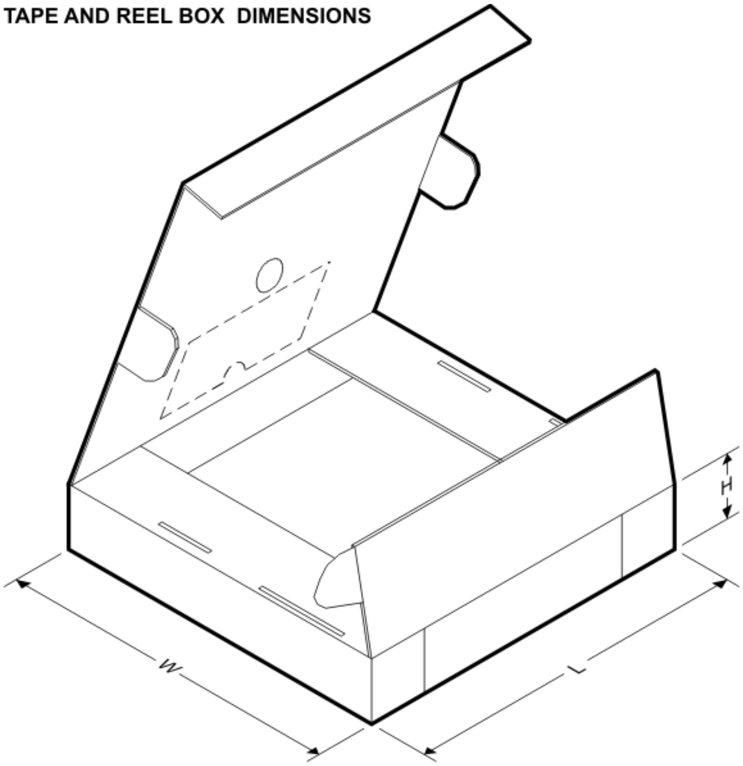
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5923RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC5923RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

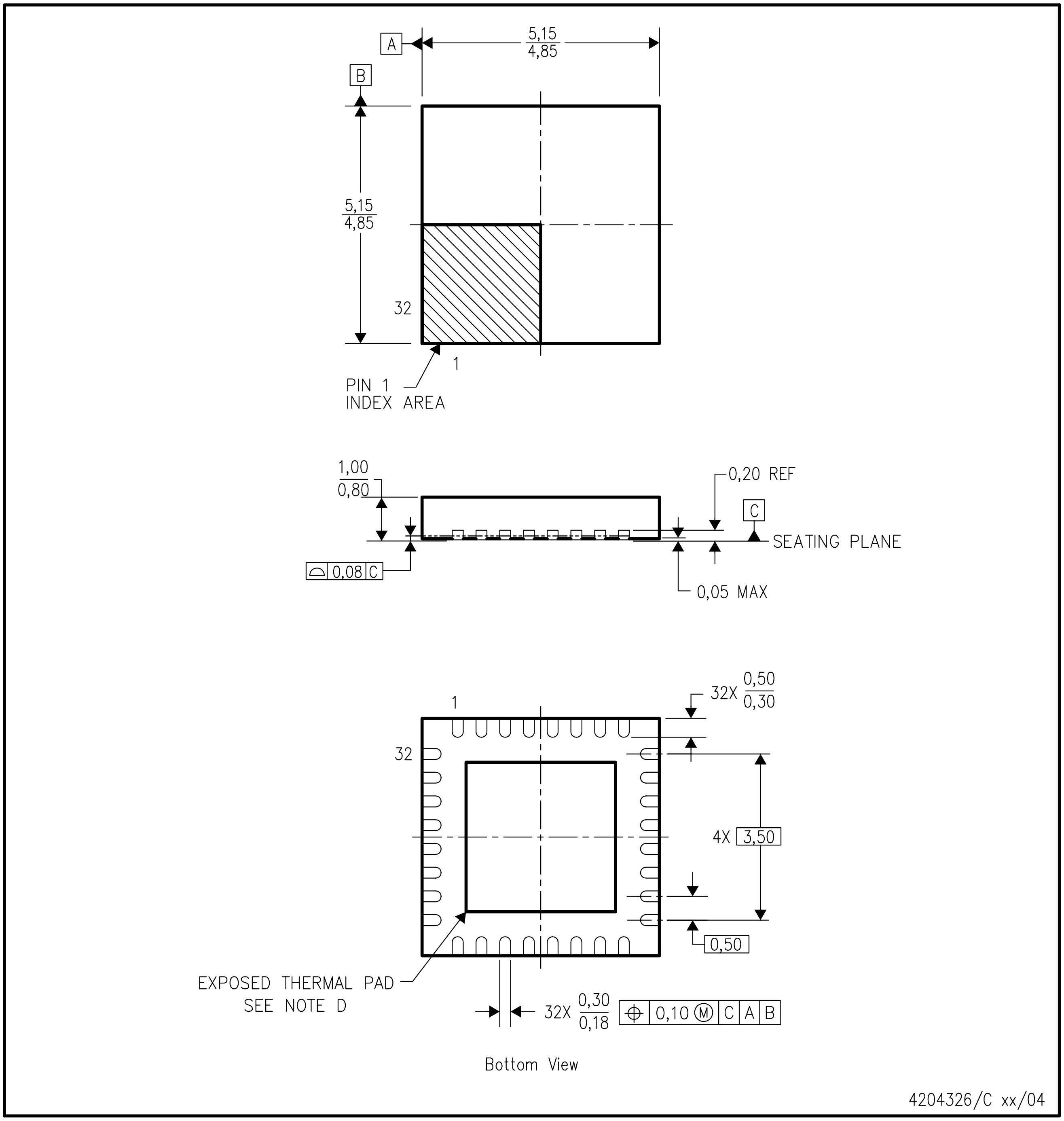
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5923RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TLC5923RHBT	QFN	RHB	32	250	190.5	212.7	31.8

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



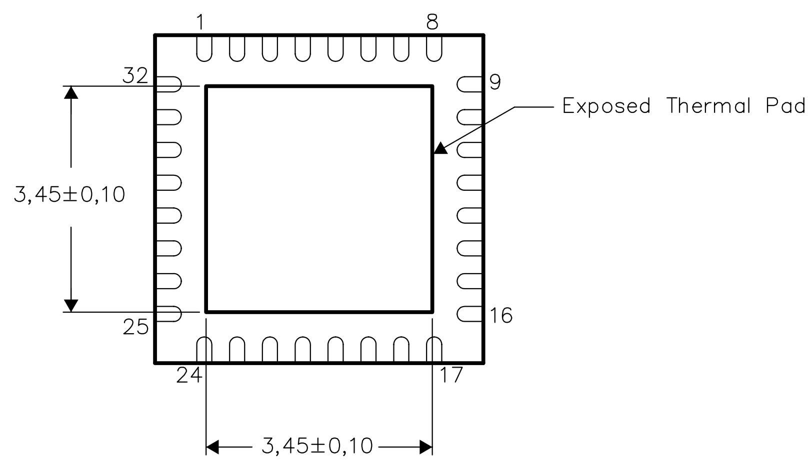
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

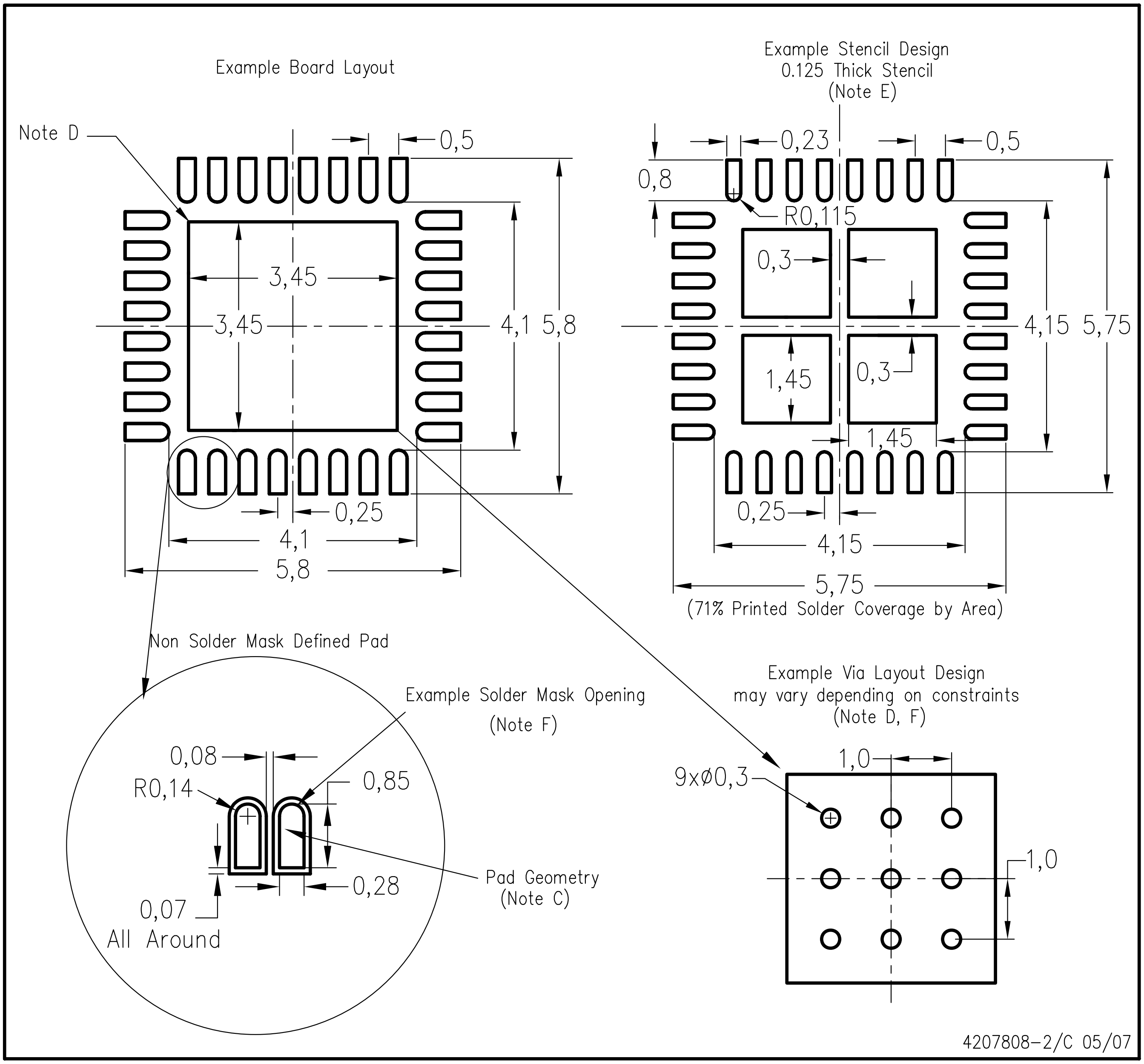


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

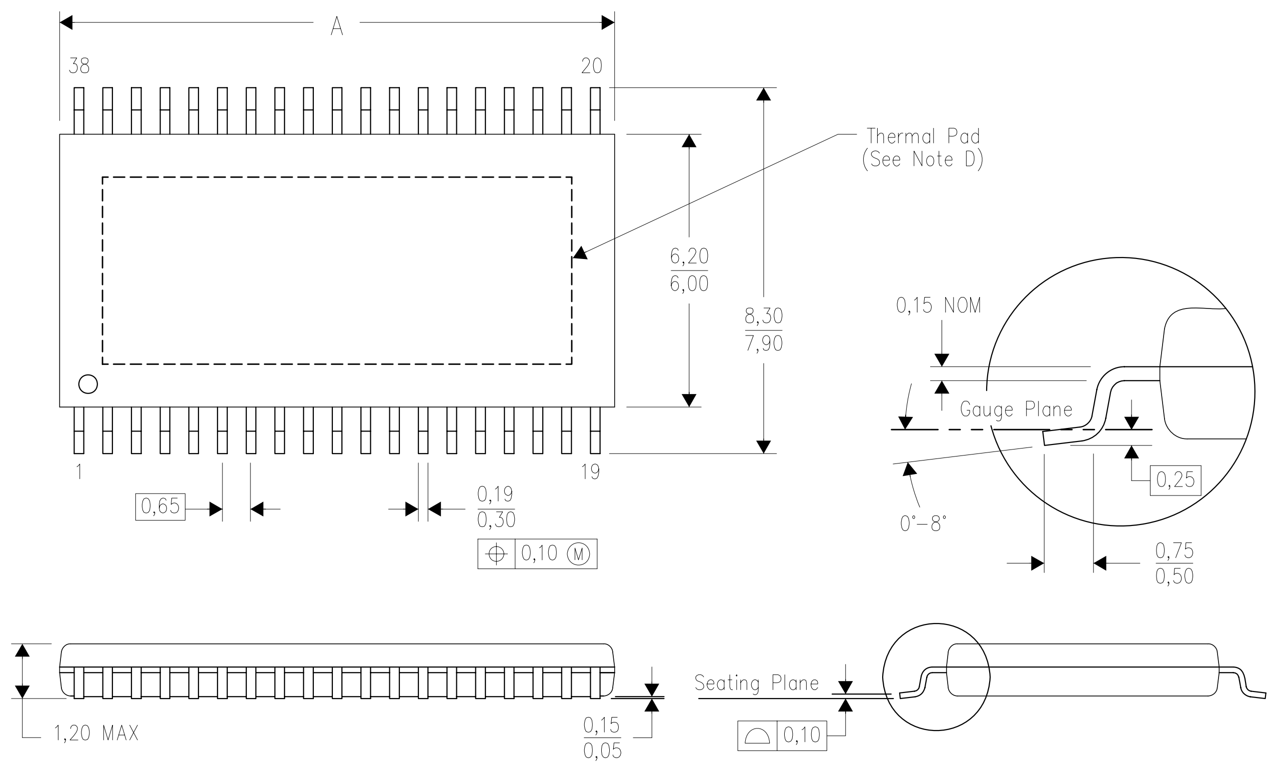
RHB (S–PQFP–N32)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DAP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

38 PINS SHOWN



PINS ** / DIM	28	30	32	38
A MAX	9,80	11,10	11,10	12,60
A MIN	9,60	10,90	10,90	12,40
(E) MO–153 Variation	DBT	DBT–1	DCT	DDT–1

4073257/D 01/2008

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
(E) Falls within JEDEC MO–153, except 30 pin body length.

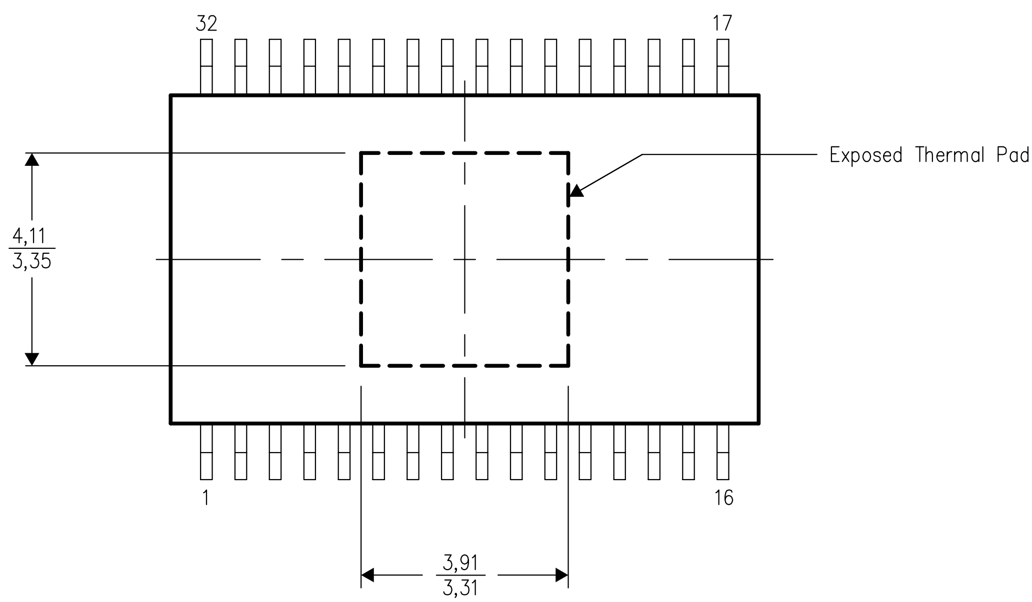
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
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Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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