OLED DISPLAY MODULE

Application Notes

PRODUCT NUMBER	DD-12864YO-1A/5A/7A with EVK board

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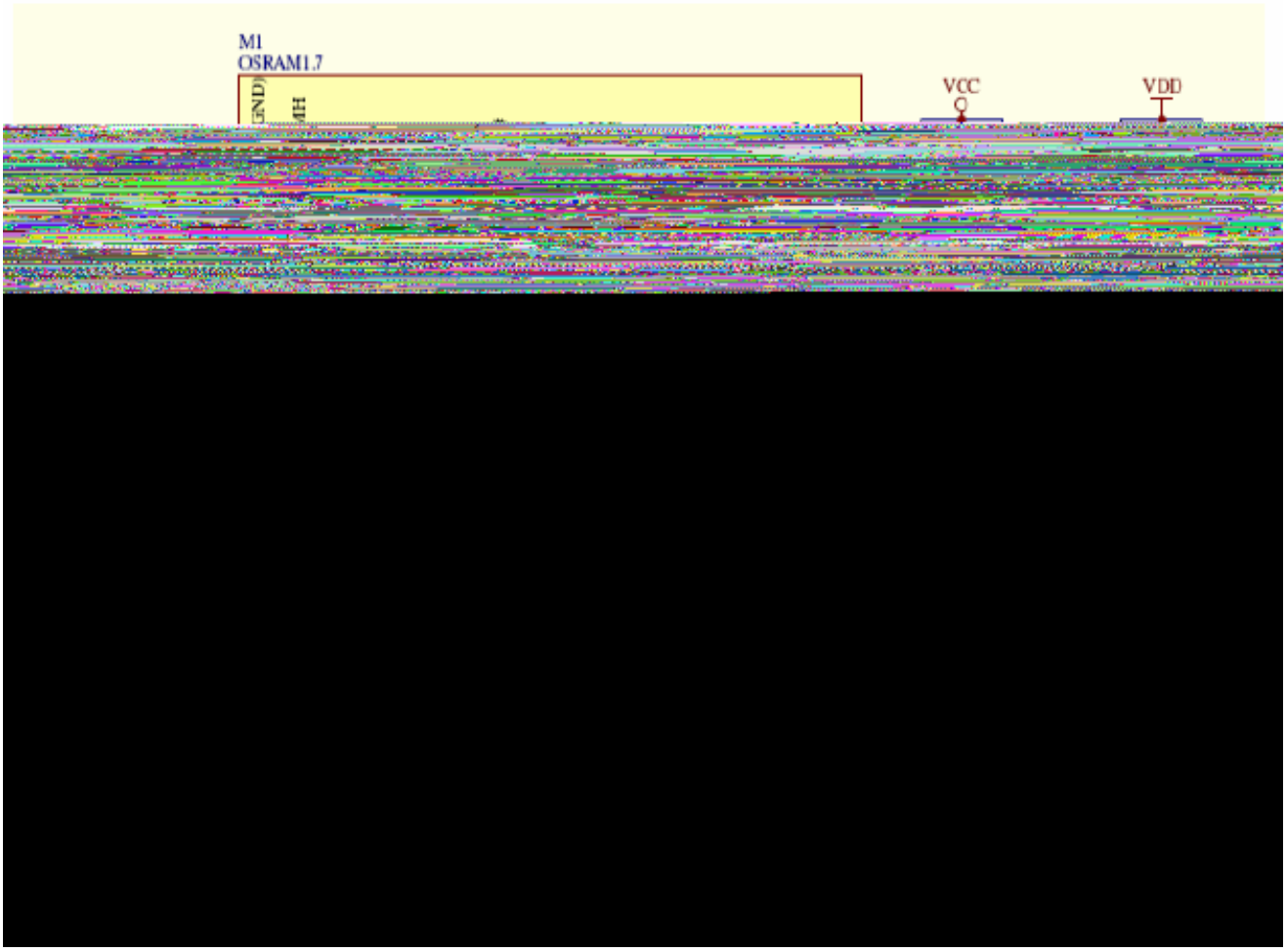
REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	7th May 2008			First Issue	

1 EVK Schematic



2 Symbol Definition

D0-D7：These pins are 8-bit bi-directional data bus to be connected to the MCU's data bus. When serial mode is selected , D1 will be the serial data input SDIN and D0 will be the serial input SCLK.

E/RD#：This pin MCU interface input. When interfacing to a 6800 series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and CS~ is pulled low. When connecting to an 8080 microprocessor this pin receives the Read(RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.

W/R# :This pin in MCU interface input. When interfacing to a 6800 series microprocessor this pin will be used as Read/Write(R/W#) selection input. Pull this pin to "High" for read mode and pull it "Low" for write mode. When 8080 interface mode is selected this pin will be the Write(W/R#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.

D/C# : This pin is Data/Command control pin. When the pin is pulled high, the data at D7~D0 is treated as display data. When the pin is pulled low, the data at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals please refer to the Timing Characteristics diagrams.

RES# : This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS# : This pin is the chip select input. The chip is enabled for MCU communication only CS# is pulled low.

BS1, BS2: This pins are MCU interface selection input, see the following table:

	6800 Parallel Interface	8080 Parallel Interface
BS0	**0**	**0**
BS1	**0**	**1**
BS2	**1**	**1**

VCC: This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC-DC voltage converter.

VDD: This is a voltage supply pin. It must be connected to external source.

VSS: This is a ground pin. It also a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

VSL: This pin is the output pin for the voltage output low level for SEG signals. A capacitor should be connected between this pin and Vss.

NC: These pins should be left open individually.

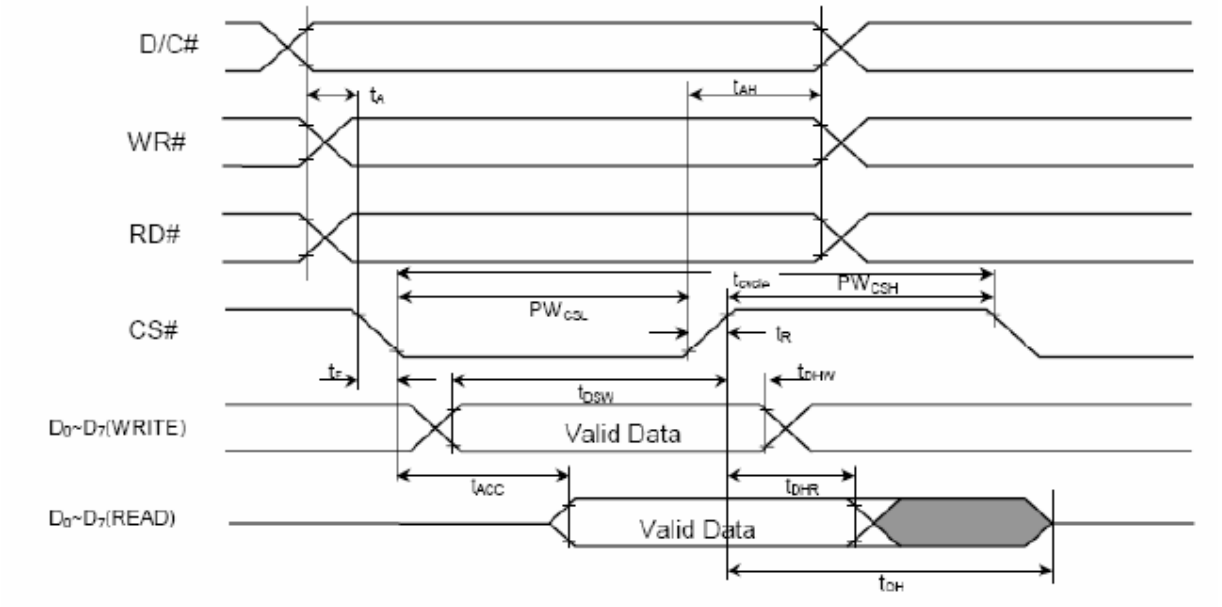
3 Timing characteristics

3.1 80 Series MPU parallel interface

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 1: 80-Series MPU Parallel Interface Timing Characteristics

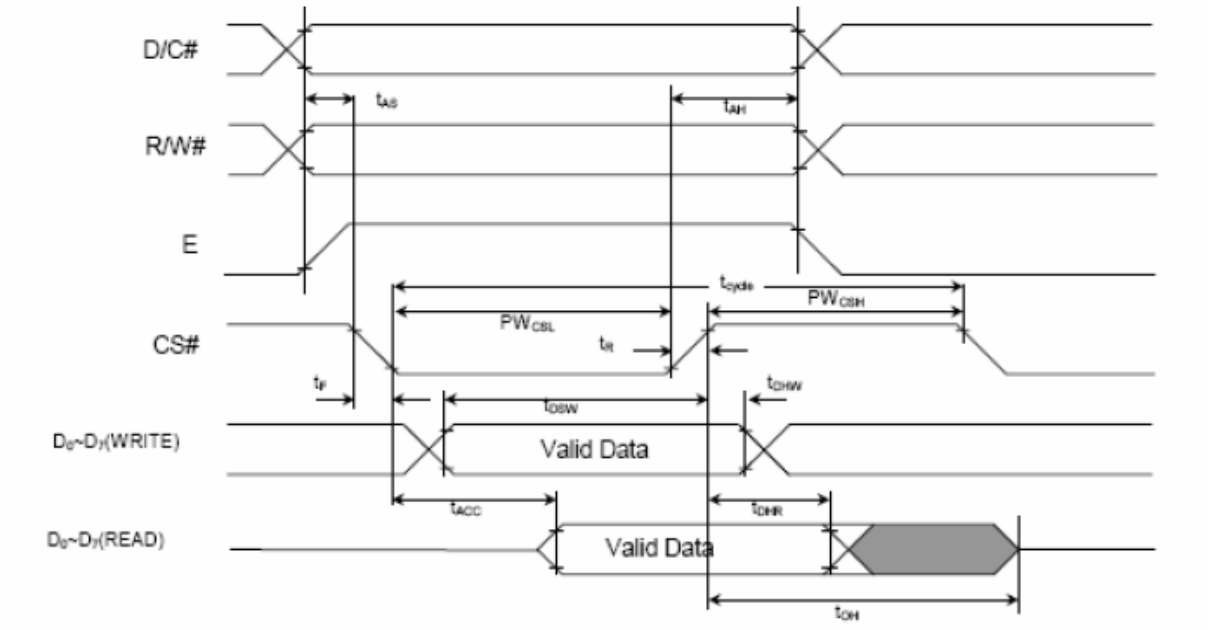


3.2 6800 Series MPU parallel interface

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 2: 6800-Series MPU Parallel Interface Timing Characteristics



4 Connection Between OLED and EVK

Figure 1 EVK PCB and DD-12864YO-1A Module

The DD-12864YO-1A is TAB+FPC) type module, please refer to figure 1 & 2. User can use leading wire to connect EVK with customers systems. The example shown in Fig 3.

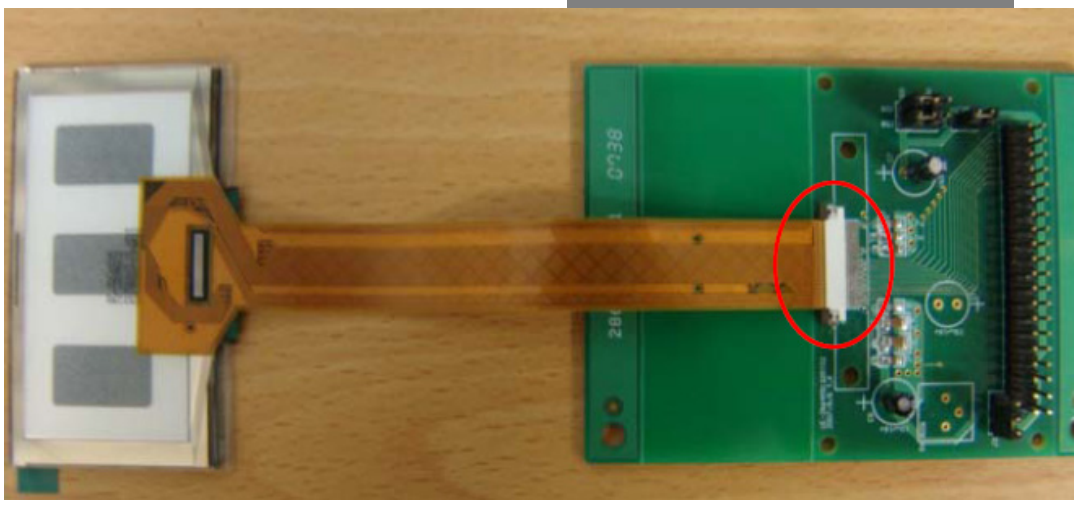


Figure 2 the combination of the module and EVK

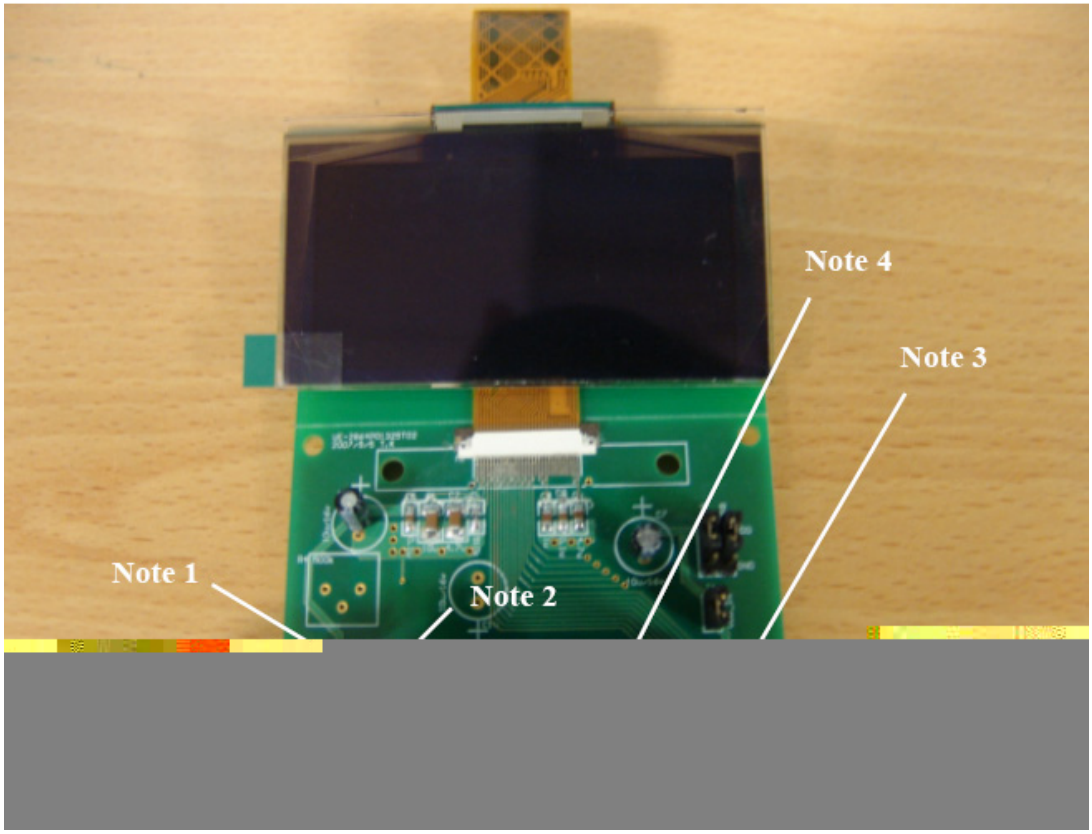


Figure 3 EVK with test platform

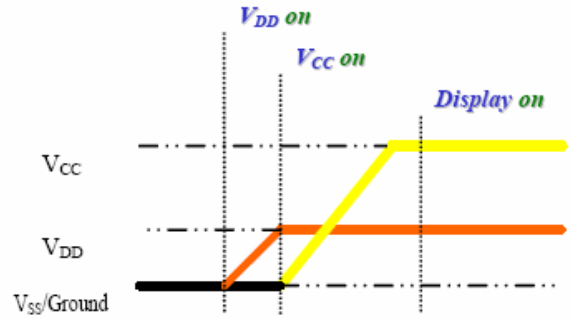
Note 1: It is OLED high voltage supply
Note 2: It is logic voltage supply
Note 3: Those are leading wire connect to control board. Those are data pin (D0~D7)
Note 4: Those are leading wore connect to control board. Those are control pin. (A0,CSB, RDB, WRB, RSTB)

5 Power down and Power Up sequence

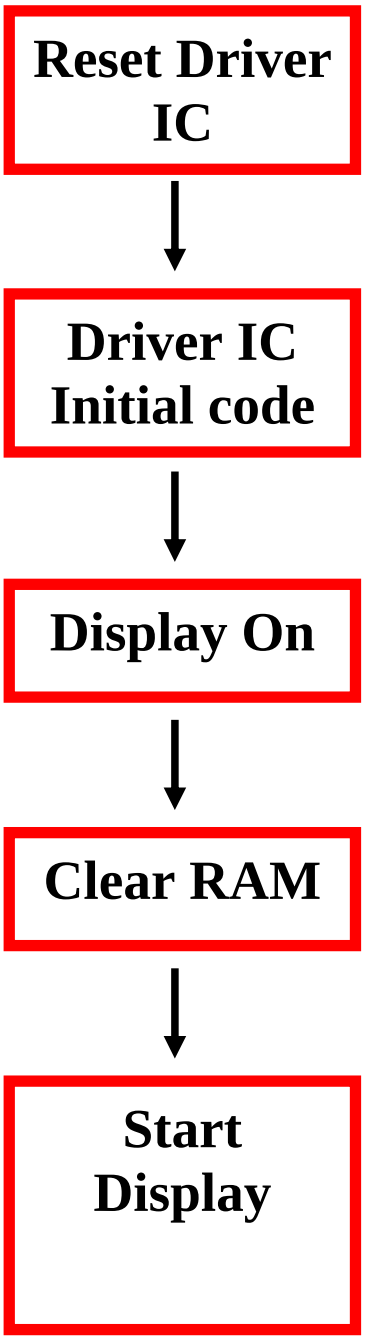
To protect the OLED panel and extend the panel life time the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. So that the panel has enough time to charge up or discharge before/ after operation.

Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DD} is stable)



6 How to use the DD-12864YO-1A/5A/7A



6.1 Recommended Initial code

```
void OLED_Init()
{
unsigned char i;

        RES=0;
        for(i=0;i<200;i++)
        {
                uDelay(200);
        }
        RES=1;

        Set_Display_On_Off(0x00);           // Display Off (0x00/0x01)
        Set_Display_Clock(0x91);            // Set Clock as 135 Frames/Sec
        Set_Multiplex_Ratio(0x3F);          // 1/64 Duty (0x0F~0x5F)
        Set_Display_Offset(0x4C);           // Shift Mapping RAM Counter (0x00~0x5F)
        Set_Start_Line(0x00);               // Set Mapping RAM Display Start Line
(0x00~0x5F)
        Set_Master_Config(0x00);            // Disable Embedded DC/DC Converter
(0x00/0x01)
        Set_Remap_Format(0x50);                     // Set Column Address 0 Mapped to
SEG0
                                            //    Disable Nibble Remap
                                            //    Horizontal Address Increment
                                            //    Scan from COM[N-1] to COM0
                                            //    Enable COM Split Odd Even
        Set_Current_Range(0x02);            // Set Full Current Range
        Set_Gray_Scale_Table();                     // Set Pulse Width for Gray Scale Table
        Set_Contrast_Current(Brightness);   // Set Scale Factor of Segment Output Current
Control
        Set_Frame_Frequency(0x46);          // Set Frame Frequency
        Set_Phase_Length(0x22);                     // Set Phase 1 as 2 Clocks & Phase 2 as 2
Clocks
        Set_Precharge_Voltage(0x10);                // Set Pre-Charge Voltage Level
        Set_Precharge_Compensation(0x20,0x07);  // Set Pre-Charge Compensation
        Set_VCOMH(0x02);                    // Set High Voltage Level of COM Pin
        Set_VSL(0x0C);                              // Set Low Voltage Level of SEG Pin
        Set_Display_Mode(0x00);                     // Normal Display Mode
(0x00/0x01/0x02/0x03)

        Fill_RAM(0x00);                             // Clear Screen

        Set_Display_On_Off(0x01);           // Display On (0x00/0x01)
}
```