4V Drive Nch+Nch MOS FET

US6M1

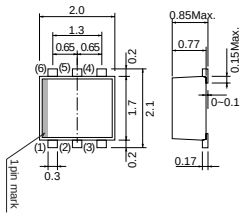
●Structure
Silicon N-channel / P-channel MOS FET

●Features
1) Low on-resistance.
2) Built-in G-S Protection Diode.
3) Small Surface Mount Package (TUMT6).

●Application
Power switching, DC / DC converter.

●External dimensions (Unit : mm)

TUMT6

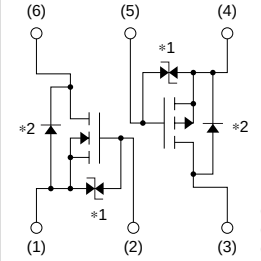


Abbreviated symbol : M01

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6M1		○

●Equivalent circuit



∗1 ESD PROTECTION DIODE
∗2 BODY DIODE

(1) Tr1 (Nch) Source
(2) Tr1 (Nch) Gate
(3) Tr2 (Pch) Drain
(4) Tr2 (Pch) Source
(5) Tr2 (Pch) Gate
(6) Tr1 (Nch) Drain

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : Nchannel	Tr2 : Pchannel	
Drain-source voltage		V_{DSS}	30	−20	V
Gate-source voltage		V_{GSS}	20	−12	V
Drain current	Continuous	I_D	±1.4	±1	A
	Pulsed	I_{DP} ∗1	±5.6	±4	A
Source current (Body diode)	Continuous	I_S	0.6	−0.4	A
	Pulsed	I_{SP} ∗1	5.6	−4	A
Total power dissipation		P_D ∗2	1		W / TOTAL
			0.7		W / ELEMENT
Channel temperature		Tch	150		°C
Storage temperature		Tstg	−55 to +150		°C

∗1 Pw≤10μs, Duty cycle≤1%
∗2 Mounted on a ceramic board.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-a)∗	125	°C / W /TOTAL
		179	°C / W / ELEMENT

∗2 Mounted on a ceramic board.

N-ch

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	10	μA	V_{GS}=20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	30	–	–	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1.0	–	2.5	V	V_{DS}=10V, I_D=1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	170	240	mΩ	I_D=1.4A, V_{GS}=10V
		–	250	350		I_D=1.4A, V_{GS}=4.5V
		–	270	380		I_D=1.4A, V_{GS}=4V
Forward transfer admittance	$\|Y_{fs}\|$ *	1.0	–	–	S	I_D=1.4A, V_{DS}=10V
Input capacitance	C_{iss}	–	70	–	pF	V_{DS}=10V
Output capacitance	C_{oss}	–	15	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	12	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	6	–	ns	I_D=0.7A, V_{DD}≒15V
Rise time	t_r *	–	6	–	ns	V_{GS}=10V
Turn-off delay time	$t_{d\ (off)}$ *	–	13	–	ns	R_L=21Ω
Fall time	t_f *	–	8	–	ns	R_G=10Ω
Total gate charge	Q_g *	–	1.4	2.0	nC	V_{DD}≒15V R_L=11Ω
Gate-source charge	Q_{gs} *	–	0.6	–	nC	V_{GS}=5V R_G=10Ω
Gate-drain charge	Q_{gd} *	–	0.3	–	nC	I_D=1.4A

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward voltage	V_{SD}	–	–	1.2	V	I_S=0.6A, V_{GS}=0V

P-ch

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	–10	μA	V_{GS}=12V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–20	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –20V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–0.7	–	–2.0	V	V_{DS}= –10V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	280	390	mΩ	I_D= –1A, V_{GS}= –4.5V
		–	310	430		I_D= –1A, V_{GS}= –4V
		–	570	800		I_D= –0.5A, V_{GS}= –2.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	0.7	–	–	S	I_D= –0.5A, V_{DS}= –10V
Input capacitance	C_{iss}	–	150	–	pF	V_{DS}= –10V
Output capacitance	C_{oss}	–	20	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	20	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	9	–	ns	I_D= –0.5A, V_{DD}≒ –15V
Rise time	t_r *	–	8	–	ns	V_{GS}= –4.5V
Turn-off delay time	$t_{d\ (off)}$ *	–	25	–	ns	R_L=30Ω
Fall time	t_f *	–	10	–	ns	R_G=10Ω
Total gate charge	Q_g *	–	2.1	–	nC	V_{DD}≒ –15V R_L=15Ω
Gate-source charge	Q_{gs} *	–	0.5	–	nC	V_{GS}= –4.5V R_G=10Ω
Gate-drain charge	Q_{gd} *	–	0.5	–	nC	I_D= –1A

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward voltage	V_{SD}	–	–	–1.2	V	I_S= –0.4A, V_{GS}=0V

N-ch

●Electrical characteristic curves

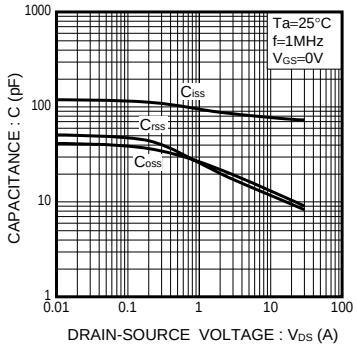


Fig.1 Typical Capacitance vs. Drain-Source Voltage

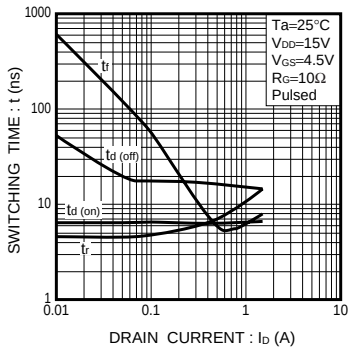


Fig.2 Switching Characteristics

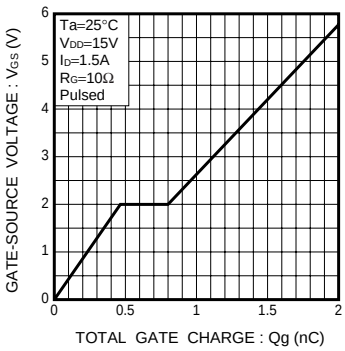


Fig.3 Dynamic Input Characteristics

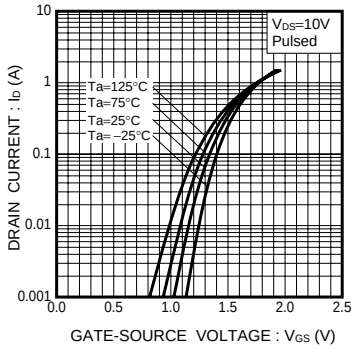


Fig.4 Typical Transfer Characteristics

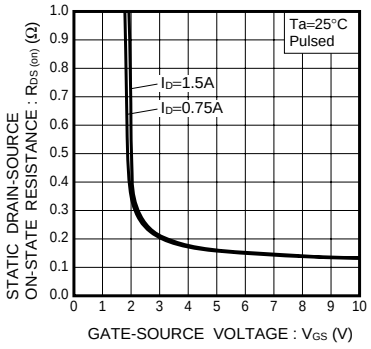


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

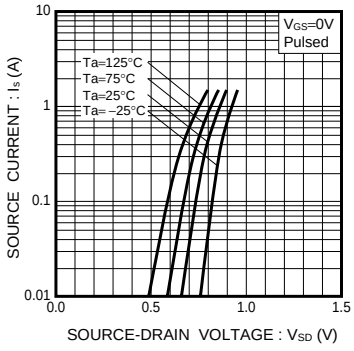


Fig.6 Source Current vs. Source-Drain Voltage

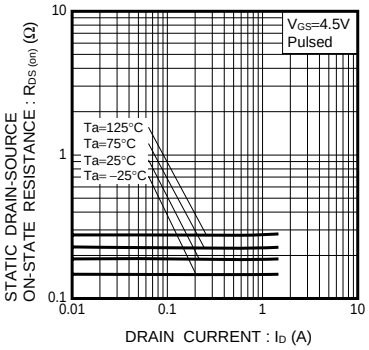


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

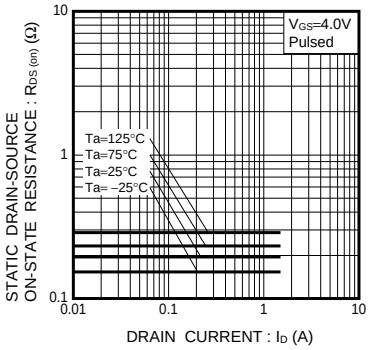


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

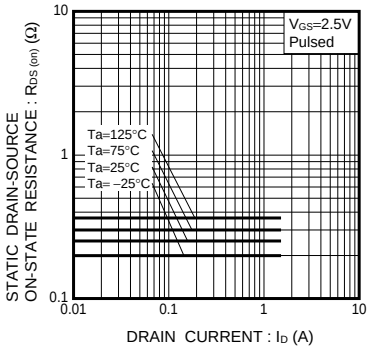


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

P-ch

●Electrical characteristic curves

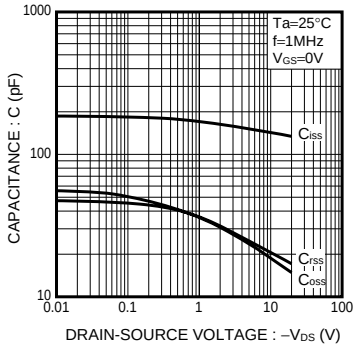


Fig.1 Typical Capacitance vs. Drain-Source Voltage

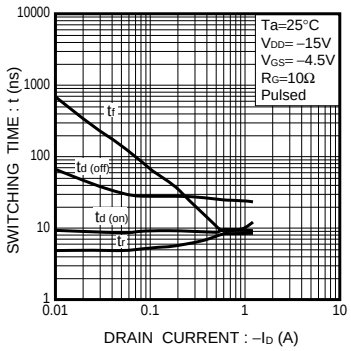


Fig.2 Switching Characteristics

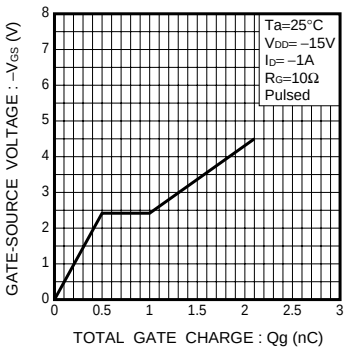


Fig.3 Dynamic Input Characteristics

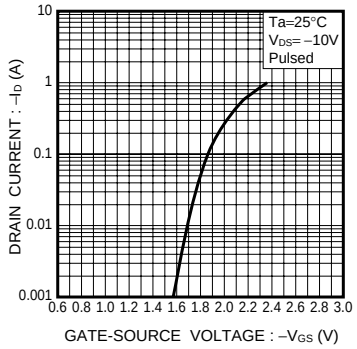


Fig.4 Typical Transfer Characteristics

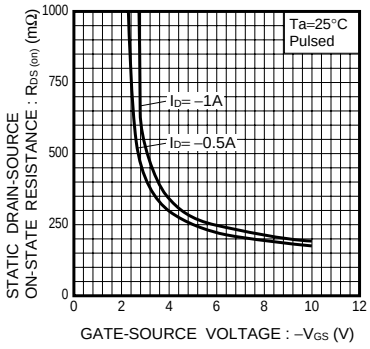


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

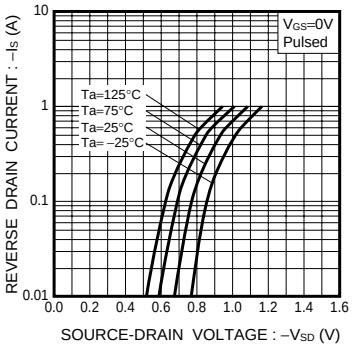


Fig.6 Source Current vs. Source-Drain Voltage

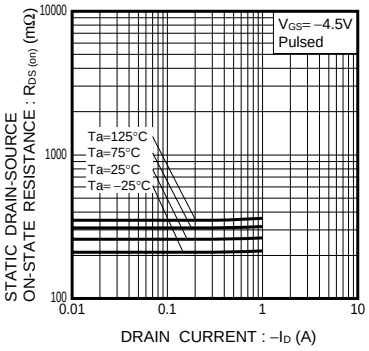


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

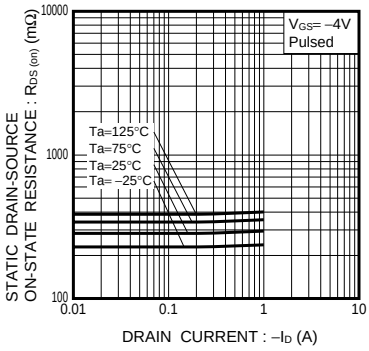


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

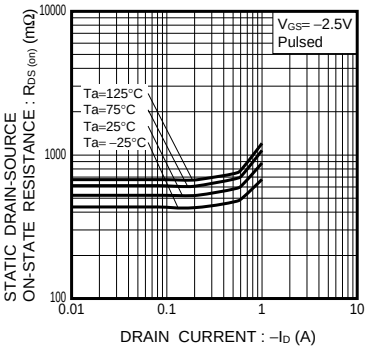


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

N-ch

●Measurement circuit

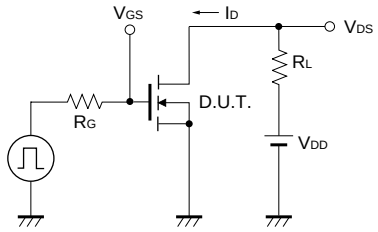


Fig.1-1 Switching Time Measurement Circuit

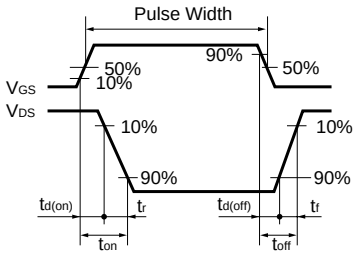


Fig.1-2 Switching Waveforms

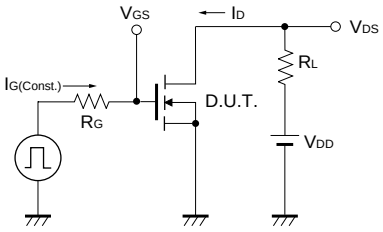


Fig.2-1 Gate Charge Measurement Circuit

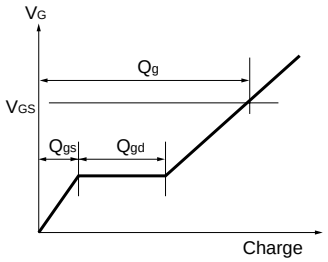


Fig.2-2 Gate Charge Waveform

P-ch

●Measurement circuit

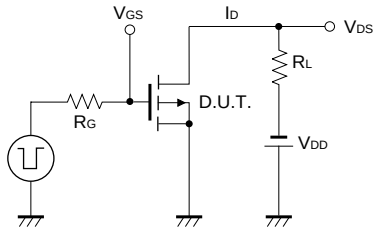


Fig.3-1 Switching Time Measurement Circuit

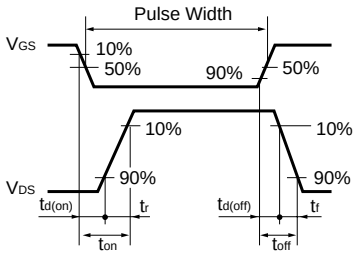


Fig.3-2 Switching Waveforms

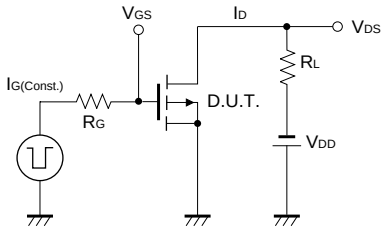


Fig.4-1 Gate Charge Measurement Circuit

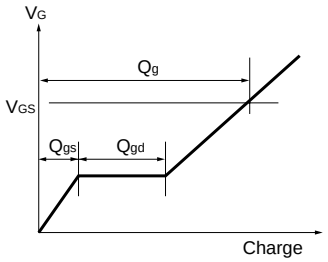


Fig.4-2 Gate Charge Waveform

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