

## 8-Bit Serial-In/Parallel-Out Shift Register

### Features

- **Buffered Inputs**
- **Typical Propagation Delay**
  - 6ns at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ ,  $C_L = 50pF$
- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω Transmission Lines

### Description

The 'AC164 and 'ACT164 are 8-bit serial-in/parallel-out shift registers with asynchronous reset that utilize Advanced CMOS Logic technology. Data is shifted on the positive edge of the clock (CP). A LOW on the Master Reset ( $\overline{MR}$ ) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided; either one can be used as a Data Enable control.

### Ordering Information

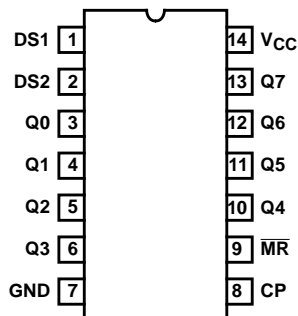
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54AC164F3A	-55 to 125	14 Ld CERDIP
CD74AC164E	-55 to 125	14 Ld PDIP
CD74AC164M	-55 to 125	14 Ld SOIC
CD54ACT164F3A	-55 to 125	14 Ld CERDIP
CD74ACT164E	-55 to 125	14 Ld PDIP
CD74ACT164M	-55 to 125	14 Ld SOIC

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

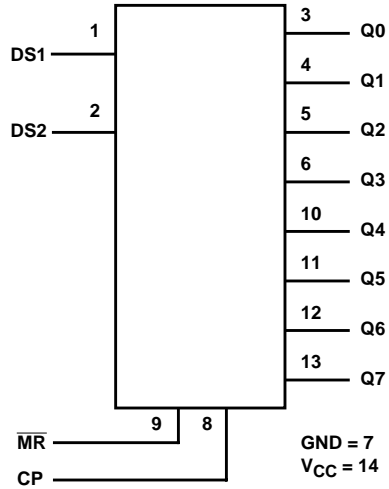
### Pinout

CD54AC164, CD54ACT164  
(CERDIP)  
CD74AC164, CD74ACT164  
(PDIP, SOIC)  
TOP VIEW



**CD54/74AC164, CD54/74ACT164**

**Functional Diagram**



**MODE SELECT - TRUTH TABLE**

OPERATING MODE	INPUTS				OUTPUTS	
	MR	CP	DS1	DS2	Q0	Q1 - Q7
<b>RESET (CLEAR)</b>	L	X	X	X	L	L - L
SHIFT	H	↑	l	l	L	q0 - q6
	H	↑	l	h	L	q0 - q6
	H	↑	h	l	L	q0 - q6
	H	↑	h	h	H	q0 - q6

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

h = HIGH voltage level one setup time prior to the LOW-to\_HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

q = Lowercase letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

↑ = LOW-to-HIGH clock transition.

## CD54/74AC164, CD54/74ACT164

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 6V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 50mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 3) .....	$\pm 100mA$

### Thermal Information

Thermal Resistance (Typical, Note 5)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	175
Maximum Junction Temperature (Plastic Package) .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$ (Note 4)	
AC Types .....	1.5V to 5.5V
ACT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Slew Rate, dt/dv	
AC Types, 1.5V to 3V .....	50ns (Max)
AC Types, 3.6V to 5.5V .....	20ns (Max)
ACT Types, 4.5V to 5.5V .....	10ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTES:

3. For up to 4 outputs per device, add  $\pm 25mA$  for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$		-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
<b>AC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	1.5	1.2	-	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	2.1	-	V	
				5.5	3.85	-	3.85	-	3.85	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	1.5	-	0.3	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	-	0.9	V	
				5.5	-	1.65	-	1.65	-	1.65	V	
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	-4	3	2.58	-	2.48	-	2.4	-	V
			-24	-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	-75	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	-50	5.5	-	-	-	-	3.85	-	V

**CD54/74AC164, CD54/74ACT164**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μA
<b>ACT TYPES</b>											
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

**NOTES:**

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

**ACT Input Load Table**

INPUT	UNIT LOAD
DS1, DS2	0.5
MR	0.74
CP	0.71

NOTE: Unit load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

**CD54/74AC164, CD54/74ACT164**

**Prerequisite For Switching Function**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
<b>AC TYPES</b>							
Max. Clock Frequency	f <sub>MAX</sub>	1.5	7	-	6	-	MHz
		3.3 (Note 9)	62	-	54	-	MHz
		5 (Note 10)	86	-	75	-	MHz
MR Pulse Width	t <sub>W</sub>	1.5	49	-	56	-	ns
		3.3	5.5	-	6.3	-	ns
		5	3.9	-	4.5	-	ns
CP Pulse Width	t <sub>W</sub>	1.5	73	-	84	-	ns
		3.3	8.2	-	9.4	-	ns
		5	5.9	-	6.7	-	ns
Set-up Time	t <sub>SU</sub>	1.5	27	-	31	-	ns
		3.3	3.1	-	3.5	-	ns
		5	2.2	-	2.5	-	ns
Hold Time	t <sub>H</sub>	1.5	27	-	31	-	ns
		3.3	3.1	-	3.5	-	ns
		5	2.2	-	2.5	-	ns
MR to CP Removal Time	t <sub>REM</sub>	1.5	1	-	1	-	ns
		3.3	1	-	1	-	ns
		5	1	-	1	-	ns
<b>ACT TYPES</b>							
Max. Clock Frequency	f <sub>MAX</sub>	5 (Note 10)	80	-	70	-	MHz
MR Pulse Width	t <sub>W</sub>	5	3.9	-	4.5	-	ns
CP Pulse Width	t <sub>W</sub>	5	6.2	-	7.1	-	ns
Set-up Time	t <sub>SU</sub>	5	2.2	-	2.5	-	ns
Hold Time	t <sub>H</sub>	5	2.6	-	3	-	ns
MR to CP Removal Time	t <sub>REM</sub>	5	0	-	0	-	ns

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 3ns, C<sub>L</sub> = 50pF (Worst Case)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>AC TYPES</b>									
Propagation Delay, CP to Qn	t <sub>PLH</sub> , t <sub>PHL</sub>	1.5	-	-	143	-	-	157	ns
		3.3 (Note 9)	4.5	-	15.9	4.4	-	17.5	ns
		5 (Note 10)	3.2	-	11.4	3.1	-	12.5	ns

## CD54/74AC164, CD54/74ACT164

### Switching Specifications Input $t_r$ , $t_f = 3\text{ns}$ , $C_L = 50\text{pF}$ (Worst Case) (Continued)

PARAMETER	SYMBOL	$V_{CC}$ (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay, $\overline{\text{MR}}$ to $Q_n$	$t_{PLH}$ , $t_{PHL}$	1.5	-	-	158	-	-	174	ns
		3.3	5	-	17.7	4.9	-	19.5	ns
		5	3.6	-	12.6	3.5	-	13.9	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	150	-	-	150	-	pF
<b>ACT TYPES</b>									
Propagation Delay, CP to $Q_n$	$t_{PLH}$ , $t_{PHL}$	5 (Note 10)	3.8	-	13.5	3.7	-	14.9	ns
Propagation Delay, $\overline{\text{MR}}$ to $Q_n$	$t_{PLH}$ , $t_{PHL}$	5	4.1	-	14.4	4	-	15.8	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	150	-	-	150	-	pF

**NOTES:**

8. Limits tested at 100%.
9. 3.3V Min at 3.6V, Max at 3V.
10. 5V Min at 5.5V, Max at 4.5V.
11.  $C_{PD}$  is used to determine the dynamic power consumption per device.  
 $P_D = C_{PD}V_{CC}^2 f_i \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ , where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

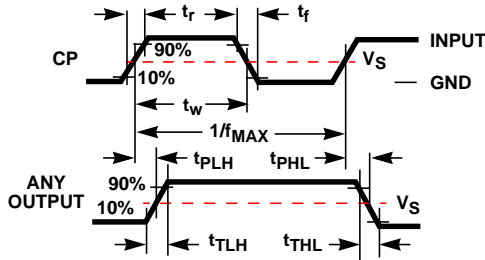


FIGURE 1.

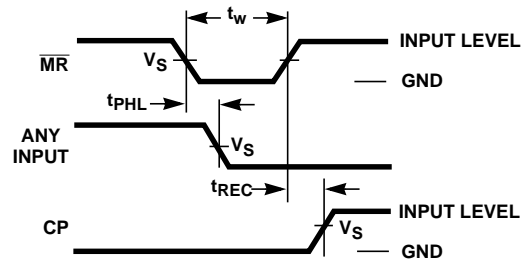


FIGURE 2.

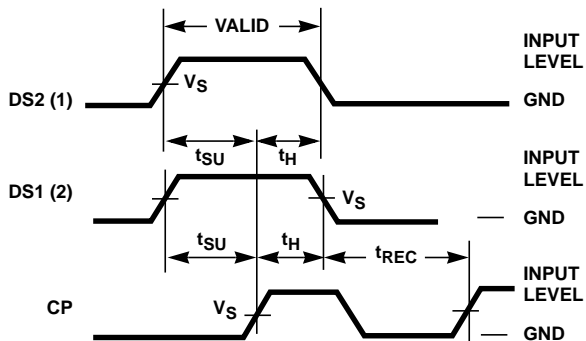


FIGURE 3.

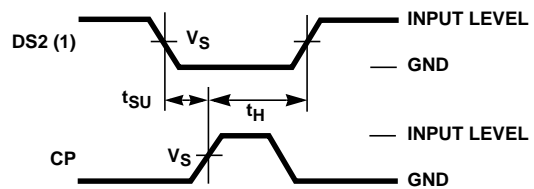
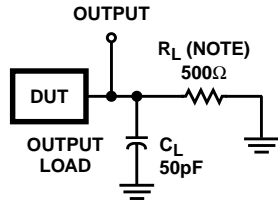


FIGURE 4.

**CD54/74AC164, CD54/74ACT164**



NOTE: For AC Series Only: When  $V_{CC} = 1.5V$ ,  $R_L = 1k\Omega$ .

	AC	ACT
Input Level	$V_{CC}$	3V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

**FIGURE 5. PROPAGATION DELAY TIMES**

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