CS5368

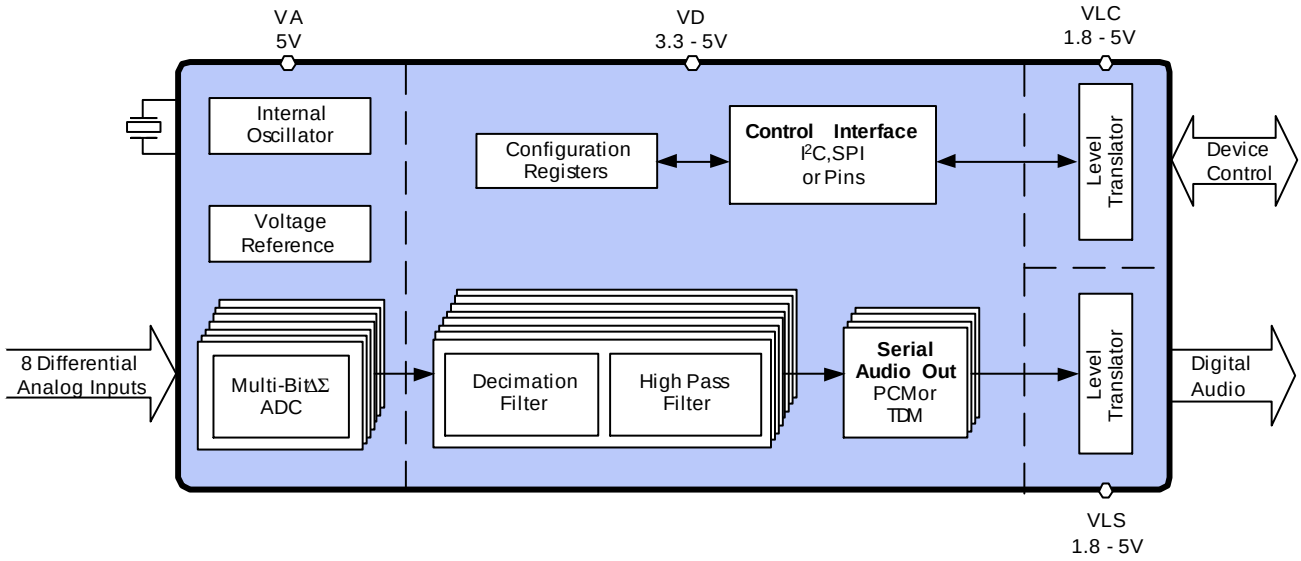
114 dB, 192 kHz, 8-Channel A/D Converter

Overall Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-Bit Conversion
- 114 dB Dynamic Range
- -105 dB THD+N
- Supports Audio Sample Rates up to 216 kHz
- Selectable Audio Interface Formats
  - Left-Justified, I²S, TDM
  - 8-channel TDM Interface Formats
- Low Latency Digital Filter
- Less than 600 mW Power Consumption
- On-Chip Oscillator Driver
- Operation as System Clock Master or Slave
- Differential Analog Architecture
- Separate 1.8 V to 5 V Logic Supplie s for Control and Serial Ports
- High-Pass Filter for DC Offset Calibration
- Overflow Detection
- Pin-Compatible with the 4-Channel CS5364 and 6-Channel CS5366

Additional Control Port Features

- Supports Standard I²C or SPI Control Interface
- Individual Channel HPF Disable
- Overflow Detection for Individual Channels
- Mute Control for Individual Channels
- Independent Power-Down Control per Channel Pair



Advanced Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Description

The CS5368 is a complete 8-channel analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for all 8-channel inputs in serial form at sample rates up to 216 kHz per channel.

The CS5368 uses a 5th-order, multi-bit delta sigma modulator followed by low latency digital filtering and decimation, which removes the need for an external anti-aliasing filter. The ADC uses a differential input architecture which provides excellent noise rejection.

Dedicated level translators for the Serial Port and Control Port allow seamless interfacing between the CS5368 and other devices operating over a wide range of logic levels. In addition, an on-chip oscillator driver provides clocking flexibility and simplifies design.

The CS5368 is the industry's first audio A/D to support a high-speed TDM interface which provides a serial output of 8 channels of audio data with sample rates up to 216 kHz within a single data stream. It further reduces layout complexity and relieves input/output constraints in digital signal processors.

The CS5368 is ideal for high-end and pro-audio systems requiring unrivaled sound quality, transparent conversion, wide dynamic range and negligible distortion, such as A/V receivers, digital mixing consoles, multi-channel recorders, outboard converters, digital effect processors, and automotive audio systems.

ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS5368	114 dB, 192 kHz, 8-channel A/D Converter	48-pin LQFP	YES	Commercial	-10° to +85°C	Tray	CS5368-CQZ
						Tape & Reel	CS5368-CQZR
				Automotive	-40° to +85°C	Tray	CS5368-DQZ
						Tape & Reel	CS5368-DQZR
CDB5368	Evaluation Board for CS5368						CDB5368

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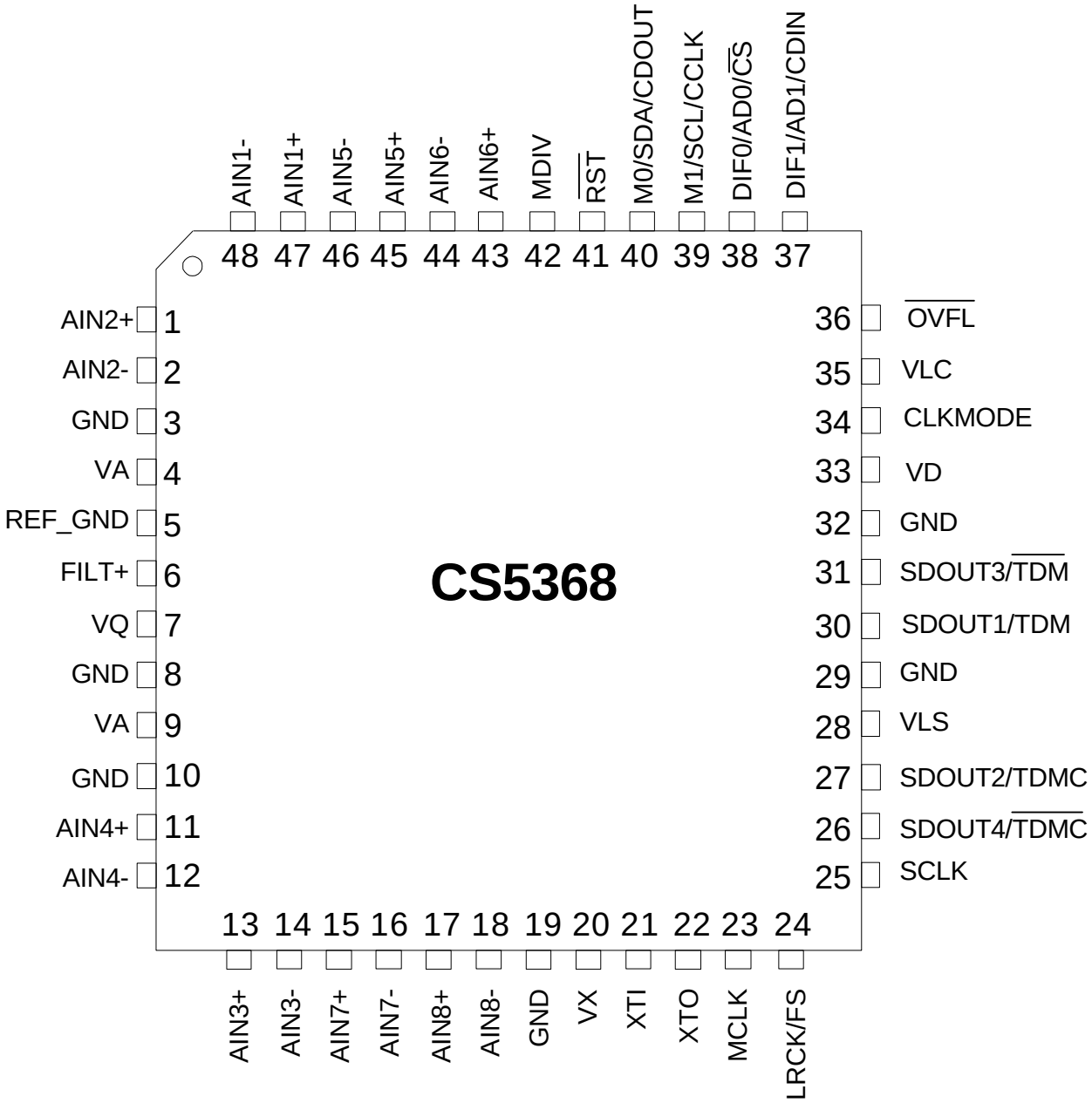


Figure 1. CS5368 Pinout

Pin Name	Pin #	Pin Description
AIN2+ AIN2- AIN4+ AIN4- AIN3+ AIN3- AIN7+ AIN7- AIN8+ AIN8- AIN6+ AIN6- AIN5+ AIN5- AIN1+ AIN1-	1,2, 11,12 13,14 15,16 17,18 43,44 45,46 47,48	**Differential Analog** (*Inputs*) - Audio signals are presented differently to the delta sigma modulators via the AIN+/- pins.
GND	3,8 10,19 29,32	Ground (*Input*) Ground reference. Must be connected to analog ground.
VA	4,9	**Analog Power** (*Input*) - Positive power supply for the analog section
VQ	7	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent reference voltage.
VX	20	**XTAL Power**
VLS	28	**Serial Audio Interface Power** - Positive power for the serial audio interface.
VD	33	**Digital Power** (*Input*)- Positive power supply for the digital section/
VLC	35	**Control Port Interface Power** - Positive power for the control port interface.
REF_GND	5	**Reference Ground** (*Input*) - For the internal sampling circuits.
FILT+	6	**Positive Voltage Reference** (*Output*) - Reference voltage for internal sampling circuits.
XTIXTO	21 22	**Crystal Oscillator Connections** (*Input/Output*) - I/O pins for an external crystal which may be used to generate MCLK.
MCLK	23	**System Master Clock** (*Input/Output*) - When a crystal is used, this pin acts as a buffered MCLK Source (Output). When the oscillator function is not used, this pin acts as an input for the system master clock. In this case, the XTI and XTO pins must be tied low.
LRCK/FS	24	**Serial Audio Channel Clock** (*Input/Output*) In I²S mode Serial Audio Channel Select. When high, the odd channels are selected. In LJ mode Serial Audio Channel Select. When low, the odd channels are selected. In TDM Mode a frame sync signal. When high, it marks the beginning of a new frame of serial audio samples. In Slave Mode, this pin acts as an input pin.
SCLK	25	**Main timing clock for the Serial Audio Interface**(*Input/Output*). During Master Mode, this pin acts as an output, and during Slave Mode it acts as an input pin.
SDOUT4/$\overline{\text{TDMC}}$	26	**Serial Audio Data** (*Output*) Channels 7,8.
SDOUT2/TDMC	27	**Serial Audio Data** (*Output*) Channels 3,4.
SDOUT1/TDM	30	**Serial Audio Data** (*Output*) Channels 1,2.
SDOUT3/$\overline{\text{TDM}}$	31	**Serial Audio Data** (*Output*) Channels 5,6.
OVFL	36	**Overflow** (*Output, open drain*) - Detects an overflow condition on both left and right channels.
RST	41	**Reset** (*Input*) - The device enters a low power mode when low.

Stand-Alone Mode		
CLKMODE	34	**CLKMODE** *(Input)* Setting this pin HIGH places a divide-by-1.5 circuit in the MCLK path to the core device circuitry.
DIF1, DIF0	37, 38	**DIF1, DIF0** (*Input*) - Inputs of the audio interface format.
M1, M0	39,40	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MDIV	42	**MCLK Divider** (*Input*) Setting this pin HIGH places a divide-by-2 circuit in the MCLK path to the core device circuitry.
Control Port Mode		
CLKMODE	34	**CLKMODE** *(Input)* This pin is ignored in Control Port Mode and the same functionality is obtained from the corresponding bit in the Global Control Register. **Note:** Should be connected to GND.
AD1/CDIN	37	**I²C Format, AD1** (*Input*) - Forms the device address input AD[1]. **SPI Format, CDIN** (*Input*) **-** Becomes the input data pin.
AD0/$\overline{CS}$	38	**I²C Format, ADO** (*Input*) - Forms the device address input AD[0]. **SPI Format, CS** (Input) - Acts as the active low chip select input.
SCL/CCLK	39	**I²C Format, SCL** (*Output*) - Acts as the serial clock output from the CS5368. **SPI Format, CCLK** (*Output*) - Acts as the serial clock output from the CS5368.
SDA/CDOUT	40	**I²C Format SDA** (*Input/Output*) - Acts as an input/output data pin. **SPI Format CDOUT** (*Output*) - Acts as an output only data pin.
MDIV	42	**MCLK Divider** (*Input*) This pin is ignored in Control Port Mode and the same functionality is obtained from the corresponding bit in the Global Control Register. **Note:** Should be connected to GND.

2. CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the specified operating conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_A = 25°C.

SPECIFIED OPERATING CONDITIONS

GND = 0 V, all voltages with respect to 0 V.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	4.75	5.0	5.25	V
	Positive Crystal	VX	4.75	5.0	5.25	V
	Positive Digital	VD	3.14	3.3	5.25	V
	Positive Serial Logic	VLS	1.71[1]	3.3	5.25	V
	Positive Control Logic	VLC	1.71	3.3	5.25	V
Ambient Operating Temperature	(-CQZ)	T_{AC}	-10	-	85	°C
	(-DQZ)	T_{AA}	-40	-	85	°C

1. TDM Quad-Speed Mode specified to operate correctly at VLS ≥ 3.14 V.

ABSOLUTE RATINGS

Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes. Transient currents up to ±100 mA on the analog input pins will not cause SCR latch-up.

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA	-0.3		+6.0	V
	Positive Crystal	VX	-0.3		+6.0	V
	Positive Digital	VD	-0.3		+6.0	V
	Positive Serial Logic	VLS	-0.3		+6.0	V
	Positive Control Logic	VLC	-0.3		+6.0	V
Input Current		I_{in}	-		±10	mA
Analog Input Voltage		V_{IN}	-0.3		VA+0.3	V
Digital Input Voltage		V_{IND}	-0.3		VL+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-50		+95	°C
Storage Temperature		T_{stg}	-65		+150	°C

SYSTEM CLOCKING

Parameter	Symbol	Min	Typ	Max	Unit
Input Master Clock Frequency	MCLK	0.512		55.05	MHz
Input Master Clock Duty Cycle	t_{clkhl}	40		60	%

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Package Thermal Resistance	θ_{JA}	-	48	-	°C/W
	θ_{JC}	-	15	-	°C/W

DC POWER CS5368

MCLK = 12.288 MHz; Master Mode. Power Down is defined as $\overline{RST}$ = LOW with all clocks and data lines held static. GND = 0 V.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	70	77	mA
(Normal Operation)	VX = 5 V	I_X	-	4	8	mA
	VD = 5 V	I_D	-	88	97	mA
	VD = 3.3 V	I_D	-	58	64	mA
	VLS, VLC = 5 V	I_L	-	8	9	mA
	VLS, VLC = 3.3 V	I_L	-	5	6	mA
Power Supply Current	VA = 5 V	I_A	-	2	-	mA
(Power-Down)	VLS, VLC,VD = 5 V	I_D	-	2	-	mA
Power Consumption						mW
(Normal Operation)	All Supplies = 5 V	-	-	830	915	mW
	VA = 5 V, VD = VLS = VLC = 3.3 V	-	-	558	616	mW
(Power-Down)		-	-	35	-	mW

LOGIC LEVELS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	%VLS/VLC	V_{IH}	70	-	-	%
Low-Level Input Voltage	%VLS/VLC	V_{IL}		-	30	%
High-Level Output Voltage at 100 µA load	%VLS/VLC	V_{OH}	85	-	-	%
Low-Level Output Voltage at -100 µA load	%VLS/VLC	V_{OL}	-	-	15	%
$\overline{OVFL}$ Current Sink				-4		mA
Input Leakage Current	logic pins only	I_{in}	-	-	±10	µA

PSRR, VQ AND FILT+ CHARACTERISTICS

MCLK = 12.288 MHz; Master Mode. Valid with the recommended capacitor values on FILT+ and VQ as shown in the “Typical Connection Diagram”.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio at 1 kHz)	PSRR	-	65	-	dB
V_Q Nominal Voltage		-	VA/2	-	V
Output Impedance		-	25	-	kΩ
Maximum allowable DC current source/sink		-	10	-	µA
Filt+ Nominal Voltage		-	VA	-	V
Output Impedance		-	4.4	-	kΩ
Maximum allowable DC current source/sink		-	10	-	µA

ANALOG PERFORMANCE (CS5368-CQZ)

Unless otherwise specified, input test signal is a 1 kHz sine wave. Measurement bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode (Fs = 48 kHz)						
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	dB
Total Harmonic Distortion + Noise	-1 dB		-	-105	-99	dB
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB		-	-51	-	dB
Double-Speed Mode (Fs = 96 kHz)						
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	dB
	40 kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	-1 dB		-	-105	-99	dB
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB		-	-51	-	dB
	40 kHz bandwidth -1dB		-	-102	-	dB
Quad-Speed Mode (Fs = 192 kHz)						
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	dB
	40 kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	-1 dB		-	-105	-99	dB
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB		-	-51	-	dB
	40 kHz bandwidth -1dB		-	-102	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-	-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		0	-	-	LSB
	HPF disabled		-	-	100	LSB
Analog Input Characteristics						
Full-scale Differential Input Voltage	(at VA = 5V)		1.07*VA	1.13*VA	1.19*VA	Vpp
Input Impedance (Differential)			-	7.5	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

ANALOG PERFORMANCE (CS5368-DQZ)

Unless otherwise specified, input test signal is a 1 kHz sine wave. Measurement bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111	-	dB
Total Harmonic Distortion + Noise	-1 dB		-	-105	-97	dB
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB		-	-51	-	dB
Double-Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111	-	dB
	40 kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	-1 dB		-	-105	-97	dB
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB		-	-51	-	dB
	40 kHz bandwidth -1 dB		-	-102	-	dB
Quad-Speed Mode Fs = 192 kHz						
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111	-	dB
	40 kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	-1 dB		-	-105	-97	dB
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB		-	-51	-	dB
	40 kHz bandwidth -1 dB		-	-102	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-	-	±7	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		0	-	-	LSB
	HPF disabled		-	-	100	LSB
Analog Input Characteristics						
Full-scale Input Voltage	(at VA = 5.0 V)		1.02*VA	1.13*VA	1.24*VA	Vpp
Input Impedance (Differential)				7.5	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

DIGITAL FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single-Speed Mode (2 kHz to 54 kHz sample rates)					
Passband (-0.1 dB)		0	-	0.47	Fs
Passband Ripple		-	-	±0.035	dB
Stopband		0.58	-	-	Fs
Stopband Attenuation		-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Double-Speed Mode (54 kHz to 108 kHz sample rates)					
Passband (-0.1 dB)		0	-	0.45	Fs
Passband Ripple		-	-	±0.035	dB
Stopband		0.68	-	-	Fs
Stopband Attenuation		-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Quad-Speed Mode (108 kHz to 216 kHz sample rates)					
Passband (-0.1 dB)		0	-	0.24	Fs
Passband Ripple		-	-	±0.035	dB
Stopband		0.78	-	-	Fs
Stopband Attenuation		-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response -3.0 dB -0.13 dB		- -	1 20	- -	Hz Hz
Phase Deviation @ 20 Hz		-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time		-	10^5/Fs	-	s

SERIAL AUDIO INTERFACE - I²S/LJ TIMING

The serial audio port is a three-pin interface consisting of SCLK, LRCK and SDOUT.
Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 30 pF, timing threshold is 50% of VLS.

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rates	Single-Speed Mode	-	2	-	54	kHz
	Double-Speed Mode	-	54	-	108	kHz
	Quad-Speed Mode	-	108	-	216	kHz
SCLK Frequency[1]		-	-	64*Fs	-	Hz
SCLK Period	1/(64*216 kHz)	t_{PERIOD}	72.3	-	-	ns
SCLK Duty Cycle		t_{HIGH}	30	-	70	%
LRCK setup	before SCLK rising	t_{SETUP1}	20	-	-	ns
LRCK hold	after SCLK rising	t_{HOLD1}	20	-	-	ns
SDOUT setup	before SCLK rising	t_{SETUP2}	10	-	-	ns
SDOUT hold	after SCLK rising	t_{HOLD2}	10	-	-	ns

Notes:

1. In Master mode, the SCLK/LRCK ratio is fixed at 64. In Slave Mode, the SCLK/RCLK ratio can be set according to preference. However, chip performance is guaranteed only when using the ratios in Section 4.6.9 Master and Slave Clock Frequencies on page 29.

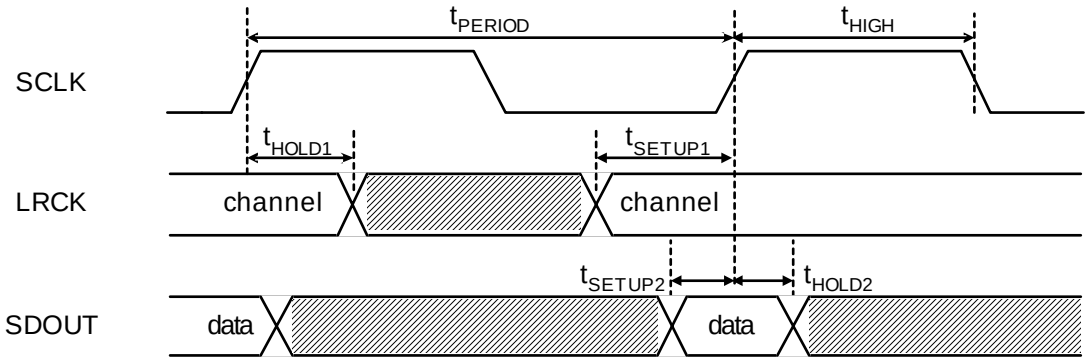


Figure 2. I²S/LJ Timing

SERIAL AUDIO INTERFACE - TDM TIMING

The serial audio port is a 3 pin interface consisting of SCLK, LRCK and SDOUT.
Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 20 pF, timing threshold is 50% of VLS.

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rates	Single-Speed Mode	-	2	-	54	kHz
	Double-Speed Mode	-	54	-	108	kHz
	Quad-Speed Mode[1]	-	108	-	216	kHz
SCLK Frequency[2]			-	256*Fs	-	Hz
SCLK Period	1/(256*54 kHz)	t_{PERIOD}	72.3	-	-	ns
SCLK Duty Cycle		t_{HIGH1}	30	-	70	%
FS setup	before SCLK rising	t_{SETUP1}	20	-	-	ns
FS hold	after SCLK rising	t_{HOLD1}	20	-	-	ns
FS width	in SCLK cycles	t_{HIGH2}	3	-	250	-
SDOUT setup	before SCLK rising	t_{SETUP2}	10	-	-	ns
SDOUT hold	after SCLK rising	t_{HOLD2}	10	-	-	ns

Notes:

1. TDM Quad-Speed Mode only specified to operate correctly at VLS ≥ 3.14 V.
2. In Master mode, the SCLK/LRCK ratio is fixed at 256. In Slave Mode, the SCLK/RCLK ratio can be set according to preference. However, chip performance is guaranteed only when using the ratios in Section 4.6.9 Master and Slave Clock Frequencies on page 29.

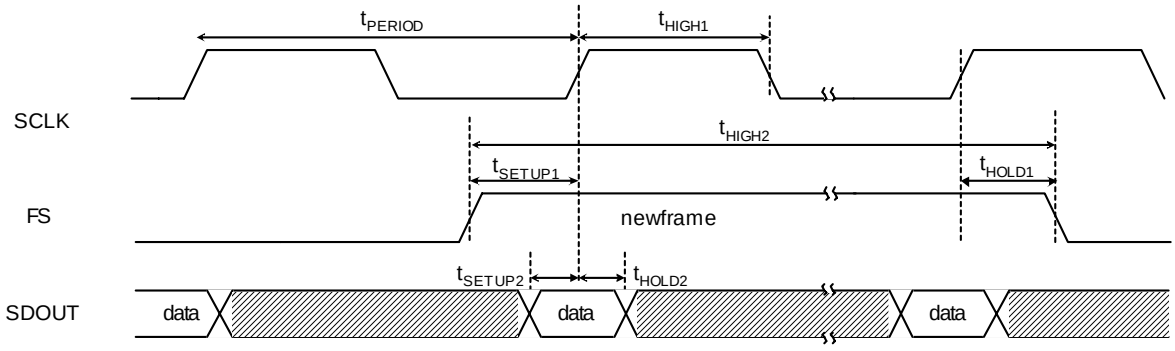


Figure 3. TDM Timing

OVERFLOW TIMEOUT

Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 15 pF, timing threshold is 50% of VLS.

Parameter	Symbol	Min	Typ	Max	Unit
OVFL time-out on overrange condition		-	$(2^{17}-1)/Fs$	-	ms
Fs = 44.1 kHz		-	2972	-	ms
Fs = 192 kHz		-	683	-	ms

Table 1. Overflow Timeout

SWITCHING SPECIFICATIONS - CONTROL PORT - I²C TIMING

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling[1]	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

1. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL

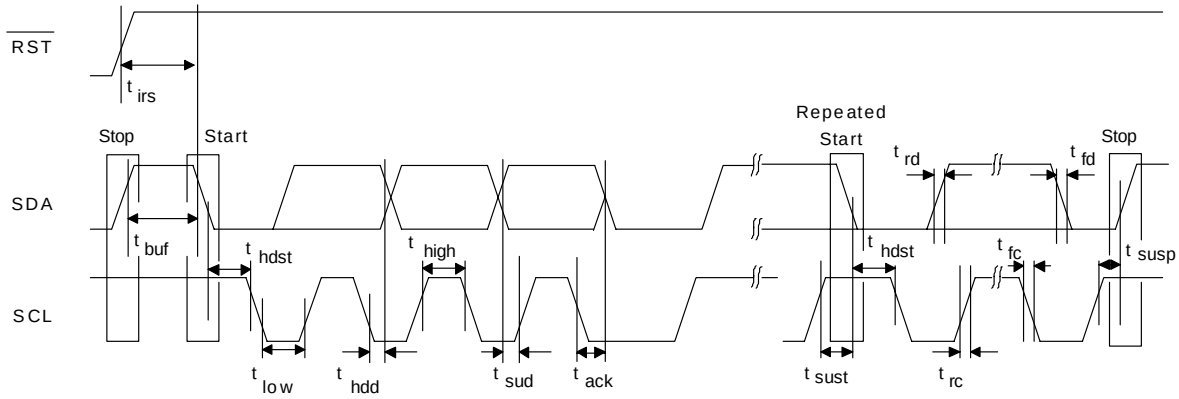


Figure 4. I²C Timing

SWITCHING SPECIFICATIONS - CONTROL PORT - SPI TIMING

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C_L = 30 pF)

Parameter	Symbol	Min	Max	Units
CCLK Clock Frequency	f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling	t_{srs}	20	-	ns
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time[1]	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable	t_{pd}	-	50	ns
Rise Time of CDOUT	t_{r1}	-	25	ns
Fall Time of CDOUT	t_{f1}	-	25	ns
Rise Time of CCLK and CDIN[2]	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN[3]	t_{f2}	-	100	ns

Notes:

1. Data must be held for sufficient time to bridge the transition time of CCLK.
2. For f_{sck} <1 MHz
3. For f_{sck} <1 MHz.

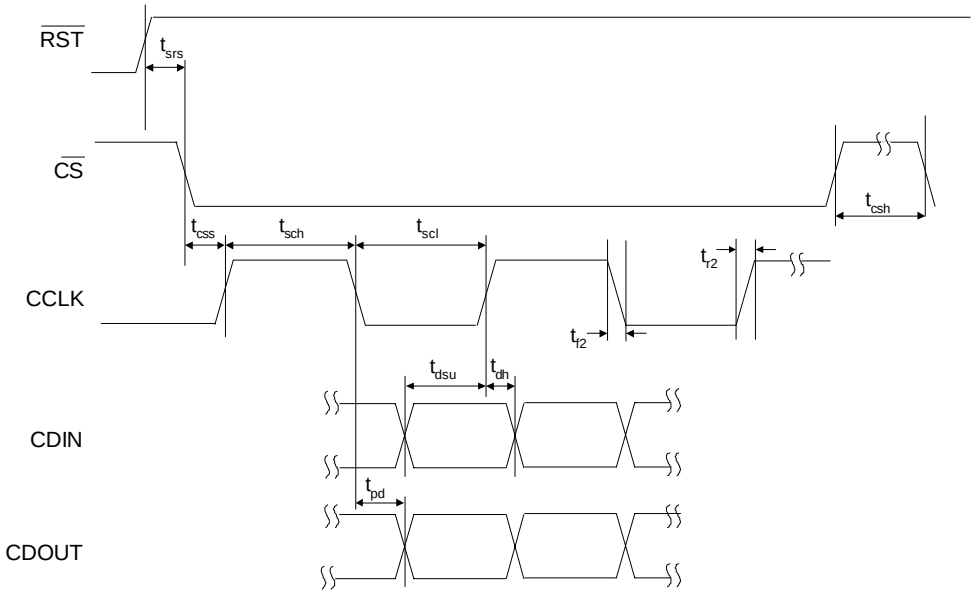


Figure 5. SPI Timing

3. TYPICAL CONNECTION DIAGRAM

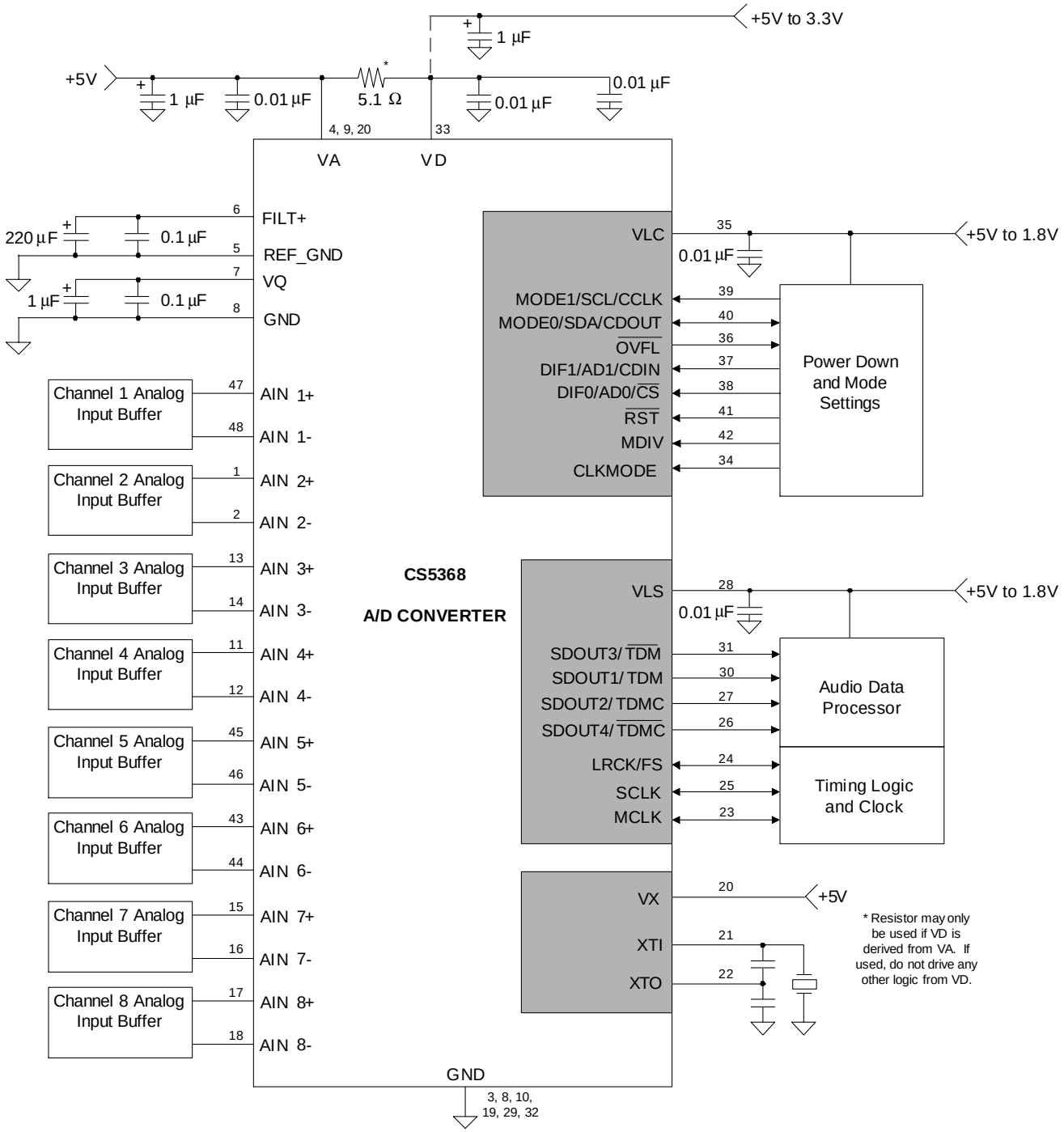


Figure 6. Typical Connection Diagram

For analog buffer configurations, refer to Cirrus Application Note AN241. Also, a low cost single ended to differential solution is provided on the Customer Evaluation Board.

3.1 Suggested Analog Input Buffer

Figure 7. "Recommended Analog Input Buffer" shows a recommended analog input buffer for a differential to differential topology. For additional configurations, refer to Crystal Application Note number AN241. A low-cost, single-ended (RCA jack) to differential solution is shown in the schematics of the Customer Evaluation Board Datasheet (CDB5368).

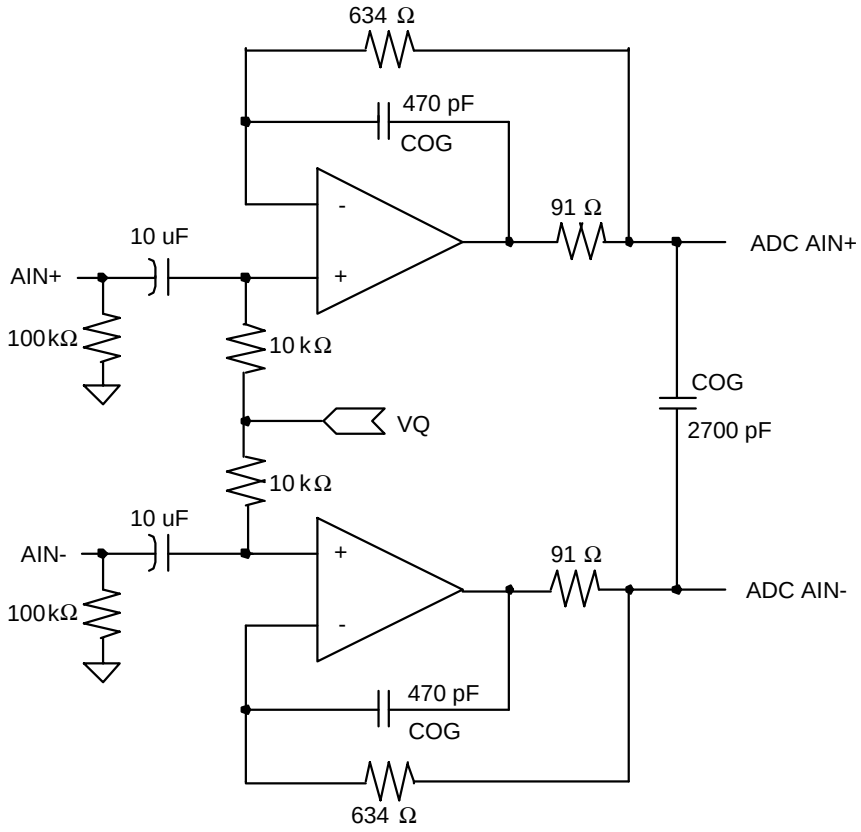


Figure 7. Recommended Analog Input Buffer

4. APPLICATIONS

4.1 Power

For convenient interfacing to external devices, there are five independent power pins for the CS5368. VD powers the digital core. VA powers the analog core. VLS powers the Serial Audio Interface. VLC powers the control logic. VX powers the crystal oscillator. The power pins may have any supported voltage range of the specified voltages supplied simultaneously.

To meet full performance specifications, the CS5368 requires normal low noise board layout. The “Typical Connection Diagram” on page 23 shows the recommended power arrangements, with VA connected to a clean supply. VD, which powers the digital filter, may be run from the system logic supply, or it may be powered from the analog supply via a single-pole decoupling filter.

Decoupling capacitors should be placed as near to the ADC as possible, with the lower value high frequency capacitors being placed nearest to the device leads. Clocks should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the device. The FILT+ and VQ decoupling capacitors must be positioned to minimize the electrical path to ground.

The CDB5368 evaluation board demonstrates an optimum layout for the device.

4.2 Clocking

The device supports clocking through the use of either an on-board crystal oscillator driver or an externally supplied clock. When using the on-board crystal driver, the topology shown in Figure 8. "Crystal Oscillator Topology" must be used. The crystal oscillator manufacturer supplies recommended capacitor values.

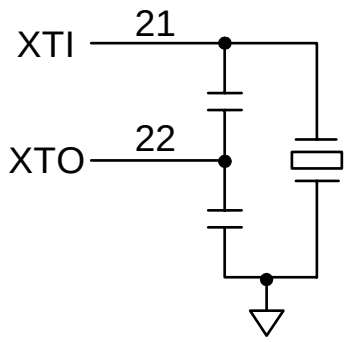


Figure 8. Crystal Oscillator Topology

When using the on-board crystal oscillator driver, the XTI pin is the input for the Master clock (MCLK) to the device. The XTO pin must not be used to drive anything other than the oscillator tank circuitry. Instead, a buffered copy of XTI is available on the MCLK pin, which is level controlled by VLS and may be used to synchronize other parts to the device.

If an external clock is used, the XTI and XTO pins must be grounded, and the MCLK pin becomes an input for the system Master clock.

The CS5368 provides on board master clock dividers that precede all other internal clocking. The available dividers are divide by 1, 1.5, 2, 3, 4.

4.3 Stand-Alone Operation

In Stand-Alone Mode, the CS5368 is programmed exclusively with multi-use configuration pins. This mode provides a set of commonly used features. To utilize the complete set of device features, Control-Port Mode needs to be used.

To use the CS5368 in Stand-Alone Mode, the configuration pins must be held in a stable state and $\overline{RST}$ must be asserted until the power supplies and clocks are stable. Upon de-assertion of $\overline{RST}$ the state of the configuration pins are latched, Vq stabilizes and the device starts sending audio output data.

4.4 Control-Port Operation

In Control-Port Mode, all features of the CS5368 are available. Four multi-use configuration pins become software pins that support the I²C or SPI bus protocol. To initiate Control-Port Mode, a controller that supports I²C or SPI must be used to enable the internal register functionality. This is done by setting the CP-EN bit (bit 7 of the Global Control Port Register). Once CP-EN is set, all of the device configuration pins are ignored, and the internal register settings determine the operating modes of the part.

4.5 DC Offset Control

The CS5368 includes a dedicated high-pass filter for each channel to remove input DC offset at the system level. If a DC level is present, clicks might be heard when switching between devices in a multichannel system.

In Standalone Mode, all of the high pass filters remain enabled. In Control-Port Mode, the high pass filters default to enabled, but may be controlled by writing to the $\overline{HPF}$ register. If any $\overline{HPF}$ bit is taken low, the respective high-pass filter is enabled, and it continuously subtracts a measure of the DC offset from the output of the decimation filter. If any $\overline{HPF}$ bit is taken high during device operation, the value of the DC offset register is frozen, and this DC offset will continue to be subtracted from the conversion result.

4.6 Serial Audio Interface (SAI)

4.6.1 General Description

The SAI port consists of two timing pins, SCLK, LRCK/FS, and four audio data output pins, SDOUT1/TDM, SDOUT2/$\overline{TDM}$, SDOUT3/TDMC and SDOUT4/$\overline{TDMC}$. The SAI port may be operated as a timing master or a timing slave. The port supplies digital audio data in three standard formats, LJ, I²S and TDM. Three sampling ranges are used to provide analog to digital audio conversion from 2 kHz to 216 kHz sampling rates.

The main TDM output port resides on the SDOUT1 pin. The remaining three TDM outputs are used to balance device substrate noise. It is recommended that all four of these nets be routed and loaded identically for best device noise performance.

4.6.2 Master and Slave Operation

In Master mode, the CS5368 outputs SCLK and LRCK/FS which are synchronously derived from MCLK. SCLK is the audio clock which shifts out the individual bits of each sample. In LJ and I²S format, LRCK/FS signifies which channel of data is being shifted out. In TDM Mode, LRCK/FS acts as a frame synchronization signal. A high transition indicates the beginning of a new frame of 8 channels of serial data.

In Slave Mode, SCLK and LRCK/FS become inputs, and the signals must be supplied by another device. The device may be another CS5368 or a microcontroller. Serial data is shifted out by the CS5368 in both cases.

Figure 9. Master Slave Clock Flow

4.6.3 Synchronization of Multiple Devices

To ensure synchronous sampling in applications where multiple ADCs are used, the MCLK and LRCK must be the same for all of the CS5368s in the system. If only one Master clock source is needed, one solution is to place one CS5368 in Master mode, and slave all of the other devices to the one master. If multiple Master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5368 reset de-assertion with the falling edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

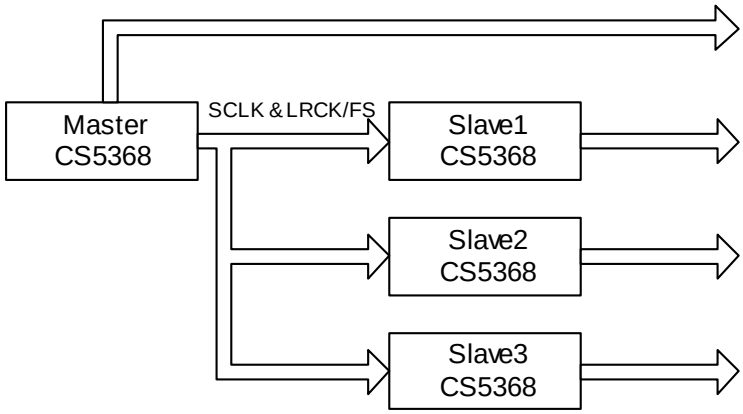


Figure 10. Master and Slave Clocking for a 32-Channel Application

4.6.4 Sample Rate Ranges

Supported sampling rates are 2 kHz-216 kHz divided into three ranges: 2 kHz-54 kHz, 54 kHz-108 kHz, and 108 kHz-216 kHz. These sampling speed modes are called Single-Speed Mode, Double-Speed Mode and Quad-Speed Mode (SSM, DSM, QSM), respectively.

4.6.5 Using M1 and M0 to Set Sampling Parameters

The Master/Slave operation and the sample rate range are controlled through the settings of the M1 and M0 pins in Stand-Alone Mode, or by the M[1] and M[0] bits in the Global Mode Control Register in Control-Port Mode.

M1	M0	Mode	Frequency Range
0	0	Single-Speed Master Mode	2 kHz - 54 kHz
0	1	Double-Speed Master Mode	54 kHz - 108 kHz
1	0	Quadruple-Speed Master Mode	108 kHz - 216 kHz
1	1	Auto-Detected Speed Slave Mode	2 kHz - 216 kHz

Table 2. M1 and M0 Settings

4.6.6 Using DIF1 and DIF0 to Set Serial Audio Interface Format

The format of the data at the Serial Audio Interface ports is controlled by the settings of the DIF1 and DIF0 pins in standalone mode, or by the DIF[1] and DIF[0] bits in the Global Mode Control Register in Control-Port Mode.

.

DIF1	DIF0	Mode
0	0	Left Justified
0	1	I²S
1	0	TDM (2 wire)
1	1	TDM (4 wire)

Table 3. DIF1 and DIF0 Pin Settings

4.6.7 Master Mode Audio Clocking

Figure 11. "Master Mode Clock Dividers" shows the configuration of the MCLK dividers and the sample rate dividers while in Master Mode.

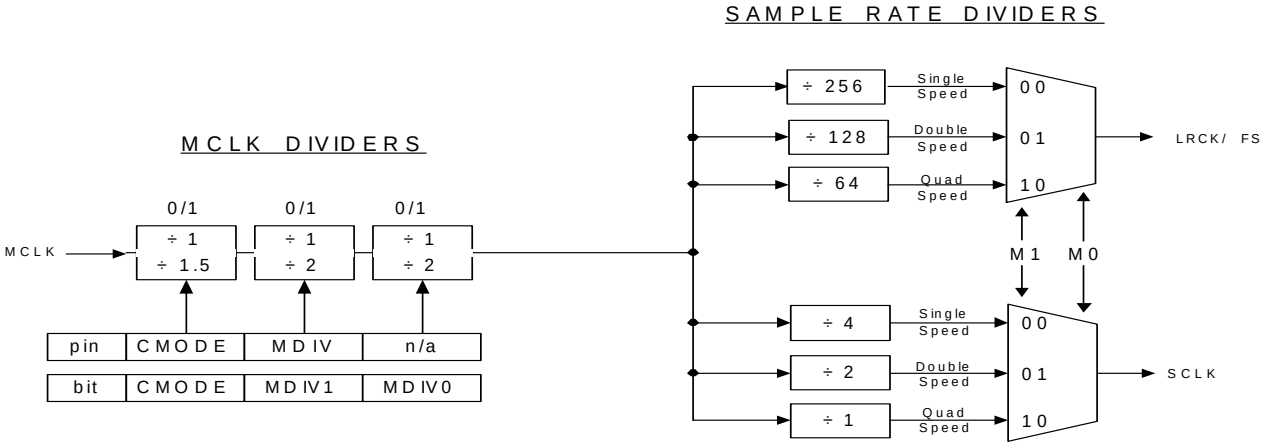


Figure 11. Master Mode Clock Dividers

4.6.8 Slave Mode Audio Clocking

In Slave Mode, the sampling rate is auto-set by examining the incoming MCLK and LRCK/FS signals. LRCK/FS and SCLK operate as inputs in Slave Mode. It is recommended that the LRCK/FS be synchronously derived from the Master clock, and it must be equal to the desired sampling rate, Fs.

4.6.9 Master and Slave Clock Frequencies

Tables 4 through 9 show the clock speeds for sample rates of 48 kHz, 96 kHz and 192 kHz. In Master Mode, the device outputs the frequencies shown. In Slave Mode, the SCLK/LRCK ratio can be set according to design preference. However, device performance is guaranteed only when using the ratios shown in the tables

.

Control Port Mode only

LJ/I²S MASTER OR SLAVE	SSM				
MCLK Divider	**÷4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	**49.152**	36.864	24.576	18.384	12.288
SCLK(MHz)	**3.072**	3.072	3.072	3.072	3.072
MCLK/LRCK Ratio	**1024**	768	512	384	256
SCLK/LRCK Ratio	**64**	64	64	64	64

Table 4. Frequencies for 48 kHz Sample Rate using LJ/I²S

LJ/I²S MASTER OR SLAVE	DSM				
MCLK Divider	**÷4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	**49.152**	36.864	24.567	18.384	12.288
SCLK(MHz)	**6.144**	6.144	6.144	6.144	6.144
MCLK/LRCK Ratio	**512**	384	256	192	128
SCLK/LRCK Ratio	**64**	64	64	64	64

Table 5. Frequencies for 96 kHz Sample Rate using LJ/I²S

LJ/I²S MASTER OR SLAVE	QSM				
MCLK Divider	**÷4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	**49.152**	36.864	24	18.384	12.288
SCLK (MHz)	**12.288**	12.288	12.288	12.288	12.288
MCLK/LRCK Ratio	**256**	192	128	96	64
SCLK/LRCK Ratio	**64**	64	64	64	64

Table 6. Frequencies for 192 kHz Sample Rate using LJ/I²S

TDM MASTER OR SLAVE	SSM				
MCLK Divider	**÷4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	**49.152**	36.864	24.567	18.384	12.288
SCLK (MHz)	**12.288**	12.288	12.288	12.288	12.288
MCLK/FS Ratio	**1024**	768	512	384	256
SCLK/FS Ratio	**256**	256	256	256	256

Table 7. Frequencies for 48 kHz Sample Rate using TDM

TDM MASTER OR SLAVE	DSM				
MCLK Divider	÷4	÷3	÷2	÷1.5	÷1
MCLK (MHz)	**49.152**	36.864	24.567	18.384	12.288
SCLK (MHz)	**24.576**	24.576	24.576	24.576	24.576
MCLK/FS Ratio	**512**	384	256	192	128
SCLK/FS Ratio	**256**	256	256	256	256

Table 8. Frequencies for 96 kHz Sample Rate using TDM

TDM MASTER OR SLAVE	QSM				
MCLK Divider	÷4	÷3	÷2	÷1.5	÷1
MCLK (MHz)	**49.152**	36.864	24.567	18.384	12.288
SCLK (MHz)	**49.152**	49.152	49.152	49.152	49.152
MCLK/FS Ratio	**256**	192	128	96	64
SCLK/FS Ratio	**256**	256	256	256	256

Table 9. Frequencies for 192 kHz Sample Rate using TDM

4.7 Serial Audio Formats

The ADC supports I²S, Left-Justified and TDM digital interface formats. Audio data should be latched by the receiver on the rising edge of SCLK within the specified setup and hold times.

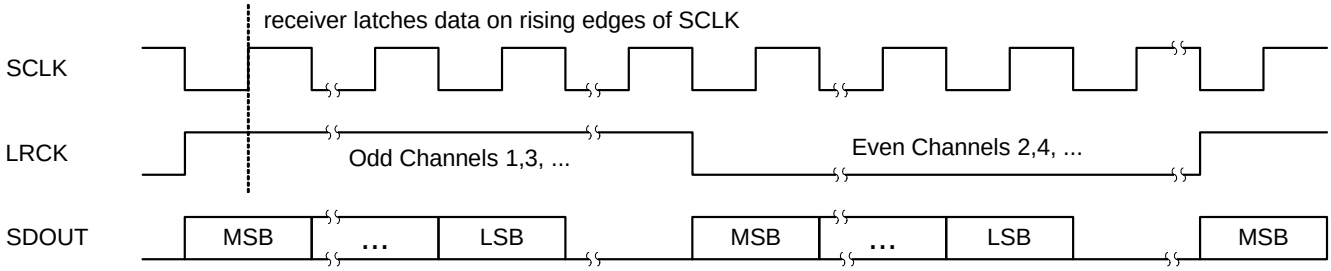


Figure 12. LJ Format

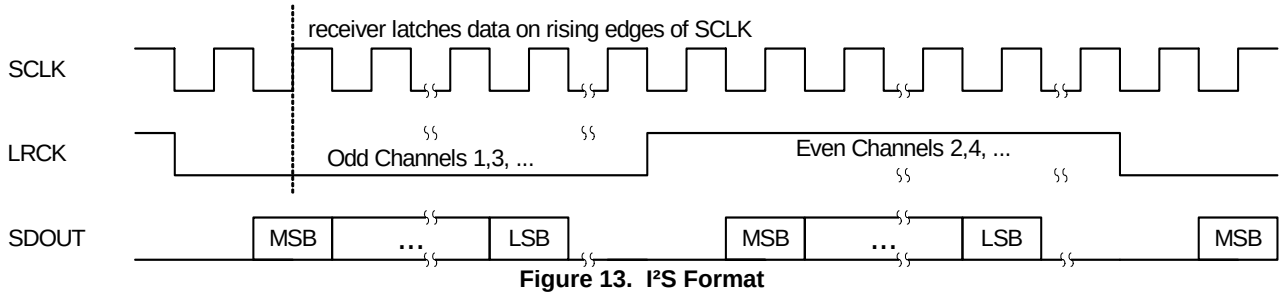


Figure 13. I²S Format

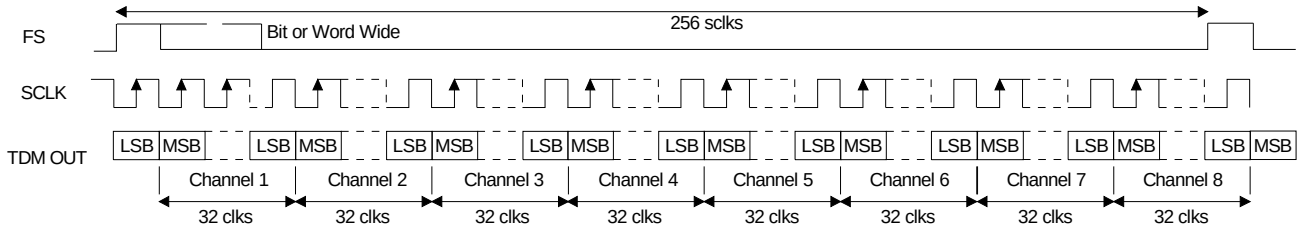


Figure 14. TDM Format

4.7.1 LJ and I²S FORMAT

The left-justified and I²S formats are both two-channel protocols. During one LRCK period, two channels of data are transmitted, odd channels first, then even. The MSB is always clocked out first.

In Slave Mode, if more than 32 SCLKs per channel are received from a Master controller, the CS5368 will fill the longer frame with trailing zeroes. If fewer than 24 SCLKs per channel are received from a Master, the CS5368 will truncate the serial data output to the number of SCLKs received.

4.7.2 TDM Format

In TDM Mode, all eight channels of audio data are serially clocked out during a single Frame Sync (FS) cycle. The rising edge of FS signifies the start of a new TDM frame cycle. Each channel slot occupies 32 SCLKs, with the data left justified and with MSB first. TDM output data should both be latched on the rising edge of SCLK within the specified setup and hold times.

To achieve maximum noise performance, SDOUT2/$\overline{\text{TDM}}$ should be loaded in the same manner as SDOUT1/TDM. For the same reason, it is also recommended that the serial clock be synchronously derived from the Master clock and be equal to 256xFS.

4.8 Overflow Detection

4.8.1 Stand-Alone Mode

The CS5368 includes overflow detection on all input channels. In Stand-Alone Mode, this information is presented as open drain, active low on the $\overline{\text{OVFL}}$ pin. The pin will go to a logical low as soon as an overrange condition in any channel is detected. The data will remain low, then timeout as specified in "Overflow Timeout" on page 19. After the timeout, the $\overline{\text{OVFL}}$ pin will return to a logical high if there has not been any other overrange condition detected. Note that an overrange condition on any channel will restart the timeout period.

4.8.2 Control-Port Mode

In Control-Port mode, the Overflow Status Register interacts with the Overflow Mask Register to provide interrupt capability for each individual channel. See page 36 for details on these two registers.

4.9 Control Port Operation

The Control Port is used to read and write the internal device registers. It supports two industry standard formats, I²C and SPI. The part is in I²C format by default. SPI mode is selected if there is ever a high-to-low transition on the AD0/$\overline{\text{CS}}$ pin after the $\overline{\text{RST}}$ pin has been brought high.

4.9.1 SPI Mode

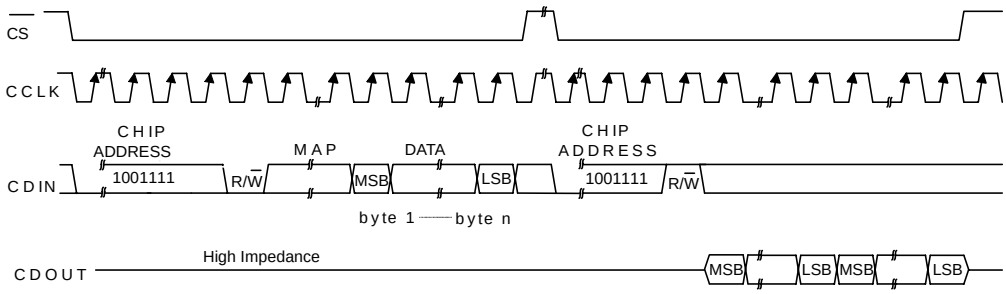
In SPI mode, $\overline{\text{CS}}$ is the CS5368 chip select signal; CCLK is the control port bit clock (input into the CS5368 from a controller); CDIN is the input data line from a controller; CDOUT is the output data line to a controller. Data is clocked in on the rising edge of CCLK and is supplied on the falling edge of CCLK.

To write to a register, bring $\overline{\text{CS}}$ low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/$\overline{\text{W}}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto-increment capability, which is enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle that finishes ($\overline{CS}$ high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively

.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 15. SPI Format

4.9.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is latched when the CS5368 is being released from $\overline{RST}$.

A Start condition is defined as a falling transition of SDA while SCL is high. A Stop condition is a rising transition of SDA while SCL is high. All other transitions of SDA occur while SCL is low. The first byte sent to the CS5368 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper five bits of the 7-bit address field are fixed at 10011. To communicate with a CS5368, the chip address field, which is the first byte sent to the CS5368, should match 10011 and be followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS5368 after each input byte is read and is input to the CS5368 from the microcontroller after each transmitted byte.

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. The write operation is aborted after the acknowledge for the MAP byte by sending a Stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 10011xx0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.

Send stop condition, aborting write.
Send start condition.
Send 10011xx1 (chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

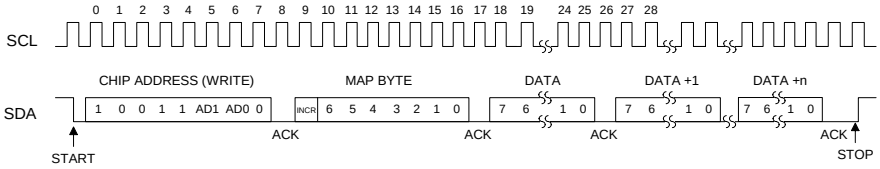


Figure 16. I²C Write Format

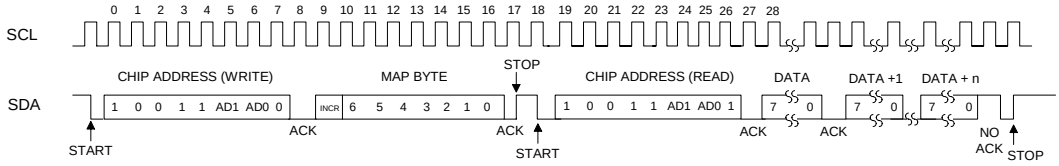


Figure 17. I²C Read Format

5. REGISTER MAP

In Control Port Mode, the bits in these registers are used to control all of the programmable features of the ADC.

5.1 Register Quick Reference

Adr	Name	7	6	5	4	3	2	1	0
00	REVI	CHIP-ID[3:0]				REVISION[3:0]			
01	GCTL	CP-EN	CLKMODE	MDIV[1:0]		DIF[1:0]		MODE[1:0]	
02	OVFL	$\overline{\text{OVFL8}}$	$\overline{\text{OVFL7}}$	$\overline{\text{OVFL6}}$	$\overline{\text{OVFL5}}$	$\overline{\text{OVFL4}}$	$\overline{\text{OVFL3}}$	$\overline{\text{OVFL2}}$	$\overline{\text{OVFL1}}$
03	OVFM	OVFM8	OVFM7	OVFM6	OVFM5	OVFM4	OVFM3	OVFM2	OVFM1
04	HPF	$\overline{\text{HPF8}}$	$\overline{\text{HPF7}}$	$\overline{\text{HPF6}}$	$\overline{\text{HPF5}}$	$\overline{\text{HPF4}}$	$\overline{\text{HPF3}}$	$\overline{\text{HPF2}}$	$\overline{\text{HPF1}}$
05	RESERVED	-	-	-	-	-	-	-	-
06	PDNE	not used		PDN-BG	PDN-OSC	PDN87	PDN65	PDN43	PDN21
07	RESERVED	-	-	-	-	-	-	-	-
08	MUTE	MUTE8	MUTE7	MUTE6	MUTE5	MUTE4	MUTE3	MUTE2	MUTE1
09	RESERVED	-	-	-	-	-	-	-	-
0A	SDEN	not used				$\overline{\text{SDEN4}}$	$\overline{\text{SDEN3}}$	$\overline{\text{SDEN2}}$	$\overline{\text{SDEN1}}$

5.2 00h (REVI) Chip ID Code & Revision Register

R/W	7	6	5	4	3	2	1	0
R	CHIP-ID[3:0]				REVISION[3:0]			

Default: See description

The Chip ID Code & Revision Register is used to store the ID and revision of the chip.

Bits[7:4] contain the chip ID, where the CS5368 is represented with a value of 0x8.

Bits[3:0] contain the revision of the chip, where revision A is represented as 0x0, revision B is represented as 0x1, etc.

5.3 01h (GCTL) Global Mode Control Register

R/W	7	6	5	4	3	2	1	0
R/W	CP-EN	CLKMODE	MDIV[1:0]		DIF[1:0]		MODE[1:0]	

Default: 0x00

The Global Mode Control Register is used to control the Master/Slave Speed modes, the serial audio data format and the Master clock dividers for all channels. It also contains a control port enable bit.

Bit[7] CP-EN manages the Control Port Mode. Until this bit is asserted, all pins behave as if in Stand-Alone Mode. When this bit is asserted, all pins used in Stand-Alone Mode are ignored, and the corresponding register values become functional.

Bit[6] CLKMODE Setting this bit puts the part in 384X mode (divides XTI by 1.5), and clearing the bit invokes 256X mode (divide XTI by 1.0 - pass through).

Bits[5:4] MDIV[1:0] Each bit selects an XTI divider. When either bit is low, an XTI divide by 1 function is selected. When either bit is HIGH, an XTI divide by 2 function is selected. With both bits HIGH, XTI is divided by 4.

The table below shows the composite XTI division using both CLKMODE and MDIV[1:0].

CLKMODE,MDIV[1],MDIV[0]	DESCRIPTION
000	Divide-by-1
100	Divide-by-1.5
001 or 010	Divide-by-2
101 or 110	Divide-by-3
011	Divide-by-4
111	Unused

Bits[3:2] DIF[1:0] Determine which data format the serial audio interface is using to clock out data.

DIF[1:0]
0x00 Left Justified format
0x01 I²S format
0x02 TDM format
0x03 TDM format

Bits[1:0] MODE[1:0] This bit field determines the device sample rate range and whether it is operating as an audio clocking Master or Slave.

MODE[1:0]
0x00 Single-Speed Mode Master
0x01 Double-Speed Mode Master
0x02 Quad-Speed Mode Master
0x03 Slave Mode all speeds

5.4 02h ($\overline{\text{OVFL}}$) Overflow Status Register

R/W	7	6	5	4	3	2	1	0
R	$\overline{\text{OVFL8}}$	$\overline{\text{OVFL7}}$	$\overline{\text{OVFL6}}$	$\overline{\text{OVFL5}}$	$\overline{\text{OVFL4}}$	$\overline{\text{OVFL3}}$	$\overline{\text{OVFL2}}$	$\overline{\text{OVFL1}}$

Default: 0xFF, no overflows have occurred.

Note: This register interacts with Register 03h, the Overflow Mask Register.

The Overflow Status Register is used to indicate an individual overflow in a channel. If an overflow condition on any channel is detected, the corresponding bit in this register is asserted (low) in addition to the open drain active low $\overline{\text{OVFL}}$ pin going low. Each overflow status bit is sticky and is cleared only when read, providing full interrupt capability.

5.5 03h (OVFM) Overflow Mask Register

R/W	7	6	5	4	3	2	1	0
R/W	OVFM8	OVFM7	OVFM6	OVFM5	OVFM4	OVFM3	OVFM2	OVFM1

Default: 0xFF, all overflow interrupts enabled.

The Overflow Mask Register is used to allow or prevent individual channel overflow events from creating activity on the $\overline{\text{OVFL}}$ pin. When a particular bit is set low in the Mask register, the corresponding overflow bit in the Overflow Status register is prevented from causing any activity on the $\overline{\text{OVFL}}$ pin.

5.6 04h ($\overline{\text{HPF}}$) High-Pass Filter Register

R/W	7	6	5	4	3	2	1	0
R/W	$\overline{\text{HPF8}}$	$\overline{\text{HPF7}}$	$\overline{\text{HPF6}}$	$\overline{\text{HPF5}}$	$\overline{\text{HPF4}}$	$\overline{\text{HPF3}}$	$\overline{\text{HPF2}}$	$\overline{\text{HPF1}}$

Default: 0x00, all high-pass filters enabled.

The High-Pass Filter Register is used to enable or disable a high-pass filter that exists for each channel. These filters are used to perform DC offset calibration, a procedure that is detailed in "DC Offset Control" on page 26.

5.7 05h Reserved

R/W	7	6	5	4	3	2	1	0
Reserved	-	-	-	-	-	-	-	-

5.8 06h (PDN) Power Down Register

R/W	7	6	5	4	3	2	1	0
R/W	RESERVED		PDN-BG	PDN-OSC	PDN87	PDN65	PDN43	PDN21

Default: 0x00 - everything powered up

The Power Down Register is used as needed to reduce the chip's power consumption.

Bit[7] **RESERVED**

Bit[6] **RESERVED**

Bit[5] **PDN-BG** When set, this bit powers-down the bandgap reference.

Bit[4] **PDN-OSC** controls power to the internal oscillator core. When asserted, the internal oscillator core is shut down, and no clock is supplied to the chip. If the chip is running off an externally supplied clock at the MCLK pin, it is also prevented from clocking the device internally.

Bit[3:0] **PDN** When any bit is set, all clocks going to a channel pair are turned off, and the serial data outputs are forced to all zeroes.

5.9 07h Reserved

R/W	7	6	5	4	3	2	1	0
Reserved	-	-	-	-	-	-	-	-

5.10 08h (MUTE) Mute Control Register

R/W	7	6	5	4	3	2	1	0
R/W	MUTE8	MUTE7	MUTE6	MUTE5	MUTE4	MUTE3	MUTE2	MUTE1

Default: 0x00, no channels are muted.

The Mute Control Register is used to mute or un-mute the serial audio data output of individual channels. When a bit is set, that channel's serial data is muted by forcing the output to all zeroes.

5.11 09h Reserved

R/W	7	6	5	4	3	2	1	0
Reserved	-	-	-	-	-	-	-	-

5.12 0Ah ($\overline{\text{SDEN}}$) SDOUT Enable Control Register

R/W	7	6	5	4	3	2	1	0
R/W	unused				$\overline{\text{SDEN4}}$	$\overline{\text{SDEN3}}$	$\overline{\text{SDEN2}}$	$\overline{\text{SDEN1}}$

Default: 0x00, all SDOUT pins enabled.

The SDOUT Enable Control Register is used to tri-state the serial audio data output pins. Each bit, when set, tri-states the associated SDOUT pin.

Appendix A Digital Filter Plots

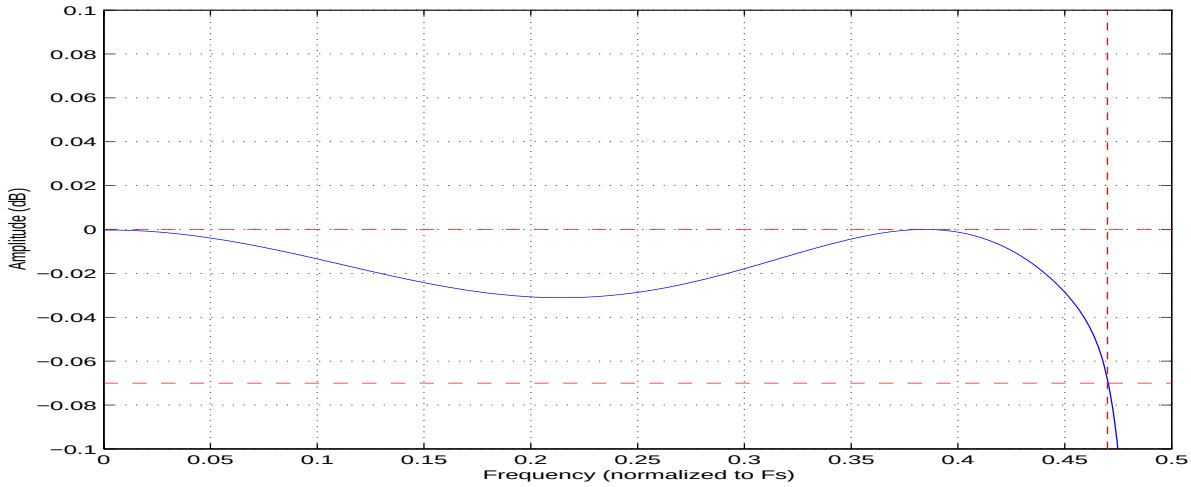


Figure 18. SSM Passband

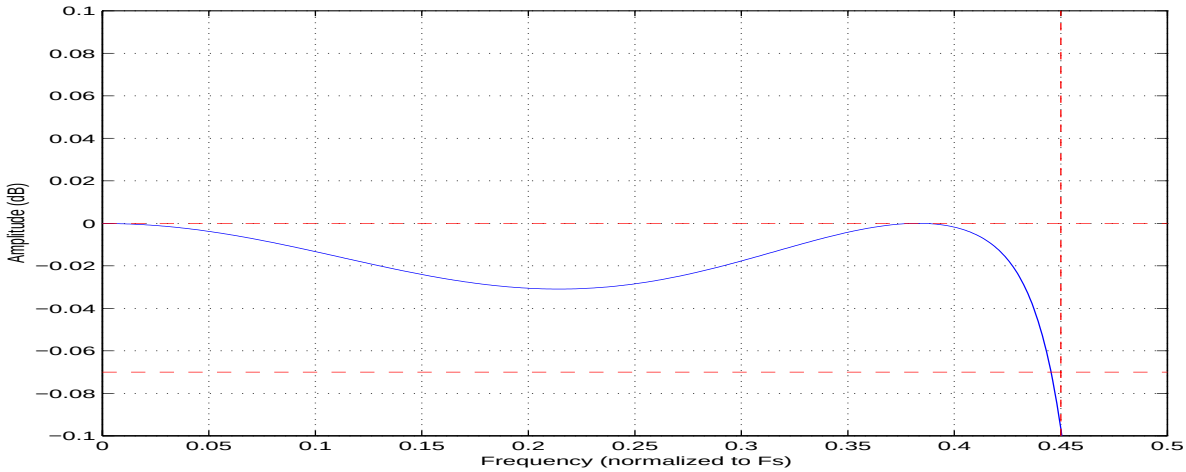


Figure 19. DSM Passband

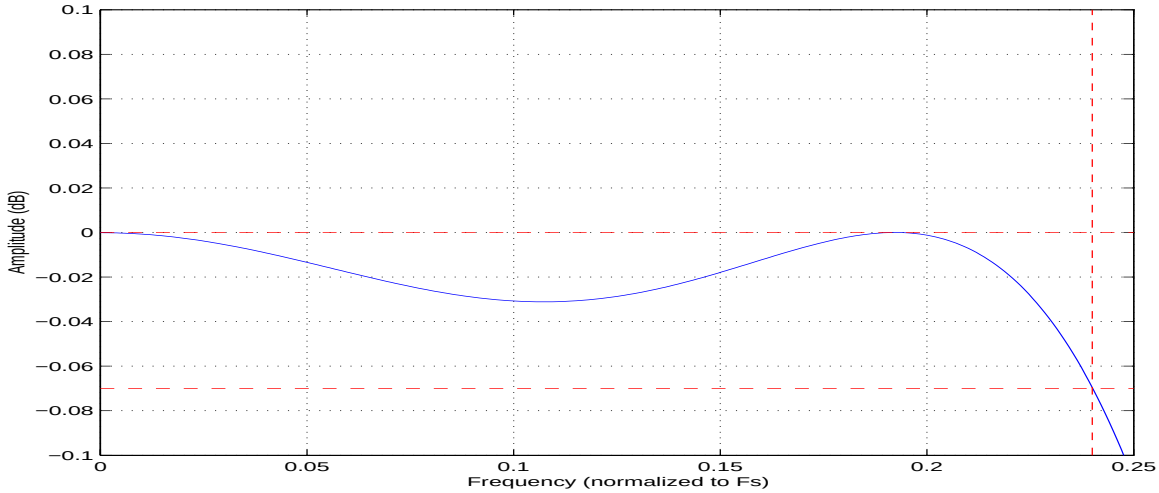


Figure 20. QSM Passband

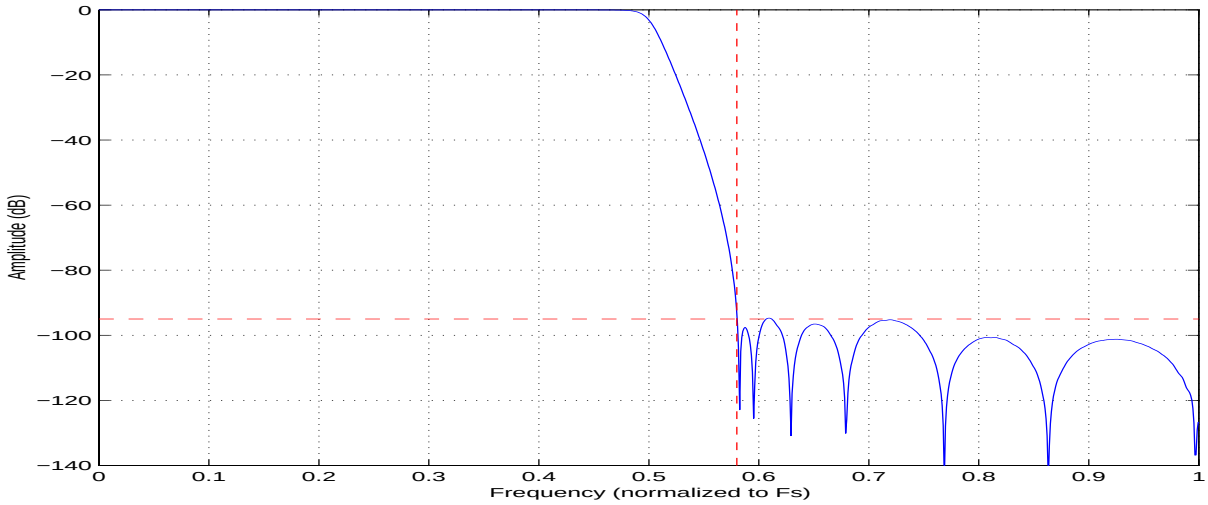


Figure 21. SSM Stopband

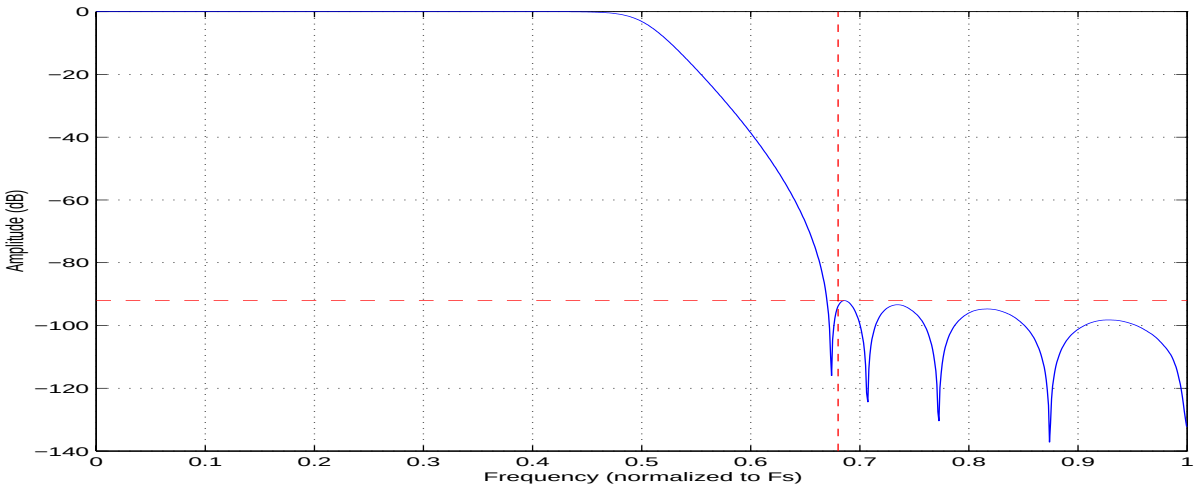


Figure 22. DSM Stopband

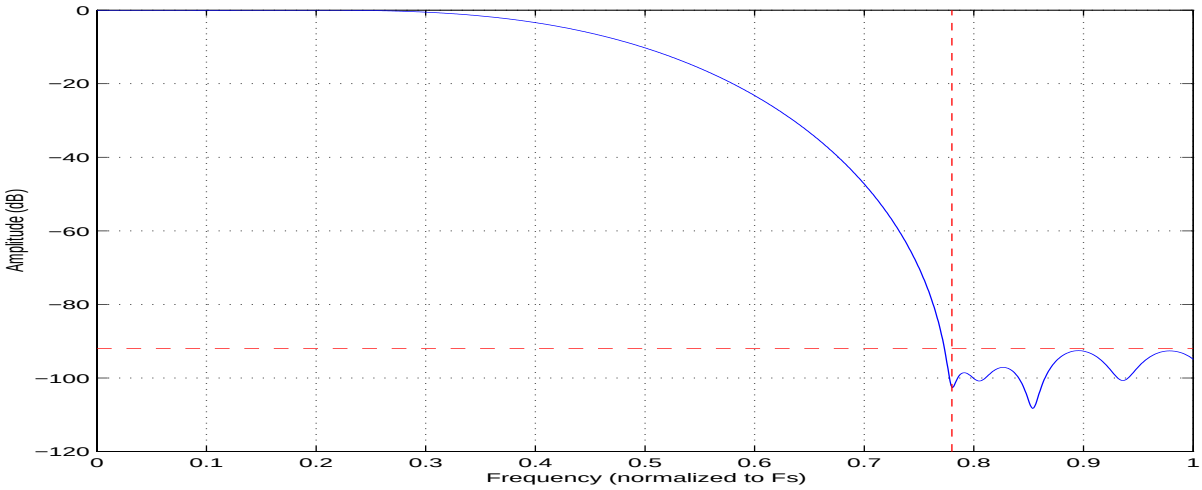


Figure 23. QSM Stopband

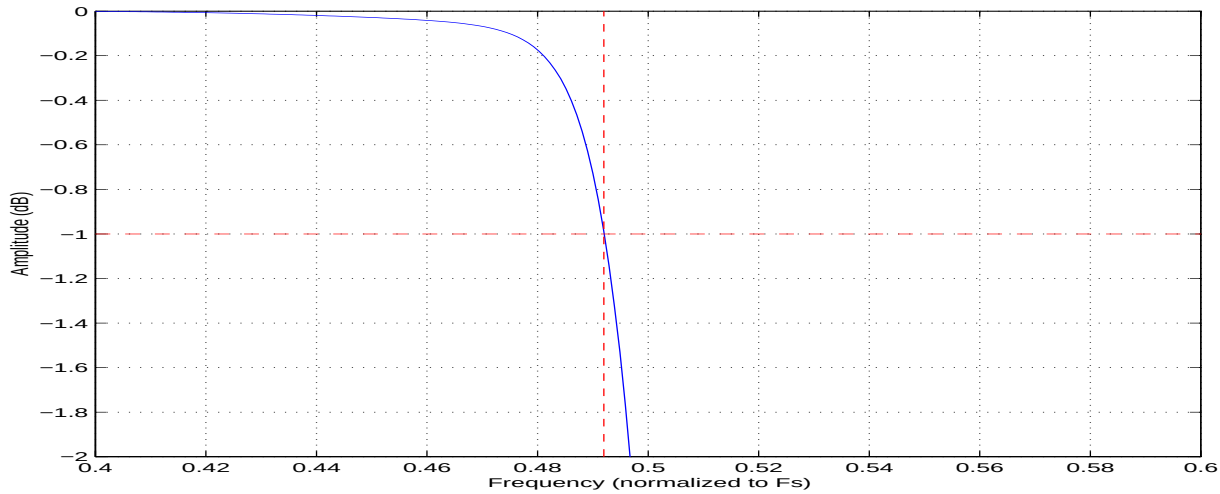


Figure 24. SSM -1 dB Cutoff

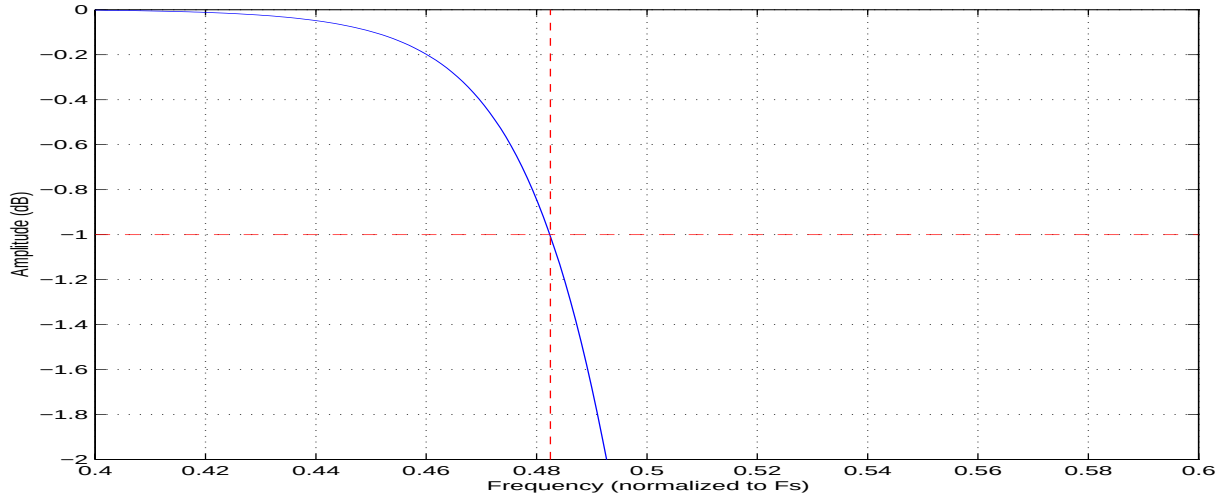


Figure 25. DSM -1 dB Cutoff

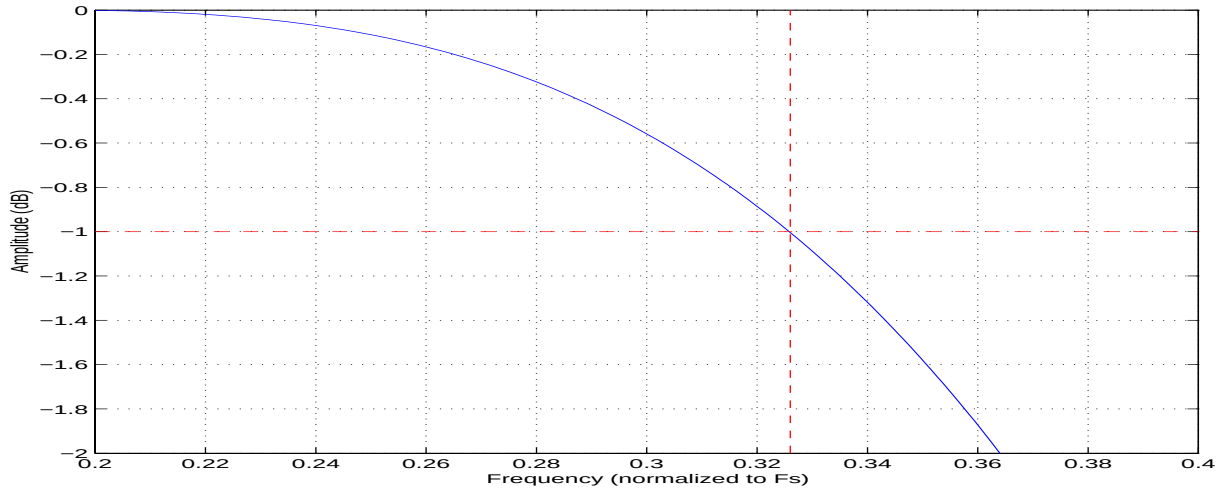


Figure 26. QSM -1 dB Cutoff

Appendix B Parameter Definitions

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-199, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels. The dynamic range is specified with and without an A-weighting filter.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A. Specified using an A-weighting filter.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between one channel and all remaining channels, measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to all other channels. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

Intrachannel Phase Deviation

The deviation from linear phase within a given channel.

Interchannel Phase Deviation

The difference in phase response between channels.

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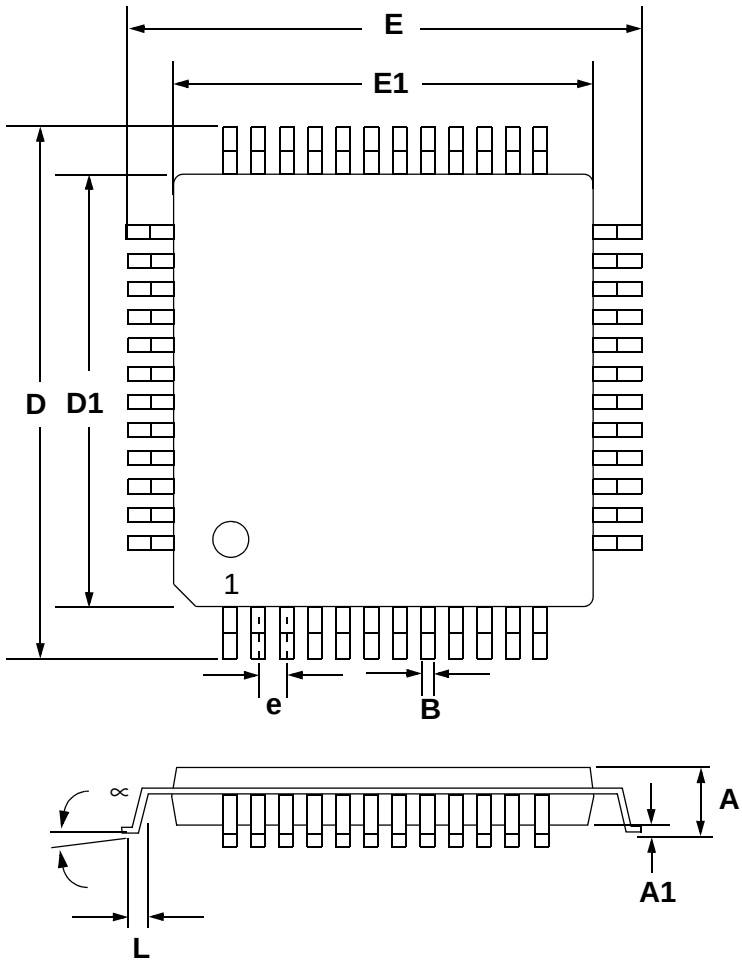
Appendix C Package Dimensions

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm
Controlling dimension is mm. JEDEC Designation: MS026

Table 10. Revision History

Revision	Date	Changes
A1	July 2005	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to http://www.cirrus.com/