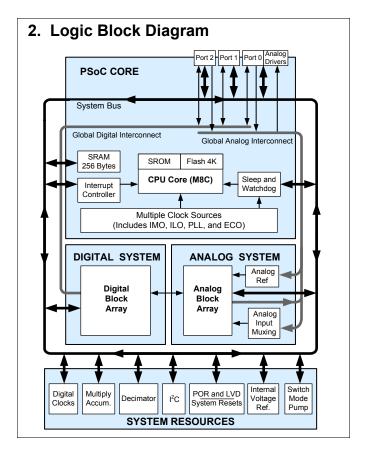


PSoC® Programmable System-on-Chip

1. Features

- Powerful Harvard Architecture Processor
 - M8C Processor speeds to 24 MHz
 - □ 8x8 multiply, 32-Bit accumulate
 - □ Low power at high speed
 - □ 2.4 to 5.25V operating voltage
 - Operating voltages down to 1.0V using on-chip switch mode pump (SMP)
 - □ Industrial temperature range: -40°C to +85°C
- Advanced Peripherals (PSoC® Blocks)
 - ☐ Six rail-to-rail Analog PSoC blocks provide:
 - Up to 14-bit ADCs
 - · Up to 9-bit DACs
 - · Programmable Gain Amplifiers
 - · Programmable filters and comparators
 - □ Four digital PSoC blocks provide:
 - · 8 to 32-Bit timers, counters, and PWMs
 - · CRC and PRS modules
 - Full-Duplex UART
 - Multiple SPI Masters or Slaves
 - · Connectable to All GPIO pins
 - □ Complex peripherals by combining blocks
- Precision, Programmable Clocking
 - □ Internal ±2.5% 24/48 MHz oscillator
 - □ High accuracy 24 MHz with optional 32 kHz crystal and PLL
 - □ Optional external oscillator, up to 24 MHz
 - □ Internal oscillator for Watchdog and Sleep
- Flexible On-Chip Memory
 - □ 4K Flash Program storage 50,000 Erase/Write cycles
 - □ 256 Bytes SRAM data storage
 - □ In-System Serial Programming (ISSP)
 - □ Partial Flash updates
 - □ Flexible protection modes
 - □ EEPROM emulation in Flash
- Programmable Pin Configurations
 - □ 25 mA Sink, 10 mA source on all GPIO
 - □ Pull up, pull down, High Z, Strong, or open Drain Drive modes on all GPIO
 - □ Eight standard Analog Inputs on GPIO, plus four additional analog inputs with restricted routing
 - □ Two 30 mA Analog Outputs on GPIO
 - □ Configurable Interrupt on All GPIO

- New CY8C24x23A PSoC Device
 - □ Derived from the CY8C24x23 device
 - □ Low power and low voltage (2.4V)
- Additional System Resources
 - □ I²C™ Slave, Master, and MultiMaster to 400 kHz
 - □ Watchdog and sleep timers
 - User-configurable low voltage detection
 - □ Integrated supervisory circuit
 - □ On-chip precision voltage reference
- Complete Development Tools
 - □ Free development software (PSoC Designer™)
 - □ Full-featured, In-Circuit Emulator, and Programmer
 - □ Full Speed Emulation
 - Complex breakpoint structure
 - □ 128K trace memory





3. PSoC Functional Overview

The PSoC family consists of many Mixed-Signal Array with On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in Figure 3-1., consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows combining all the device resources into a complete custom system. The PSoC CY8C24x23A family can have up to three I/O ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 6 analog blocks.

3.1 PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 11 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watchdog Timers (WDT).

Memory encompasses 4 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

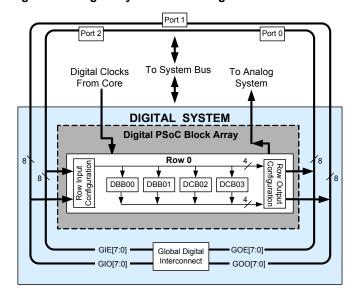
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is required, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin can generate a system interrupt on high level, low level, and change from last read.

3.2 Digital System

The Digital System consists of 4 digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 3-1. Digital System Block Diagram



Digital peripheral configurations are:

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I²C slave and multi-master (one is available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This gives a choice of system resources for your application. Family resources are shown in Table 3-1 on page 4.



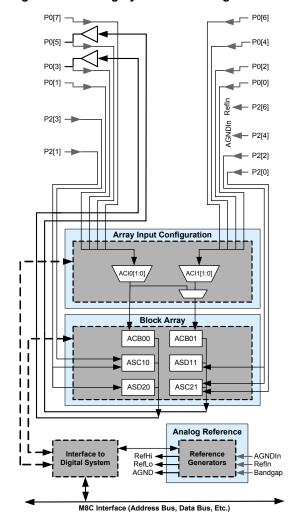
3.1 Analog System

The Analog System consists of six configurable blocks, each consisting of an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC Core resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in Figure 3-2..

Figure 3-2. Analog System Block Diagram



3.1 Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks may be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I²C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master are supported.



- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

3.2 PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 3-1 lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted in this table.

Table 3-1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	12	4	4	12	2K	32K
CY8C27x43	up to 44	2	8	12	4	4	12	256 Bytes	16K
CY8C24x94	49	1	4	48	2	2	6	1K	16K
CY8C24x23	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C24x23A	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C21x34	up to 28	1	4	28	0	2	4 ^[1]	512 Bytes	8K
CY8C21x23	16	1	4	8	0	2	4 ^[1]	256 Bytes	4K
CY8C20x34	up to 28	0	0	28	0	0	3 ^[2]	512 Bytes	8K

4. Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming information, see the PSoC® Programmable System-on-Chip Technical Reference Manual for CY8C24xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

4.1 Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

4.2 Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

4.3 Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

4.4 Cypros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

4.5 Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

4.6 Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Notes

- Limited analog functionality.
- Two analog blocks and one CapSense.



5. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

5.1 PSoC Designer Software Subsystems

5.1.1 System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

5.1.2 Chip-Level View

The chip-level view is a more traditional Integrated Development Environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

5.1.3 Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

5.1.4 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

5.1.5 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

5.1.6 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

5.2 In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.



6. Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

- 1. Select components
- 2. Configure components
- 3. Organize and Connect
- 4. Generate, Verify, and Debug

6.1 Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called "drivers" and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I²C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called "user modules". User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

6.2 Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

6.3 Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

6.4 Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.



7. Document Conventions

7.1 Acronyms Used

The following table lists the acronyms that are used in this document.

Table 7-1. Acronyms Used

Acronym	Description				
AC	alternating current				
ADC	analog-to-digital converter				
API	application programming interface				
CPU	central processing unit				
CT	continuous time				
DAC	digital-to-analog converter				
DC	direct current				
ECO	external crystal oscillator				
EEPROM	electrically erasable programmable read-only memory				
FSR	full scale range				
GPIO	general purpose I/O				
GUI	graphical user interface				
НВМ	human body model				
ICE	in-circuit emulator				
ILO	internal low speed oscillator				
IMO	internal main oscillator				
I/O	input/output				
IPOR	imprecise power on reset				
LSb	least-significant bit				
LVD	low voltage detect				
MSb	most-significant bit				
PC	program counter				
PLL	phase-locked loop				
POR	power on reset				
PPOR	precision power on reset				
PSoC®	Programmable System-on-Chip				
PWM	pulse width modulator				
SC	switched capacitor				
SLIMO	slow IMO				
SMP	switch mode pump				
SRAM	static random access memory				

7.2 Units of Measure

A unit of measure table is located in the section Electrical Specifications on page 17. Table 9-1 on page 14 lists all the abbreviations used to measure the PSoC devices.

7.3 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

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8. Pinouts

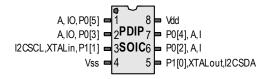
This section describes, lists, and illustrates the CY8C24x23A PSoC device pins and pinout configurations. Every port pin (labeled with a "P") is capable of Digital I/O. However, Vss, Vdd, SMP, and XRES are not capable of Digital I/O.

8.1 8-Pin Part Pinoutt

Table 8-1. Pin Definitions - 8-Pin PDIP and SOIC

Pin	Ту	ре	Pin	Description
No.	Digital	Analog	Name	Description
1	I/O	I/O	P0[5]	Analog Column Mux Input and Column Output
2	I/O	I/O	P0[3]	Analog Column Mux Input and Column Output
3	I/O		P1[1]	Crystal Input (XTALin), I ² C Serial Clock (SCL), ISSP-SCLK*
4	Power		Vss	Ground Connection
5	I/O		P1[0]	Crystal Output (XTALout), I ² C Serial Data (SDA), ISSP-SDATA*
6	I/O	I	P0[2]	Analog Column Mux Input
7	I/O	I	P0[4]	Analog Column Mux Input
8	Power	•	Vdd	Supply Voltage

Figure 8-1. CY8C24123A 8-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

^{*} These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for details.

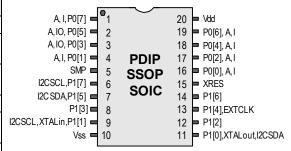


8.1 20-Pin Part Pinout

Table 8-2. Pin Definitions - 20-Pin PDIP, SSOP, and SOIC

Pin	Ту	pe	Pin	Description
No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	Analog Column Mux Input
2	I/O	I/O	P0[5]	Analog Column Mux Input and Column Output
3	I/O	I/O	P0[3]	Analog Column Mux Input and Column Output
4	I/O	I	P0[1]	Analog Column Mux Input
5	Power		SMP	Switch Mode Pump (SMP) Connection to External Components required
6	I/O		P1[7]	I ² C Serial Clock (SCL)
7	I/O		P1[5]	I ² C Serial Data (SDA)
8	I/O		P1[3]	
9	I/O		P1[1]	Crystal Input (XTALin), I ² C Serial Clock (SCL), ISSP-SCLK*
10	Power		Vss	Ground Connection.
11	I/O		P1[0]	Crystal Output (XTALout), I ² C Serial Data (SDA), ISSP-SDATA*
12	I/O		P1[2]	
13	I/O		P1[4]	Optional External Clock Input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active High External Reset with Internal Pull Down
16	I/O	I	P0[0]	Analog Column Mux Input
17	I/O	I	P0[2]	Analog Column Mux Input
18	I/O	I	P0[4]	Analog Column Mux Input
19	I/O	I	P0[6]	Analog Column Mux Input
20	Power		Vdd	Supply Voltage

Figure 8-2. CY8C24223A 20-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

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[+] Feedback

^{*} These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for details.



8.1 28-Pin Part Pinout

Table 8-3. Pin Definitions - 28-Pin PDIP, SSOP, and SOIC

Pin	Ту	ре	Pin	December 1971
No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	Analog Column Mux Input
2	I/O	I/O	P0[5]	Analog Column Mux Input and column output
3	I/O	I/O	P0[3]	Analog Column Mux Input and Column Output
4	I/O	I	P0[1]	Analog Column Mux Input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct Switched Capacitor Block Input
8	I/O	1	P2[1]	Direct Switched Capacitor Block Input
9	Power		SMP	Switch Mode Pump (SMP) Connection to External Components required
10	I/O		P1[7]	I ² C Serial Clock (SCL)
11	I/O		P1[5]	I ² C Serial Data (SDA)
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal Input (XTALin), I ² C Serial Clock (SCL), ISSP-SCLK*
14	Power		Vss	Ground connection.
15	I/O		P1[0]	Crystal Output (XTALout), I ² C Serial Data (SDA), ISSP-SDATA*
16	I/O		P1[2]	
17	I/O		P1[4]	Optional External Clock Input (EXTCLK)
18	I/O		P1[6]	
19	Input		XRES	Active High External Reset with Internal Pull Down
20	I/O	I	P2[0]	Direct Switched Capacitor Block Input
21	I/O	1	P2[2]	Direct Switched Capacitor Block Input
22	I/O		P2[4]	External Analog Ground (AGND)
23	I/O		P2[6]	External Voltage Reference (VRef)
24	I/O	I	P0[0]	Analog Column Mux Input
25	I/O	I	P0[2]	Analog Column Mux Input
26	I/O	I	P0[4]	Analog Column Mux Input
27	I/O	I	P0[6]	Analog Column Mux Input
28	Power		Vdd	Supply Voltage

Figure 8-3. CY8C24423A 28-Pin PSoC Device A, I, P0[7] 28 Widd
27 P0[6], A, I
26 P0[4], A, I
25 P0[2], A, I
24 P0[0], A, I
23 P2[6], External VRef
22 P2[4], External AGND A, IO, P0[5] A, IO, P0[3] 3 A, I, P0[1] P2[7] = P2[5] = A,I, P2[3] = 6 **PDIP** 7 **SSOP** 21 P2[2], A,I 20 P2[0], A,I A, I, P2[1] SOIC SMP = 9 19 = XRES 18 = P1[6] 17 = P1[4],EXTCLK 16 = P1[2] 12CSCL,P1[7] = 10 I2CSDA, P1[5] = 11 P1[3] = 12 I2CSCL,XTALin,P1[1] = 13

15 P1[0],XTALout,I2CSDA

Vss **=** 14

LEGEND : A = Analog, I = Input, and O = Output.

^{*} These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable Sytem-on-Chip Technical Reference Manual* for details.



8.1 32-Pin Part Pinout

Table 8-4. Pin Definitions - 32-Pin QFN**

Pin	Ту	ре	Pin	B		
No.	Digital	Analog	Name	Description		
1	I/O		P2[7]			
2	I/O		P2[5]			
3	I/O	I	P2[3]	Direct Switched Capacitor Block Input		
4	I/O	I	P2[1]	Direct Switched Capacitor Block Input		
5	Power		Vss	Ground Connection		
6	Power		SMP	Switch Mode Pump (SMP) Connection to External Components required		
7	I/O		P1[7]	I ² C Serial Clock (SCL).		
8	I/O		P1[5]	I ² C Serial Data (SDA).		
9			NC	No Connection		
10	I/O		P1[3]			
11	I/O		P1[1]	Crystal Input (XTALin), I ² C Serial Clock (SCL), ISSP-SCLK*		
12	Power		Vss	Ground Connection		
13	I/O		P1[0]	Crystal Output (XTALout), I ² C Serial Data (SDA), ISSP-SDATA*		
14	I/O		P1[2]			
15	I/O		P1[4]	Optional External Clock Input (EXTCLK)		
16			NC	No Connection		
17	I/O		P1[6]			
18	Input		XRES	Active High External Reset with Internal Pull Down		
19	I/O	I	P2[0]	Direct Switched Capacitor Block Input		
20	I/O	I	P2[2]	Direct Switched Capacitor Block Input		
21	I/O		P2[4]	External Analog Ground (AGND)		
22	I/O		P2[6]	External Voltage Reference (VRef)		
23	I/O	I	P0[0]	Analog Column Mux Input		
24	I/O	I	P0[2]	Analog Column Mux Input		
25			NC	No Connection		
26	I/O	I	P0[4]	Analog Column Mux Input		
27	I/O	I	P0[6]	Analog Column Mux Input		
28	Power	•	Vdd	Supply Voltage		
29	I/O	I	P0[7]	Analog Column Mux Input		
30	I/O	I/O	P0[5]	Analog Column Mux Input and Column Output		
31	I/O	I/O	P0[3]	Analog Column Mux Input and Column Output		
32	I/O	I	P0[1]	Analog Column Mux Input		

Figure 8-4. CY8C24423A 32-Pin PSoC Device

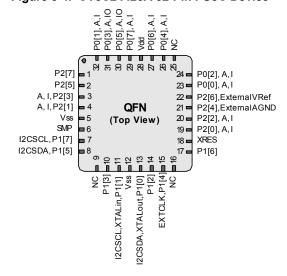
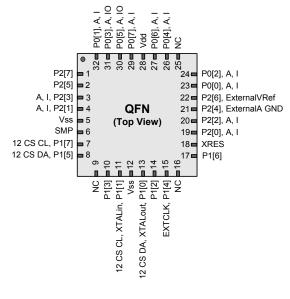


Figure 8-5. CY8C24423A 32-Pin Sawn PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

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^{*} These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for details.

^{**} The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.



8.1 56-Pin Part Pinout

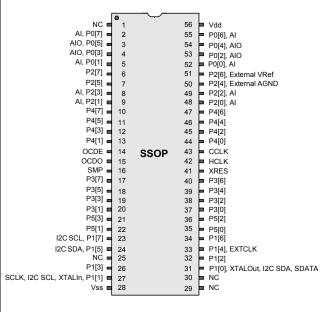
The 56-pin SSOP part is for the CY8C24000A On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 8-5. Pin Definitions - 56-Pin SSOP

		pe				
Pin No.	Digital	Analog	Pin Name	Description		
1	Digital	Allalog	NC	No Connection		
2	I/O	li .	P0[7]	Analog Column Mux Input		
3	I/O	I	P0[5]	Analog Column Mux Input and		
3	1/0	'	i o[o]	Column Output		
4	I/O	I	P0[3]	Analog Column Mux Input and Column Output		
5	I/O	I	P0[1]	Analog Column Mux Input		
6	I/O		P2[7]			
7	I/O		P2[5]			
8	I/O	I	P2[3]	Direct Switched Capacitor Block Input		
9	I/O	I	P2[1]	Direct sWitched Capacitor Block Input		
10	I/O		P4[7]			
11	I/O		P4[5]			
12	I/O	I	P4[3]			
13	I/O	I	P4[1]			
14	OCD		OCD E	OCD Even Data I/O.		
15	OCD		OCD O	OCD Odd Data Output		
16	Power	1	SMP	Switch Mode Pump (SMP) Connection to required External Components		
17	I/O		P3[7]			
18	I/O		P3[5]			
19	I/O		P3[3]			
20	I/O		P3[1]			
21	I/O		P5[3]			
22	I/O		P5[1]			
23	I/O		P1[7]	I ² C Serial Clock (SCL)		
24	I/O		P1[5]	I ² C Serial Data (SDA)		
25			NC	No Connection		
26	I/O		P1[3]			
27	I/O		P1[1]	Crystal Input (XTALin), I ² C Serial Clock (SCL), ISSP-SCLK*		
28	Power	I	Vdd	Supply Voltage		
29			NC	No Connection		
30			NC	No Connection		
31	I/O		P1[0]	Crystal Output (XTALout), I ² C Serial Data (SDA), ISSP-SDATA*		
32	I/O		P1[2]			
33	I/O		P1[4]	Optional External Clock Input (EXTCLK)		

Figure 8-6. CY8C24000A 56-Pin PSoC Device



Not for Production

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Table 8-5. Pin Definitions - 56-Pin SSOP (continued)

Pin			Pin	Description
No.	Digital	Analog	Name	Description
34	I/O		P1[6]	
35	I/O		P5[0]	
36	I/O		P5[2]	
37	I/O		P3[0]	
38	I/O		P3[2]	
39	I/O		P3[4]	
40	I/O		P3[6]	
41	Input		XRES	Active high external reset with internal pull down.
42	OCD		HCLK	OCD high-speed clock output.
43	OCD		CCLK	OCD CPU clock output.
44	I/O		P4[0]	
45	I/O		P4[2]	
46	I/O		P4[4]	
47	I/O		P4[6]	
48	I/O	1	P2[0]	Direct switched capacitor block input.
49	I/O	I	P2[2]	Direct switched capacitor block input.
50	I/O		P2[4]	External Analog Ground (AGND).
51	I/O		P2[6]	External Voltage Reference (VRef).
52	I/O	I	P0[0]	Analog column mux input.
53	I/O	I	P0[2]	Analog column mux input and column output.
54	I/O	I	P0[4]	Analog column mux input and column output.
55	I/O	I	P0[6]	Analog column mux input.
56	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

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^{*} These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for details.



9. Register Reference

This section lists the registers of the CY8C24x23A PSoC device. For detailed register information, refer the *PSoC Programmable Sytem-on-Chip Reference Manual*.

9.1 Register Conventions

9.1.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 9-1. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
С	Clearable register or bit(s)
#	Access is bit specific

9.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

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Table 9-2. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	Nume	40	Access	ASC10CR0	80	RW	Itallic	C0	Access
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	1
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	1
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		7.00110110	88	1444		C8	
PRT2IE	09	RW		49			89			C9	<u> </u>
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	<u> </u>
TITIZDIVIZ	OC OC	IXVV		4C			8C			CC	ļ
	0D			4D			8D			CD	<u> </u>
	0E			4E			8E			CE	<u> </u>
	0F			4F		40000000	8F	DW		CF	
	10			50		ASD20CR0	90	RW		D0	ļ
	11			51		ASD20CR1	91	RW		D1	<u> </u>
	12			52		ASD20CR2	92	RW		D2	<u> </u>
	13			53		ASD20CR3	93	RW	<u> </u>	D3	
	14			54		ASC21CR0	94	RW	<u> </u>	D4	<u> </u>
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E	†		AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	+
	31		ACB00CR0	71	RW	RDIOSYN	B1	RW	 	F1	+
	32		ACB00CR1	72	RW	RDIOIS	B2	RW	 	F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW	 	F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW	 	F4	
	35		ACB01CR3	75	RW	RDI0RO0	B5	RW	<u> </u>	F5	
	36		ACB01CR0	76	RW	RDI0RO1	B6	RW	 	F6	
	37		ACB01CR1	77	RW		B7	1 1 1 7 7	CPU F	F7	RL
	38		, 100010112	78	1111		B8	-	<u> </u>	F8	11/2
	39			79	-		B9		<u> </u>	F9	
							-		 		
	3A			7A	 		BA	1	<u> </u>	FA	
	3B			7B			BB		 	FB	
	3C 3D			7C			BC		 	FC	<u> </u>
				7D	İ		BD	1	i	FD	Ī
							55		OBLL CODY		- ,,
	3E 3F			7E 7F			BE BF		CPU_SCR1 CPU_SCR0	FE FF	#

Blank fields are Reserved and must not be accessed.

Access is bit specific.



Table 9-3. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Acces
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44			84	RW		C4	
						ASD11CR0					
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1											
PRT2IC1	0B	RW		4B			8B			СВ	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW	CDL O IN	D0	RW
									GDI_O_IN		
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54	1	ASC21CR0	94	RW		D4	1
	15			55	-	ASC21CR1	95	RW		D5	-
											ļ
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	<u> </u>
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
OBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
JBB0100		IZVV									
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A		Ī	AA		BDG_TR	EA	RW
	2B	-	-	6B	-	}	AB	-	ECO_TR	EB	W
CD02EN	2C	D\A/									
DCB03FN		RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	<u> </u>
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDIOSYN	B1	RW		F1	-
											ļ
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
-	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	1
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	-
						ADIOIAO I		1744	CDULE		Di
	37		ACB01CR2	77	RW	.	B7		CPU_F	F7	RL
	38			78		<u> </u>	B8			F8	<u> </u>
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	1
											ļ
	3C			7C			BC			FC	
	3D			7D	<u> </u>		BD			FD	<u> </u>
	3E			7E			BE		CPU_SCR1	FE	#
	3E			7F					01 0_00111	· -	**

Blank fields are Reserved and must not be accessed.

Access is bit specific.



10. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23A PSoC device. For the latest electrical specifications, check if you have the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

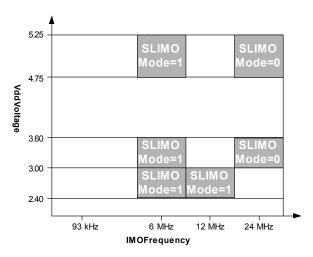
Specifications are valid for -40°C \leq T_A \leq 85°C and T_J \leq 100°C, except where noted.

Refer to Table 10-21 on page 32 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 10-1. Voltage versus CPU Frequency

5.25
4.75
VddVoitage
3.00
2.40
93 kHz 3 MHz 12 MHz 24 MHz
CPUFrequency

Figure 10-2. IMO Frequency Trim Options



The following table lists the units of measure that are used in this section.

Table 10-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure		
°C	degree Celsius	μW	microwatts		
dB	decibels	mA	milli-ampere		
fF	femto farad	ms	milli-second		
Hz	hertz	mV	milli-volts		
KB	1024 bytes	nA	nanoampere		
Kbit	1024 bits	ns	nanosecond		
kHz	kilohertz	nV	nanovolts		
kΩ	kilohm	Ω	ohm		
MHz	megahertz	рА	picoampere		
ΜΩ	megaohm	pF	picofarad		
μΑ	microampere	рр	peak-to-peak		
μF	microfarad	ppm	parts per million		
μΗ	microhenry	ps	picosecond		
μS	microsecond	sps	samples per second		
μV	microvolts	σ	sigma: one standard deviation		
μVrms	microvolts root-mean-square	V	volts		

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10.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10-2. Absolute Maximum Ratings

Symbol	Description	Min	Тур	Max	Units	Notes
T _{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
T _A	Ambient Temperature with Power Applied	-40	-	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	_	+6.0	V	
V _{IO}	DC Input Voltage	Vss - 0.5	-	Vdd + 0.5	V	
V _{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	-	Vdd + 0.5	V	
I _{MIO}	Maximum Current into any Port Pin	-25	-	+50	mA	
ESD	Electro Static Discharge Voltage	2000	-	_	V	Human Body Model ESD.
LU	Latch-up Current	_	-	200	mA	

10.2 Operating Temperature

Table 10-3. Operating Temperature

Symbol	Description	Min	Тур	Max	Units	Notes
T _A	Ambient Temperature	-40	_	+85	°C	
Тл	Junction Temperature	-40	I	+100		The temperature rise from ambient to junction is package specific. See Table 11-1 on page 51. The user must limit the power consumption to comply with this requirement.

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10.3 DC Electrical Characteristics

10.3.1 DC Chip-Level Specifications

Table 10-4 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-4. DC Chip-Level Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
Vdd	Supply Voltage	2.4	-	5.25	V	See DC POR and LVD specifications, Table 10-19 on page 30.
I _{DD}	Supply Current	_	5	8	mA	Conditions are Vdd = $5.0V$, $T_A = 25^{\circ}C$, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0.100 IMO = 24 MHz.
I _{DD3}	Supply Current	-	3.3	6.0	mA	Conditions are Vdd = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = $0.$ IMO = 24 MHz.
I _{DD27}	Supply Current	_	2	4	mA	Conditions are Vdd = $2.7V$, $T_A = 25^{\circ}C$, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz, analog power = off. SLIMO mode = 1. IMO = 6 MHz.
I _{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT. ^[3]	_	3	6.5	μА	Conditions are with internal slow speed oscillator, Vdd = $3.3V$, $-40^{\circ}C \le T_A \le 55^{\circ}C$, analog power = off.
I _{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature. ^[3]	_	4	25	μА	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55°C < T _A ≤ 85°C, analog power = off.
I _{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal. ^[3]	_	4	7.5	μА	Conditions are with properly loaded, 1 μ W max, 32.768 kHz crystal. Vdd = 3.3V, -40°C \leq T _A \leq 55°C, analog power = off.
I _{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature. ^[3]	_	5	26	μА	Conditions are with properly loaded, $1\mu W$ max, 32.768 kHz crystal. Vdd = 3.3 V, $55^{\circ}C$ < $T_A \le 85^{\circ}C$, analog power = off.
V _{REF}	Reference Voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate Vdd. Vdd > 3.0V
V _{REF27}	Reference Voltage (Bandgap)	1.16	1.30	1.32	V	Trimmed for appropriate Vdd. Vdd = 2.4V to 3.0V

Note

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^{3.} Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.



10.3.2 DC General Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-5. 5V and 3.3V DC GPIO Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
R _{PU}	Pull up Resistor	4	5.6	8	kΩ	
R _{PD}	Pull down Resistor	4	5.6	8	kΩ	
V _{OH}	High Output Level	Vdd - 1.0	1	-	V	I_{OH} = 10 mA, Vdd = 4.75 to 5.25V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V _{OL}	Low Output Level		-	0.75	V	I_{OL} = 25 mA, Vdd = 4.75 to 5.25V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I _{OH}	High Level Source Current	10	-	_	mA	V_{OH} = Vdd-1.0V, see the limitations of the total current in the note for V_{OH}
I _{OL}	Low Level Sink Current	25	-	-	mA	V_{OL} = 0.75V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input Low Level	_	-	8.0	V	Vdd = 3.0 to 5.25
V_{IH}	Input High Level	2.1	-		V	Vdd = 3.0 to 5.25
V_{H}	Input Hysterisis	_	60	-	mV	
I _{IL}	Input Leakage (Absolute Value)	-	1	ı	nA	Gross tested to 1 μA
C _{IN}	Capacitive Load on Pins as Input	_	3.5	10	pF	Package and pin dependent. Temp = 25°C
C _{OUT}	Capacitive Load on Pins as Output	_	3.5	10	pF	Package and pin dependent. Temp = 25°C

Table 10-6. 2.7V DC GPIO Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
R _{PU}	Pull up Resistor	4	5.6	8	kΩ	
R _{PD}	Pull down Resistor	4	5.6	8	kΩ	
V _{OH}	High Output Level	Vdd - 0.4	ı	_	V	I_{OH} = 2 mA (6.25 Typ), Vdd = 2.4 to 3.0V (16 mA maximum, 50 mA Typ combined I_{OH} budget).
V _{OL}	Low Output Level	_	ı	0.75	V	I_{OL} = 11.25 mA, Vdd = 2.4 to 3.0V (90 mA maximum combined I_{OL} budget).
Гон	High Level Source Current	2	-	_	mA	V_{OH} = Vdd - 0.4, see the limitations of total current in note for V_{OH} .
V _{IL}	Input Low Level	-	-	0.75	V	Vdd = 2.4 to 3.0
V _{IH}	Input High Level	2.0	_	-	V	Vdd = 2.4 to 3.0
V_{H}	Input Hysteresis	-	90	_	mV	

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Table 10-6. 2.7V DC GPIO Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
I _{OL}	Low Level Sink Current	11.25	-	_	mA	V_{OL} = .75, see the limitations of total current in note for V_{OL} .
I _{IL}	Input Leakage (Absolute Value)	_	1	_	nA	Gross tested to 1 μA
C _{IN}	Capacitive Load on Pins as Input	-	3.5	10	pF	Package and pin dependent. Temp = 25°C
C _{OUT}	Capacitive Load on Pins as Output	-	3.5	10	pF	Package and pin dependent. Temp = 25°C

10.3.3 DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-7. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High		1.6 1.3 1.2	10 8 7.5	mV mV mV	
TCV _{OSOA}	Average Input Offset Voltage Drift	_	7.0	35.0	μV/°C	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	_	20	-	pА	Gross tested to 1 μA
C _{INOA}	Input Capacitance (Port 0 Analog Pins)	-	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V _{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	-	Vdd Vdd - 0.5	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G _{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	60 60 80	-	-	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
V _{OHIGHOA}	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	- - -	_ _ _	V V V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	- - -	- - -	0.2 0.2 0.5	V V V	

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Table 10-7. 5V DC Operational Amplifier Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
I _{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = High	_	150	200	μΑ	
	Power = Low, Opamp Bias = High	_	300	400	μΑ	
	Power = Medium, Opamp Bias = High	_	600	800	μΑ	
	Power = Medium, Opamp Bias = High	_	1200	1600	μΑ	
	Power = High, Opamp Bias = High	_	2400	3200	μΑ	
	Power = High, Opamp Bias = High	_	4600	6400	μΑ	
PSRR _{OA}	Supply Voltage Rejection Ratio	64	80	-	dB	$Vss \le VIN \le (Vdd - 2.25)$ or $(Vdd - 1.25V) \le VIN \le Vdd$

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Table 10-8. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5 Volts Only	_ _	1.65 1.32	10 8	mV mV	
TCV _{OSOA}	Average Input Offset Voltage Drift	_	7.0	35.0	μV/°C	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	-	20	-	pА	Gross tested to 1 μA
C _{INOA}	Input Capacitance (Port 0 Analog Pins)	_	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V _{CMOA}	Common Mode Voltage Range	0.2	-	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G _{OLOA}	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	60 60 80	1	-	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
V _{OHIGHOA}	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	- - -	- - -	V V V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	- - -		0.2 0.2 0.2	V V V	
I _{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High		150 300 600 1200 2400 4600	200 400 800 1600 3200 6400	μΑ μΑ μΑ μΑ μΑ	
PSRR _{OA}	Supply Voltage Rejection Ratio	64	80	-	dB	$Vss \le VIN \le (Vdd - 2.25) \text{ or } \\ (Vdd - 1.25V) \le VIN \le Vdd$

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Table 10-9. 2.7V DC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5 Volts Only	_ _	1.65 1.32	10 8	mV mV	
TCV _{OSOA}	Average Input Offset Voltage Drift	_	7.0	35.0	$\mu V/^{\circ}C$	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	_	20	_	pА	Gross tested to 1 μA
C _{INOA}	Input Capacitance (Port 0 Analog Pins)	_	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V _{CMOA}	Common Mode Voltage Range	0.2	-	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G _{OLOA}	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High	60 60 80	_	-	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
V _{OHIGHOA}	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	_ _ _	_ _ _	V V V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	- - -	_ _ _	0.2 0.2 0.2	V V V	
I _{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	- - - - -	150 300 600 1200 2400 4600	200 400 800 1600 3200 6400	дА дА дА дА дА	
PSRR _{OA}	Supply Voltage Rejection Ratio	64	80	_	dB	$Vss \leq VIN \leq (Vdd - 2.25) \ or \\ (Vdd - 1.25V) \leq VIN \leq Vdd$

10.3.4 DC Low Power Comparator Specifications

Table 10-10 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-10. DC Low Power Comparator Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	ı	Vdd - 1	V	
I _{SLPC}	LPC supply current	-	10	40	μА	
V _{OSLPC}	LPC voltage offset	-	2.5	30	mV	

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10.3.5 DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-11. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOB}	Input Offset Voltage (Absolute Value)	_	3	12	mV	
TCV _{OSOB}	Average Input Offset Voltage Drift	_	+6	_	μV/°C	
V _{CMOB}	Common-Mode Input Voltage Range	0.5	_	Vdd - 1.0	V	
R _{OUTOB}	Output Resistance Power = Low Power = High		1		W	
V _{OHIGHOB}	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.1 0.5 x Vdd + 1.1		- -	V	
V _{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	_ _	_ _	.5 x Vdd - 1.3 0.5 x Vdd - 1.3	V	
I _{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	_ _	1.1 2.6	5.1 8.8	mA mA	
PSRR _{OB}	Supply Voltage Rejection Ratio	52	64	_	dB	V _{OUT} > (Vdd - 1.25).

Table 10-12. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOB}	Input Offset Voltage (Absolute Value)	_	3	12	mV	
TCV _{OSOB}	Average Input Offset Voltage Drift	_	+6	_	μV/°C	
V _{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R _{OUTOB}	Output Resistance Power = Low Power = High		1		W W	
V _{OHIGHOB}	High Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.0 0.5 x Vdd + 1.0		_ _	V	
V _{OLOWOB}	Low Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	_ _		0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	V	
I _{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	_	0.8 2.0	2.0 4.3	mA mA	
PSRR _{OB}	Supply Voltage Rejection Ratio	52	64	_	dB	V _{OUT} > (Vdd - 1.25)

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Table 10-13. 2.7V DC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOB}	Input Offset Voltage (Absolute Value)	_	3	12	mV	
TCV _{OSOB}	Average Input Offset Voltage Drift	_	+6	-	μV/°C	
V _{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R _{OUTOB}	Output Resistance Power = Low Power = High	- -	1 1	_ _	W W	
V _{OHIGHOB}	High Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	0.5 x Vdd + 0.2 0.5 x Vdd + 0.2		_ _	V	
V _{OLOWOB}	Low Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	_ _	_ _	0.5 x Vdd - 0.7 0.5 x Vdd - 0.7	V	
I _{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	-	0.8 2.0	2.0 4.3	mA mA	
PSRR _{OB}	Supply Voltage Rejection Ratio	52	64	_	dB	V _{OUT} > (Vdd - 1.25).

10.3.6 DC Switch Mode Pump Specifications

Table 10-14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-14. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{PUMP} 5V	5V Output Voltage from Pump	4.75	5.0	5.25	V	Configuration listed in footnote. ^[4] Average, neglecting ripple. SMP trip voltage is set to 5.0V.
V _{PUMP} 3V	3.3V Output Voltage from Pump	3.00	3.25	3.60	V	Configuration listed in footnote. ^[4] Average, neglecting ripple. SMP trip voltage is set to 3.25V.
V _{PUMP} 2V	2.6V Output Voltage from Pump	2.45	2.55	2.80	V	Configuration listed in footnote. ^[4] Average, neglecting ripple. SMP trip voltage is set to 2.55V.

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^{4.} $L_1 = 2$ mH inductor, $C_1 = 10$ mF capacitor, $D_1 = S$ chottky diode. See Figure 10-2..



Table 10-14. DC Switch Mode Pump (SMP) Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
Іримр	Available Output Current V_{BAT} = 1.8V, V_{PUMP} = 5.0V V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.3V, V_{PUMP} = 2.55V	5 8 8		-	mA mA mA	Configuration listed in footnote. [4] SMP trip voltage is set to 5.0V. SMP trip voltage is set to 3.25V. SMP trip voltage is set to 2.55V.
V _{BAT} 5V	Input Voltage Range from Battery	1.8	_	5.0	V	Configuration listed in footnote. [4] SMP trip voltage is set to 5.0V.
V _{BAT} 3V	Input Voltage Range from Battery	1.0	-	3.3	V	Configuration listed in footnote. [4] SMP trip voltage is set to 3.25V.
V _{BAT} 2V	Input Voltage Range from Battery	1.0	-	3.0	V	Configuration listed in footnote. [4] SMP trip voltage is set to 2.55V.
V _{BATSTART}	Minimum Input Voltage from Battery to Start Pump	1.2	_	_	V	Configuration listed in footnote. $^{[4]}$ 0°C \leq T _A \leq 100. 1.25V at T _A = -40°C
ΔV _{PUMP_Line}	Line Regulation (over V _{BAT} range)	-	5	-	%V _O	Configuration listed in footnote. [4] V _O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 10-19 on page 30.
ΔV _{PUMP_Load}	Load Regulation	-	5	-	%V _O	Configuration listed in footnote. [4] V _O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 10-19 on page 30.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	_	100	-	mVpp	Configuration listed in footnote. ^[4] Load is 5 mA.
E ₃	Efficiency	35	50	-	%	Configuration listed in footnote. ^[4] Load is 5 mA. SMP trip voltage is set to 3.25V.
E ₂	Efficiency					
F _{PUMP}	Switching Frequency	_	1.3	_	MHz	
DC _{PUMP}	Switching Duty Cycle	_	50	_	%	

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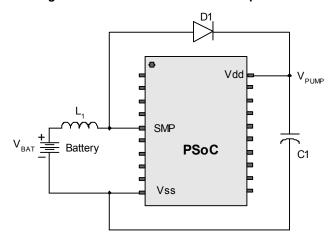


Figure 10-2. Basic Switch Mode Pump Circuit

10.3.7 DC Analog Reference Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, 3.0V to 3.6V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at $25^{\circ}C$ and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 10-15. 5V DC Analog Reference Specifications

Symbol	Description	Min	Тур	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
_	AGND = Vdd/2	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
_	AGND = 2 x BandGap	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
_	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
_	AGND = BandGap	BG - 0.009	BG + 0.008	BG + 0.016	V
_	AGND = 1.6 x BandGap	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
_	AGND Block to Block Variation (AGND = Vdd/2)	-0.034	0.000	0.034	V
_	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
_	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
_	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
_	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
_	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2 P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6]+ 0.100	V
_	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
_	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V
_	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V
_	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
-	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
_	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

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Table 10-16. 3.3V DC Analog Reference Specifications

Symbol	Description	Min Typ		Max	Units		
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V		
_	AGND = Vdd/2	Vdd/2 - 0.03 Vdd/2 - 0.01		Vdd/2 + 0.005	V		
_	AGND = 2 x BandGap		Not Allowed				
_	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V		
_	AGND = BandGap	BG - 0.009	BG + 0.005	BG + 0.015	V		
_	AGND = 1.6 x BandGap	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V		
_	AGND Column to Column Variation (AGND = Vdd/2)	-0.034	0.000	0.034	mV		
_	RefHi = Vdd/2 + BandGap		Not Allowed				
_	RefHi = 3 x BandGap		Not Allowed				
_	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)		Not Allowed				
_	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)		Not Allowed				
_	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V		
_	RefHi = 3.2 x BandGap		Not Allowed				
_	RefLo = Vdd/2 - BandGap		Not Allowed				
_	RefLo = BandGap		Not Allowed				
_	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed					
_	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)	Not Allowed					
_	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V		

Table 10-17. 2.7V DC Analog Reference Specifications

Symbol	Description	Min	Тур	Max	Units		
BG	Bandgap Voltage Reference	1.16	1.30	1.32	V		
_	AGND = Vdd/2	Vdd/2 - 0.03 Vdd/2 - 0.01		Vdd/2 + 0.01	V		
_	AGND = 2 x BandGap		Not Allowed		•		
_	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.01	P2[4]	P2[4] + 0.01	V		
_	AGND = BandGap	BG - 0.01	BG	BG + 0.015	V		
_	AGND = 1.6 x BandGap		Not Allowed		•		
_	AGND Column to Column Variation (AGND = Vdd/2)	-0.034	0.000	0.034	mV		
_	RefHi = Vdd/2 + BandGap		Not Allowed		•		
_	RefHi = 3 x BandGap		Not Allowed				
_	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)		Not Allowed				
_	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)		Not Allowed				
_	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.08	P2[4] + P2[6] - 0.01	P2[4] + P2[6] + 0.06	V		
_	RefHi = 3.2 x BandGap		Not Allowed		•		
_	RefLo = Vdd/2 - BandGap		Not Allowed				
_	RefLo = BandGap		Not Allowed				
_	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed					
_	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed					
_	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.05	P2[4]- P2[6] + 0.01	P2[4] - P2[6] + 0.09	V		

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10.3.8 DC Analog PSoC Block Specifications

Table 11-7. lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$, or 2.4V to 3.0V and $-40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-18. DC Analog PSoC Block Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
R _{CT}	Resistor Unit Value (Continuous Time)	-	12.2	-	kΩ	
C _{SC}	Capacitor Unit Value (Switched Capacitor)	-	80	ı	fF	

10.3.9 DC POR, SMP, and LVD Specifications

Table 11-8. lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40° C \leq T_A \leq 85°C, $\bar{3}.0$ V to 3.6V and -40° C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40° C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for more information on the VLT_CR register.

Table 10-19. DC POR and LVD Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{PPOR0} V _{PPOR1} V _{PPOR2}	Vdd Value for PPOR Trip PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	_	2.36 2.82 4.55	2.40 2.95 4.70	V V V	Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
VLVD0 VLVD1 VLVD2 VLVD3 VLVD4 VLVD5 VLVD6 VLVD7	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 101b VM[2:0] = 111b	2.40 2.85 2.95 3.06 4.37 4.50 4.62 4.71	2.45 2.92 3.02 3.13 4.48 4.64 4.73 4.81	2.51 ^[5] 2.99 ^[6] 3.09 3.20 4.55 4.75 4.83 4.95	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	
VPUMP0 VPUMP1 VPUMP2 VPUMP3 VPUMP4 VPUMP5 VPUMP6 VPUMP7	Vdd Value for SMP Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 111b	2.50 2.96 3.03 3.18 4.54 4.62 4.71 4.89	2.55 3.02 3.10 3.25 4.64 4.73 4.82 5.00	2.62 ^[7] 3.09 3.16 3.32 ^[8] 4.74 4.83 4.92 5.12	V V V V	

- Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.
- Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply. Always greater than 50 mV above V_{LVD0} .
- Always greater than 50 mV above V_{LVD3}.



10.3.10 DC Programming Specifications

Table 11-9. lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-20. DC Programming Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
Vdd _{IWRITE}	Supply Voltage for Flash Write Operations	2.70	_	_	V	
I _{DDP}	Supply Current During Programming or Verify	-	5	25	mA	
V _{ILP}	Input Low Voltage During Programming or Verify	-	-	0.8	V	
V _{IHP}	Input High Voltage During Programming or Verify	2.1	-	_	V	
I _{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	_	_	0.2	mA	Driving internal pull down resistor.
I _{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	_	_	1.5	mA	Driving internal pull down resistor.
V _{OLV}	Output Low Voltage During Programming or Verify	-	-	Vss + 0.75	V	
V _{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	_	Vdd	V	
Flash _{ENPB}	Flash Endurance (per block)	50,000 ^[9]	_	_	_	Erase/write cycles per block
Flash _{ENT}	Flash Endurance (total) ^[10]	1,800,000	-	_	-	Erase/write cycles
Flash _{DR}	Flash Data Retention	10	-	_	Years	

^{9.} The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4V to 3.0V, 3.0V to 3.6V,

^{10.} A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.



10.4 AC Electrical Characteristics

10.4.1 AC Chip-Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-21. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6 ^[11,12,13]	MHz	using factory trim values. See Figure 10-2. on page 17. SLIMO mode = 0.
F _{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5 ^[11,12,13]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 10-2. on page 17. SLIMO mode = 1.
F _{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6 ^[11,12]	MHz	
F _{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3 ^[12,13]	MHz	
F _{48M}	Digital PSoC Block Frequency	0	48	49.2 ^[11,12,14]	MHz	Refer to the AC Digital Block Specifications.
F _{24M}	Digital PSoC Block Frequency	0	24	24.6 ^[12,14]	MHz	
F _{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F _{32K2}	External Crystal Oscillator	_	32.768	_	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F _{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	_	-	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
F _{PLL}	PLL Frequency	_	23.986	_	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	_	_	600	ps	
T _{PLLSLEW}	PLL Lock Time	0.5	_	10	ms	
T _{PLLSLEWSLOW}	PLL Lock Time for Low Gain Setting	0.5	_	50	ms	
T _{OS}	External Crystal Oscillator Startup to 1%	_	1700	2620	ms	
Tosacc	External Crystal Oscillator Startup to 100 ppm	_	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. $3.0V \le Vdd \le 5.5V$, -40 °C $\le T_A \le 85$ °C.
Jitter32k	32 kHz Period Jitter	_	100		ns	
T _{XRST}	External Reset Pulse Width	10	_	_	μS	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC _{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	_	50	_	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2 ^[11,13]	MHz	Trimmed. Using factory trim values.
Jitter24M1P	24 MHz Period Jitter (IMO) Peak-to-Peak	_	300		ps	

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^{11. 4.75}V < Vdd < 5.25V.

^{.... 3.3.0}V < Vdd < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

^{14.} See the individual user module data sheets for information on maximum frequencies for user modules.



Table 10-21. 5V and 3.3V AC Chip-Level Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared	_	-	600	ps	
F _{MAX}	Maximum frequency of signal on row input or row output.	_	-	12.3	MHz	
SR _{POWER_UP}	Power Supply Slew Rate	_	_	250	V/ms	Vdd slew rate during power up.
T _{POWERUP}	Time from end of POR to CPU executing code	_	16	100	ms	Power up from 0V. See the System Resets section of the PSoC Technical Reference Manual.

Table 10-22. 2.7V AC Chip-Level Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{IMO12}	Internal Main Oscillator Frequency for 12 MHz	11.5	12	12.7 ^[15,16,17]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 10-2. on page 17. SLIMO mode = 1.
F _{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5 ^[15,16,17]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 10-2. on page 17. SLIMO mode = 1.
F _{CPU1}	CPU Frequency (2.7V Nominal)	0.93	3	3.15 ^[15,16]	MHz	
F _{BLK27}	Digital PSoC Block Frequency (2.7V Nominal)	0	12	12.7 ^[15,16,17]	MHz	Refer to the AC Digital Block Specifications.
F _{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
F _{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	_	-	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
Jitter32k	32 kHz Period Jitter	_	150		ns	
T _{XRST}	External Reset Pulse Width	10	_	_	μS	
DC12M	12 MHz Duty Cycle	40	50	60	%	
DC _{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Jitter12M1P	12 MHz Period Jitter (IMO) Peak-to-Peak	_	340		ps	
Jitter12M1R	12 MHz Period Jitter (IMO) Root Mean Squared	_	_	600	ps	
F _{MAX}	Maximum frequency of signal on row input or row output.	_	_	12.7	MHz	
SR _{POWER_UP}	Power Supply Slew Rate	_	_	250	V/ms	Vdd slew rate during power up.
T _{POWERUP}	Time from end of POR to CPU executing code	_	16	100	ms	Power up from 0V. See the System Resets section of the PSoC Technical Reference Manual.

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Figure 10-3. PLL Lock Timing Diagram

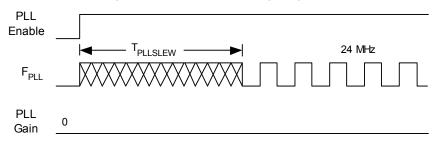


Figure 10-4. PLL Lock for Low Gain Setting Timing Diagram

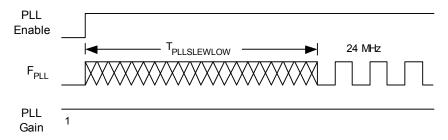


Figure 10-5. External Crystal Oscillator Startup Timing Diagram

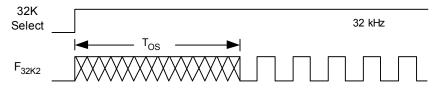


Figure 10-6. 24 MHz Period Jitter (IMO) Timing Diagram



Notes

^{15. 2.4}V < Vdd < 3.0V.

^{16.} Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.

^{17.} See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on maximum frequency for User Modules.



Figure 10-7. 32 kHz Period Jitter (ECO) Timing Diagram



10.4.2 AC General Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

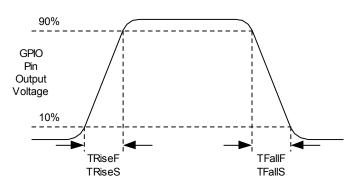
Table 10-23. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{GPIO}	GPIO Operating Frequency	0	_	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	_	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	_	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	_	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	-	ns	Vdd = 3 to 5.25V, 10% - 90%

Table 10-24. 2.7V AC GPIO Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{GPIO}	GPIO Operating Frequency	0	_	3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	6	-	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	6	-	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%

Figure 10-8. GPIO Timing Diagram



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10.4.3 AC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V and 2.7V.

Table 10-25. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units
T _{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	_	_	3.9	μS
	Power = Medium, Opamp Bias = High	_	_	0.72	μS
	Power = High, Opamp Bias = High	_	_	0.62	μS
T _{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	_	_	5.9	μS
	Power = Medium, Opamp Bias = High	_	_	0.92	μS
	Power = High, Opamp Bias = High	_	_	0.72	μS
SR _{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain)				
11071	Power = Low, Opamp Bias = Low	0.15	_	_	V/μs
	Power = Medium, Opamp Bias = High	1.7	_	_	V/µs
	Power = High, Opamp Bias = High	6.5	_	_	V/μs
SR _{FOA}	Falling Slew Rate (20% to 80%) (10 pF load, Unity Gain)				
1 0/1	Power = Low, Opamp Bias = Low	0.01	_	_	V/μs
	Power = Medium, Opamp Bias = High	0.5	_	_	V/μs
	Power = High, Opamp Bias = High	4.0	_	_	V/μs
BW _{OA}	Gain Bandwidth Product				
0,1	Power = Low, Opamp Bias = Low	0.75	_	_	MHz
	Power = Medium, Opamp Bias = High	3.1	_	-	MHz
	Power = High, Opamp Bias = High	5.4	_	_	MHz
E _{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	_	100	_	nV/rt-Hz

Table 10-26. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units
T _{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	_	_	3.92	μS
	Power = Medium, Opamp Bias = High	_	_	0.72	μS
T _{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	_	_	5.41	μS
	Power = Medium, Opamp Bias = High	_	_	0.72	μS
SR _{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.31	_	_	V/μs
	Power = Medium, Opamp Bias = High	2.7	_	_	V/μs
SR _{FOA}	Falling Slew Rate (20% to 80%) (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.24	_	_	V/μs
	Power = Medium, Opamp Bias = High	1.8	_	_	V/μs
BW _{OA}	Gain Bandwidth Product				
	Power = Low, Opamp Bias = Low	0.67	_	_	MHz
	Power = Medium, Opamp Bias = High	2.8	_	_	MHz
E _{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	-	100	_	nV/rt-Hz

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Table 10-27. 2.7V AC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units
T _{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	_	_	3.92	μS
	Power = Medium, Opamp Bias = High	_	_	0.72	μS
T _{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	_	_	5.41	μS
	Power = Medium, Opamp Bias = High	_	_	0.72	μS
SR _{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.31	_	_	V/μs
	Power = Medium, Opamp Bias = High	2.7	_	_	V/μs
SR _{FOA}	Falling Slew Rate (20% to 80%) (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.24	_	_	V/μs
	Power = Medium, Opamp Bias = High	1.8	_	_	V/μs
BW _{OA}	Gain Bandwidth Product				
	Power = Low, Opamp Bias = Low	0.67	_	_	MHz
	Power = Medium, Opamp Bias = High	2.8	_	_	MHz
E _{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	-	100	_	nV/rt-Hz

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When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

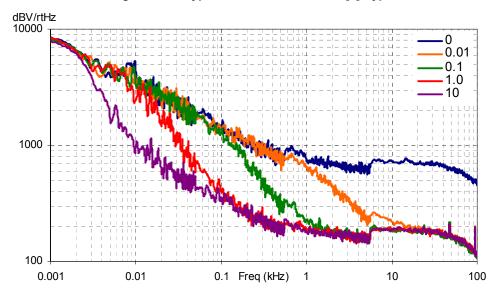


Figure 10-9. Typical AGND Noise with P2[4] Bypass

At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

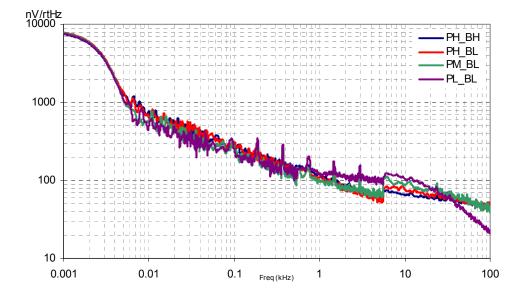


Figure 10-10. Typical Opamp Noise



10.4.4 AC Low Power Comparator Specifications

Table 10-28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-28. AC Low Power Comparator Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
T _{RLPC}	LPC response time	_	_	50	μS	≥ 50 mV overdrive comparator
						reference set within V _{REFLPC}

10.4.5 AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-29. 5V and 3.3V AC Digital Block Specifications

Function	Description	Min	Тур	Max	Units	Notes
Timer	Capture Pulse Width	50 ^[18]	_	_	ns	
	Maximum Frequency, No Capture	_	_	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, With Capture	_	_	24.6	MHz	
Counter	Enable Pulse Width	50 ^[18]	_	_	ns	
	Maximum Frequency, No Enable Input	_	_	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, Enable Input	_	_	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	_	_	ns	
	Synchronous Restart Mode	50 ^[18]	_	_	ns	
	Disable Mode	50 ^[18]	_	_	ns	
	Maximum Frequency	_	_	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	_	_	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	-	-	24.6	MHz	
SPIM	Maximum Input Clock Frequency	_	-	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	_	_	4.1	ns	
	Width of SS_Negated Between Transmissions	50 ^[18]	_	_	ns	
Transmitter	Maximum Input Clock Frequency	-	-	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	_	_	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	-	_	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	-	_	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

Note

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^{18.50} ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).



Table 10-30. 2.7V AC Digital Block Specifications

Function	Description	Min	Тур	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			12.7	MHz	2.4V < Vdd < 3.0V
Timer	Capture Pulse Width	100 ^[19]	_	_	ns	
	Maximum Frequency, With or Without Capture	-	_	12.7	MHz	
Counter	Enable Pulse Width	100 ^[19]	_	_	ns	
	Maximum Frequency, No Enable Input	-	_	12.7	MHz	
	Maximum Frequency, Enable Input	-	_	12.7	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	_	_	ns	
	Synchronous Restart Mode	100 ^[19]	_	_	ns	
	Disable Mode	100 ^[19]	_	_	ns	
	Maximum Frequency	_	_	12.7	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	1	-	12.7	MHz	
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	_	_	12.7	MHz	
SPIM	Maximum Input Clock Frequency	_	_	6.35	MHz	Maximum data rate at 3.17 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	-	-	4.23	ns	
	Width of SS_Negated Between Transmissions	100 ^[19]	_	_	ns	
Transmitter	Maximum Input Clock Frequency	_	_	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	_	_	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.

Note

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^{19.50} ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).



10.4.6 AC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-31. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Units
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High			2.5 2.5	μ s μ s
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High		_ _	2.2 2.2	μ s μ s
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	0.65 0.65	_ _	<u>-</u>	V/μs V/μs
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	0.65 0.65		<u>-</u>	V/μs V/μs
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	0.8 0.8		_ _	MHz MHz
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	300 300	_ _	_ _	kHz kHz

Table 10-32. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Units
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	- -	_ _	3.8 3.8	μs μs
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	- -	_ _	2.6 2.6	μs μs
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	0.5 0.5	_ _	<u>-</u>	V/μs V/μs
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	0.5 0.5	_ _	<u>-</u>	V/μs V/μs
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	0.7 0.7	_ _	-	MHz MHz
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	200 200	_ _	- -	kHz kHz

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Table 10-33. 2.7V AC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Units
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	_ _	_ _	4 4	μ s μ s
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	- -	_ _	3 3	μs μs
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	0.4 0.4	_ _	_ _	V/μs V/μs
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	0.4 0.4	_ _	_ _	V/μs V/μs
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	0.6 0.6	_ _	_ _	MHz MHz
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	180 180	_ _	_ _	kHz kHz

10.4.7 AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-34. 5V AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units
F _{OSCEXT}	Frequency	0.093	_	24.6	MHz
_	High Period	20.6	_	5300	ns
_	Low Period	20.6	_	_	ns
_	Power Up IMO to Switch	150	_	_	μS

Table 10-35. 3.3V AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units
F _{OSCEXT}	Frequency with CPU Clock divide by 1 ^[20]	0.093	_	12.3	MHz
F _{OSCEXT}	Frequency with CPU Clock divide by 2 or greater ^[21]	0.186	_	24.6	MHz
_	High Period with CPU Clock divide by 1	41.7	_	5300	ns
_	Low Period with CPU Clock divide by 1	41.7	_	_	ns
_	Power Up IMO to Switch	150	-	-	μS

Notes

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^{20.} Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.

^{21.} If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met



Table 10-36. 2.7V AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU Clock divide by 1 ^[22]	0.093	_	12.3	MHz	
F _{OSCEXT}	Frequency with CPU Clock divide by 2 or greater ^[23]	0.186	-	12.3	MHz	
_	High Period with CPU Clock divide by 1	41.7	_	5300	ns	
_	Low Period with CPU Clock divide by 1	41.7	_	-	ns	
_	Power Up IMO to Switch	150	_	-	μS	

10.4.8 AC Programming Specifications

Table 10-37 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 10-37. AC Programming Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
T _{RSCLK}	Rise Time of SCLK	1	-	20	ns	
T _{FSCLK}	Fall Time of SCLK	1	_	20	ns	
T _{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	_	_	ns	
T _{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	_	_	ns	
F _{SCLK}	Frequency of SCLK	0	_	8	MHz	
T _{ERASEB}	Flash Erase Time (Block)	_	20	_	ms	
T _{WRITE}	Flash Block Write Time	_	80	_	ms	
T _{DSCLK}	Data Out Delay from Falling Edge of SCLK	_	_	45	ns	Vdd > 3.6
T _{DSCLK3}	Data Out Delay from Falling Edge of SCLK	_	_	50	ns	$3.0 \leq Vdd \leq 3.6$
T _{DSCLK2}	Data Out Delay from Falling Edge of SCLK	_	_	70	ns	$2.4 \leq Vdd \leq 3.0$
T _{ERASEALL}	Flash Erase Time (Bulk)	-	20	_	ms	Erase all Blocks and protection fields at once
T _{PROGRAM_HOT}	Flash Block Erase + Flash Block Write Time	_	_	200 ^[24]	ms	0°C <= Tj <= 100°C
T _{PROGRAM_COL}	Flash Block Erase + Flash Block Write Time	-	_	400 ^[24]	ms	-40°C <= Tj <= 0°C

Notes

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^{22.} Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.

^{23.} If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

^{24.} For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.



10.4.9 AC I²C Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, or 2.4V to 3.0V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

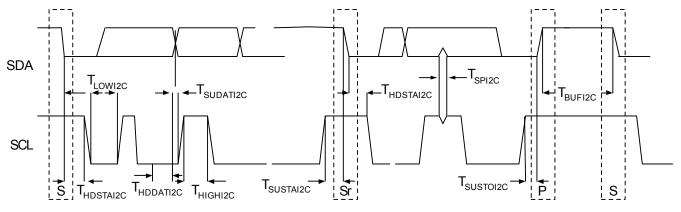
Table 10-38. AC Characteristics of the I²C SDA and SCL Pins for Vdd > 3.0V

Symbol	Description	Standar	d Mode	Fast I	Mode	Units
Symbol	Description	Min	Max	Min	Max	Ullits
F _{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
T _{HDSTAI2C}	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	_	0.6	_	μS
T _{LOWI2C}	LOW Period of the SCL Clock	4.7	_	1.3	-	μS
T _{HIGHI2C}	HIGH Period of the SCL Clock	4.0	_	0.6	-	μS
T _{SUSTAI2C}	Setup Time for a Repeated START Condition	4.7	_	0.6	-	μS
T _{HDDATI2C}	Data Hold Time	0	_	0	-	μS
T _{SUDATI2C}	Data Setup Time	250	_	100 ^[25]	-	ns
T _{SUSTOI2C}	Setup Time for STOP Condition	4.0	_	0.6	-	μS
T _{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	_	1.3	-	μS
T _{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	_	_	0	50	ns

Table 10-39. AC Characteristics of the I²C SDA and SCL Pins for Vdd < 3.0V (Fast Mode Not Supported)

Symbol	Description	Standard	d Mode	Fast	Units			
Symbol	Description	Min	Max	Min	Max	Onits		
F _{SCLI2C}	SCL Clock Frequency	0	100	_	_	kHz		
T _{HDSTAI2C}	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	_	-	_	μS		
T _{LOWI2C}	LOW Period of the SCL Clock	4.7	_	_	_	μS		
T _{HIGHI2C}	HIGH Period of the SCL Clock		_	_	_	μS		
T _{SUSTAI2C}	Setup Time for a Repeated START Condition		_	_	-	μS		
T _{HDDATI2C}	Data Hold Time		_	_	_	μS		
T _{SUDATI2C}			_	_	-	ns		
T _{SUSTOI2C}	Setup Time for STOP Condition	4.0	_	-	-	μS		
T _{BUFI2C}	Bus Free Time Between a STOP and START Condition		_	_	_	μS		
T _{SPI2C}	Pulse Width of spikes are suppressed by the input filter	-	_	_	_	ns		

Figure 10-11. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

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^{25.} A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement t_{SU:DAT} Š 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU:DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.



11. Packaging Information

This section illustrates the packaging specifications for the CY8C24x23A PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

11.1 Packaging Dimensions

Figure 11-1. 8-Pin (300-Mil) PDIP

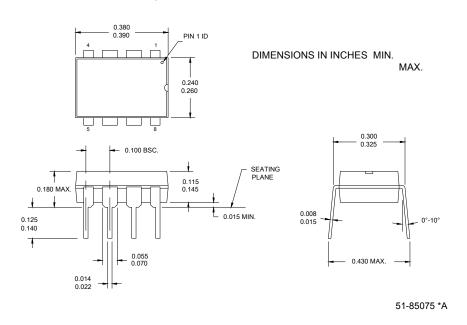
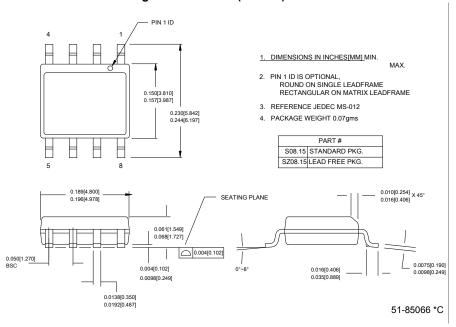


Figure 11-2. 8-Pin (150-Mil) SOIC



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Figure 11-3. 20-Pin (300-Mil) Molded DIP

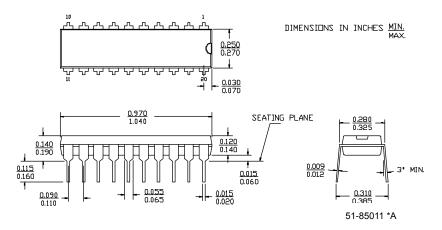
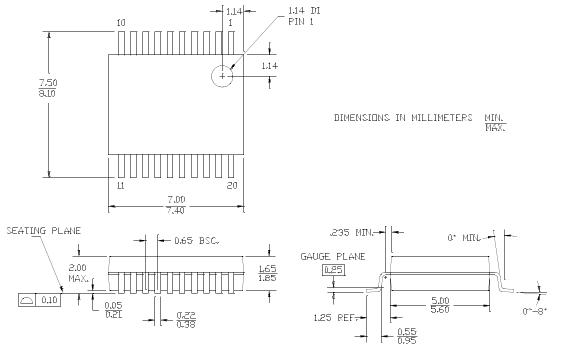


Figure 11-4. 20-Pin (210-Mil) SSOP



51-85077 *C



Figure 11-5. 20-Pin (300-Mil) Molded SOIC

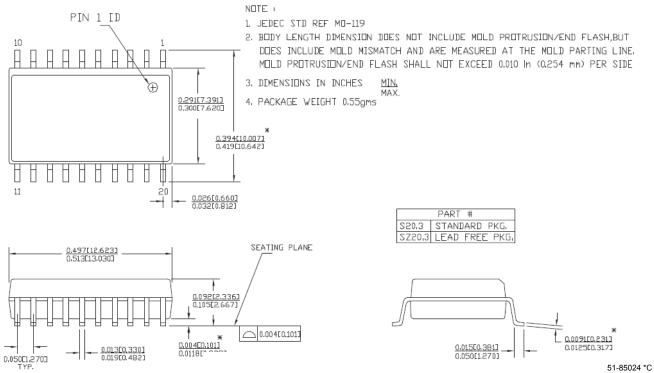
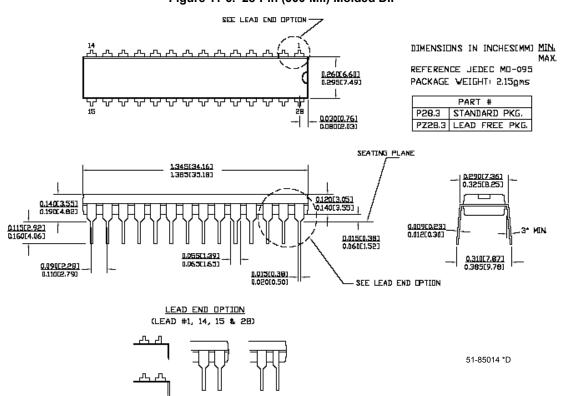


Figure 11-6. 28-Pin (300-Mil) Molded DIP

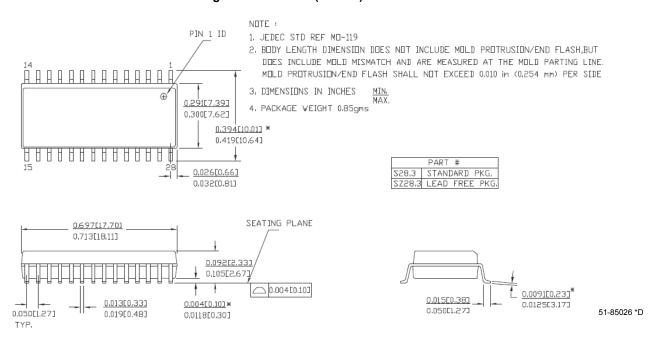


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Figure 11-7. 28-Pin (210-Mil) SSOP

Figure 11-8. 28-Pin (300-Mil) Molded SOIC





SIDE VIEW TOP VIEW ☐ 0.05 C BOTTOM VIEW 0.93 MAX--0.05 MAX 4.65 4.85 -0.20 REF 3.50 -0.50 DIA 0.80 MAX-0.23±0.05 3.50 0.30 - 0.500.42±0.18 [4X] [C]-

Figure 11-9. 32-Pin (5x5 mm) QFN

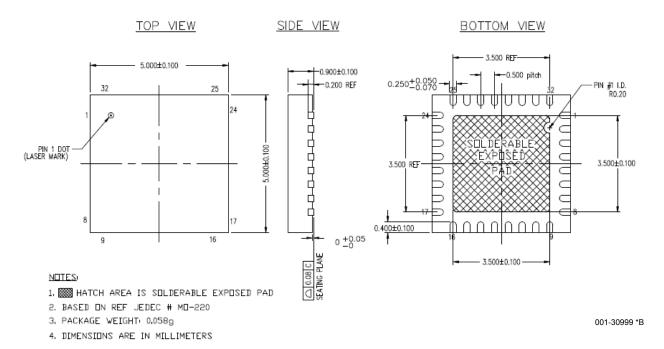
NOTES:

- 1. I HATCH AREA IS SOLDERABLE EXPOSED PAD.
- 2. REFERENCE JEDEC#: MO-220
- 3. PACKAGE WEIGHT: 0.054g
- 4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
- 5. PACKAGE CODE

PART#	DESCRIPTION
LF32	STANDARD
LY32	PB-FREE

51-85188 *C

Figure 11-10. 32-Pin Sawn QFN Package

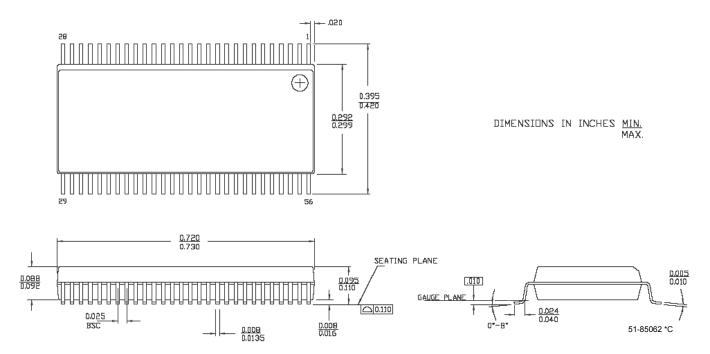


Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

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Figure 11-11. 56-Pin (300-Mil) SSOP





11.1 Thermal Impedances

Table 11-1. Thermal Impedances per Package

Package	Typical θ _{JA} ^[26]
8 PDIP	123°C/W
8 SOIC	185°C/W
20 PDIP	109°C/W
20 SSOP	117 °C/W
20 SOIC	81°C/W
28 PDIP	69 °C/W
28 SSOP	101°C/W
28 SOIC	74 °C/W
32 QFN	22°C/W

11.2 Capacitance on Crystal Pins

Table 11-2. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8 PDIP	2.8 pF
8 SOIC	2.0 pF
20 PDIP	3.0 pF
20 SSOP	2.6 pF
20 SOIC	2.5 pF
28 PDIP	3.5 pF
28 SSOP	2.8 pF
28 SOIC	2.7 pF
32 QFN	2.0 pF

11.3 Solder Reflow Peak Temperature

The following table lists the minimum solder reflow peak temperatures to achieve good solderability.

Table 11-3. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature ^[27]	Maximum Peak Temperature
8 PDIP	240°C	260°C
8 SOIC	240°C	260°C
20 PDIP	240°C	260°C
20 SSOP	240°C	260°C
20 SOIC	220°C	260°C
28 PDIP	240°C	260°C
28 SSOP	240°C	260°C
28 SOIC	220°C	260°C
32 QFN	240°C	260°C

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 $[\]begin{array}{l} \textbf{Notes} \\ \textbf{26.} \ \textbf{T}_{\textbf{J}} = \textbf{T}_{\textbf{A}} + \textbf{POWER} \ \textbf{x} \ \boldsymbol{\theta}_{\textbf{JA}} \end{array}$

^{27.} Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.



12. Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C24x23A family.

12.1 Software

12.1.1 PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at

http://www.cypress.com/psocdesigner and includes a free C compiler.

12.1.2 PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free ofcharge at http://www.cypress.com/psocprogrammer.

12.2 Development Kits

All development kits can be purchased from the Cypress Online Store.

12.2.1 CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

12.3 Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

12.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

12.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

12.3.3 CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack



12.4 Device Programmers

All device programmers can be purchased from the Cypress Online Store.

12.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

12.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

12.5 Accessories (Emulation and Programming)

Table 12-1. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit ^[28]	Foot Kit ^[29]	Adapter ^[30]
All non-QFN	All non QFN	CY3250-24X23A	CY3250-8DIP-FK, CY3250-8SOIC-FK, CY3250-20DIP-FK, CY3250-20SOIC-FK, CY3250-20SSOP-FK, CY3250-28DIP-FK, CY3250-28SOIC-FK, CY3250-28SOP-FK	Adapters can be found at http://www.emulation.com.
CY8C24423A-24LFXI	32 QFN	CY3250-24X23AQFN	CY3250-32QFN-FK	

12.6 Third Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

12.7 Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see application note AN2323 "Debugging - Build a PSoC Emulator into Your Board".

Notes

- 28. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
- 29. Foot kit includes surface mount feet that can be soldered to the target PCB.
- 30. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

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13. Ordering Information

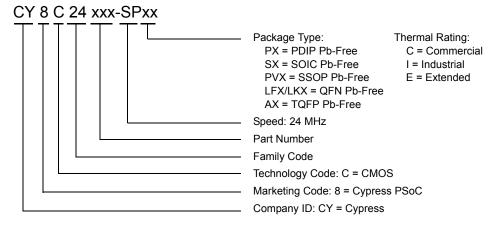
The following table lists the CY8C24x23A PSoC device's key package features and ordering codes.

Table 13-1. CY8C24x23A PSoC Device Key Features and Ordering Information

					1						
Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
8 Pin (300 Mil) DIP	CY8C24123A-24PXI	4K	256	No	-40C to +85C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC	CY8C24123A-24SXI	4K	256	No	-40C to +85C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC (Tape and Reel)	CY8C24123A-24SXIT	4K	256	No	-40C to +85C	4	6	6	4	2	No
20 Pin (300 Mil) DIP	CY8C24223A-24PXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP	CY8C24223A-24PVXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24223A-24PVXIT	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC	CY8C24223A-24SXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24223A-24SXIT	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
28 Pin (300 Mil) DIP	CY8C24423A-24PXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP	CY8C24423A-24PVXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24423A-24PVXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC	CY8C24423A-24SXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24423A-24SXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm) QFN	CY8C24423A-24LFXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm 1.00 MAX) SAWN QFN	CY8C24423A-24LTXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm 1.00 MAX) SAWN QFN (Tape and Reel)	CY8C24423A-24LTXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
56 Pin OCD SSOP	CY8C24000A-24PVXI ^[31]	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

13.1 Ordering Code Definitions



Note

31. This part may be used for in-circuit debugging. It is NOT available for production

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14. Document History Page

	Document Title: CY8C24123A, CY8C24223A, CY8C24423A PSoC® Programmable System-on-Chip Document Number: 38-12028						
Rev.	ECN	Orig. of Change	Submission Date	Description of Change			
**	236409	SFV	See ECN	New silicon and new document – Preliminary Data Sheet.			
*A	247589	SFV	See ECN	Changed the title to read "Final" data sheet. Updated Electrical Specifications chapter.			
*B	261711	HMT	See ECN	Input all SFV memo changes. Updated Electrical Specifications chapter.			
*C	279731	НМТ	See ECN	Update Electrical Specifications chapter, including 2.7 VIL DC GPIO spec. Add Solder Reflow Peak Temperature table. Clean up pinouts and fine tune wording and format throughout.			
*D	352614	НМТ	See ECN	Add new color and CY logo. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications. Re-add ISSP pinout identifier. Delete Electrical Specification sentence re: devices running at greater than 12 MHz. Update Solder Reflow Peak Temperature table. Fix CY.com URLs. Update CY copyright.			
*E	424036	НМТ	See ECN	Fix SMP 8-pin SOIC error in Feature and Order table. Update 32-pin QFN E-Pad dimensions and rev. *A. Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Add OCD non-production pinout and package diagram. Update CY branding and QFN convention. Update package diagram revisions.			
*F	521439	НМТ	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table.			
*G	2256806	UVS/PYRS	See ECN	Added Sawn pin information.			
*H	2425586	DSO/AESA	See ECN	Corrected Ordering Information to include CY8C24423A-24LTXI and CY8C24423A-24LTXIT			
*	2619935	OGNE/AESA	12/11/2008	Changed title to "CY8C24123A, CY8C24223A, CY8C24423A PSoC [®] Programmable System-on-Chip™" Updated package diagram 001-30999 to *A. Added note on digital signaling in DC Analog Reference Specifications on page 28. Added Die Sales information note to Ordering Information on page 54.			
*J	2692871	DPT/PYRS	04/16/2009	Updated Max package thickness for 32-pin QFN package Formatted Notes Updated "Getting Started" on page 4 Updated "Development Tools" on page 5 and "Designing with PSoC Designer" on page 6			
*K	2762168	JVY/AESA	06/25/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 and TWRITE specifications. Replaced T _{RAMP} (time) specification with SR _{POWER_UP} (slew rate) specification. Added note [9] to Flash Endurance specification. Added IOH, IOL, DC _{ILO} , F _{32K_U} , T _{POWERUP} T _{ERASEALL} , T _{PROGRAM_HOT} , and T _{PROGRAM_COLD} specifications.			

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15. Sales, Solutions, and Legal Information

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