AT91SAM7L-EK Evaluation Board

User Guide

6370A–ATARM–15-Feb-08

Table of Contents

Section 1

Overview

1.1 Scope

The AT91SAM7L-EK evaluation kit enables the evaluation of and code development of applications running on an AT91SAM7L device.

The kit consists of two boards which can be connected together:

- The Handheld Board (hereafter referred to as HB) and
- The Docking Board (hereafter referred to as DB)

These two boards must be connected together in debug or programming mode.

This guide focuses on the AT91SAM7L-EK board as an evaluation platform.

1.2 Deliverables

The AT91SAM7L-EK package contains the following items:

- One Handheld Board
- One Docking Board
- One Universal input AC/DC power supply with US, UK and European plug adapters
- One RS232 crossed serial cable
- One AT91SAM7L-EK dedicated CD-ROM

1.3 The AT91SAM7L-EK Evaluation Board

1.3.1 Handheld Board

The handheld board is equipped with an AT91SAM7L128 (128-lead LQFP package) together with the following:

- 400-segment LCD Display
- 35-key Keyboard (7x5 matrix)
- Two AAA battery clip socket
- IrDA® transceiver
- Weather Station Capabilities (Temperature/Pressure sensor)
- SPI DataFlash® SD/MMC Card connector
- ZIGBEE expansion connector (optional RZ502 board)
- VCC level monitor

- Force Wake-up push button
- Reset push button
- Configuration Jumpers

1.3.2 Docking Board

The docking board is equipped with I/O expansion connectors and Debug devices:

- 5-Volt DC power supply input
- Yellow Power Supply LED (software controlled)
- Two Green User LEDs
- JTAG/ICE interface
- HE10 ADC connector (4 inputs)
- Three expansion connectors (PIO A, PIO B, PIO C)

Section 2

Setting Up the AT91SAM7L-EK Board

2.1 Electrostatic Warning

The AT91SAM7L-EK evaluation board is shipped in protective anti-static packaging. The board must not be exposed to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM7L-EK evaluation board, the following items are needed:

- The AT91SAM7L-EK evaluation board itself
- AC/DC power adapter (5V at 2A), 2.1 mm x 5.5 mm
- An DS732 crossed cable and/or a JTAG/ICE interface depending on the kind of development projects to be done.

2.3 Layout

Figure 2-1. AT91SAM7L-EK Layout -Top View

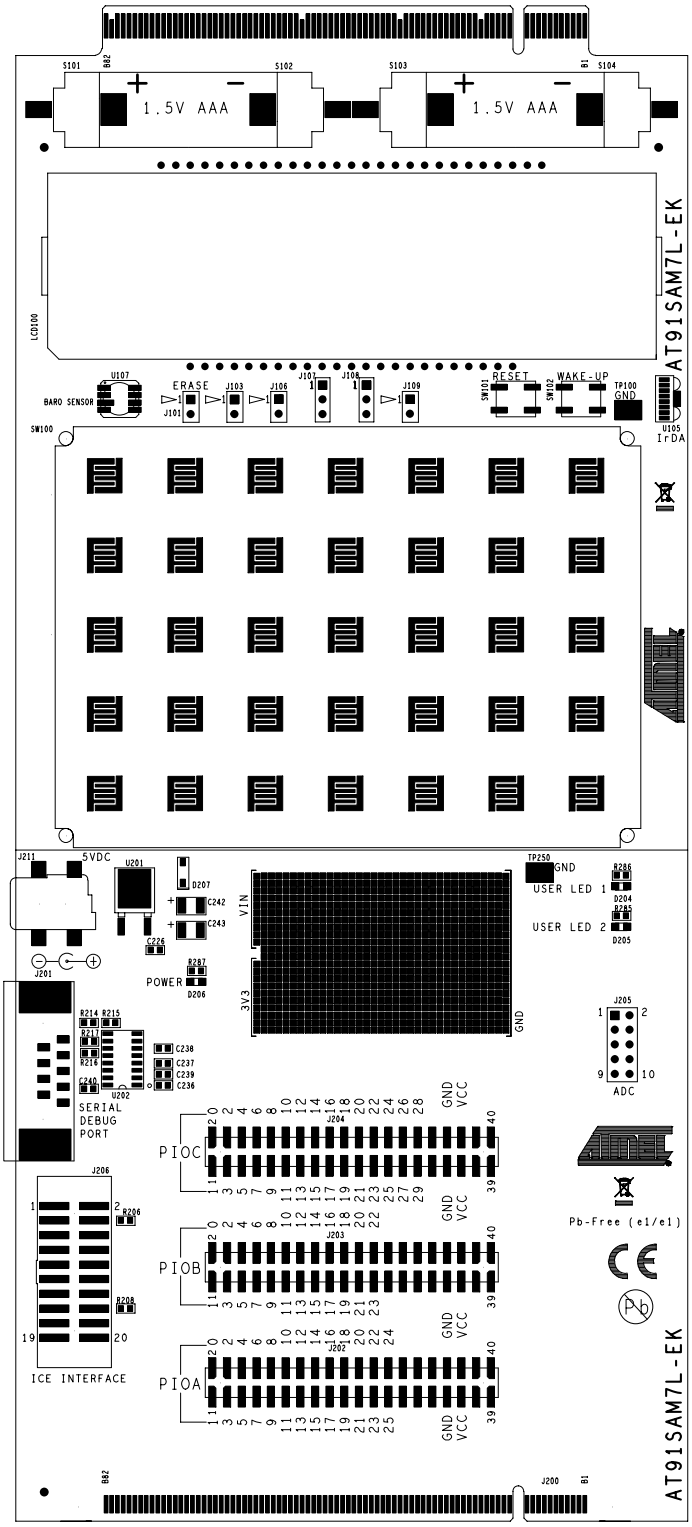
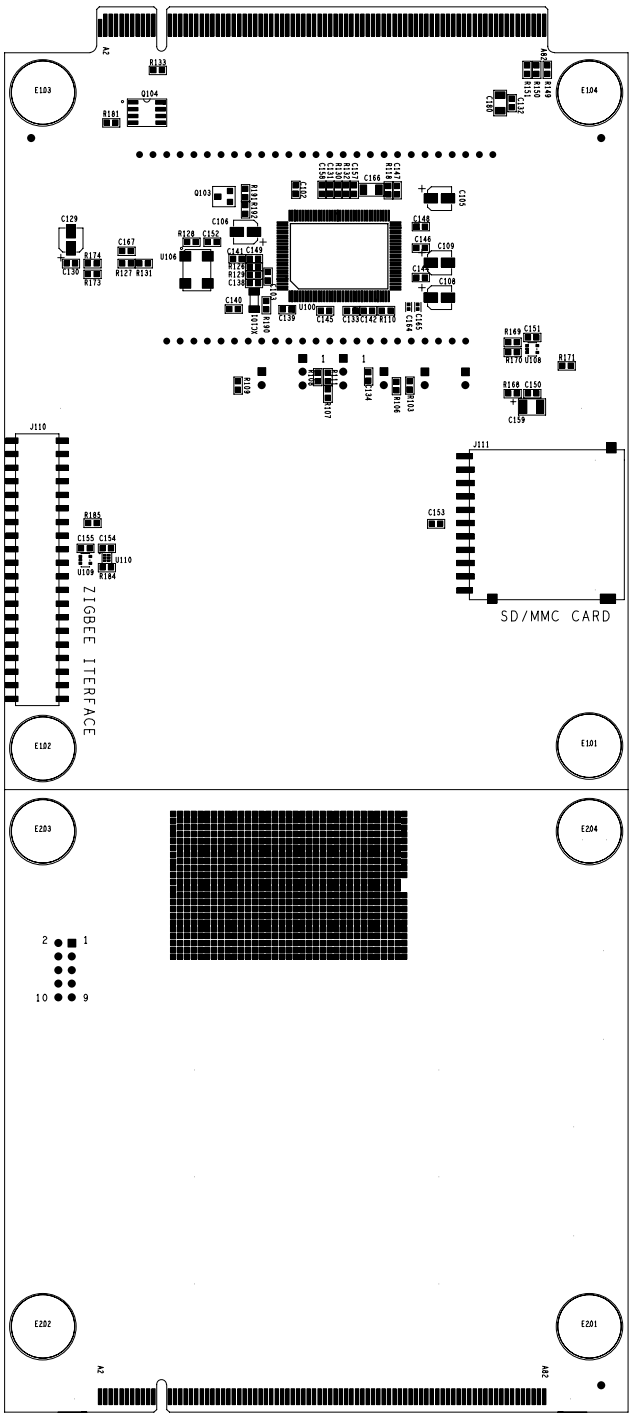


Figure 2-2. AT91SAM7L-EK Layout - Bottom View



2.4 Powering Up the Board

The AT91SAM7L-EK requires 5V DC (± 5%). DC power is supplied to the board via the 2.1 mm x 5.5 mm socket J211. Coaxial plug center positive standard.

2.5 Handheld Board in Stand-alone Mode

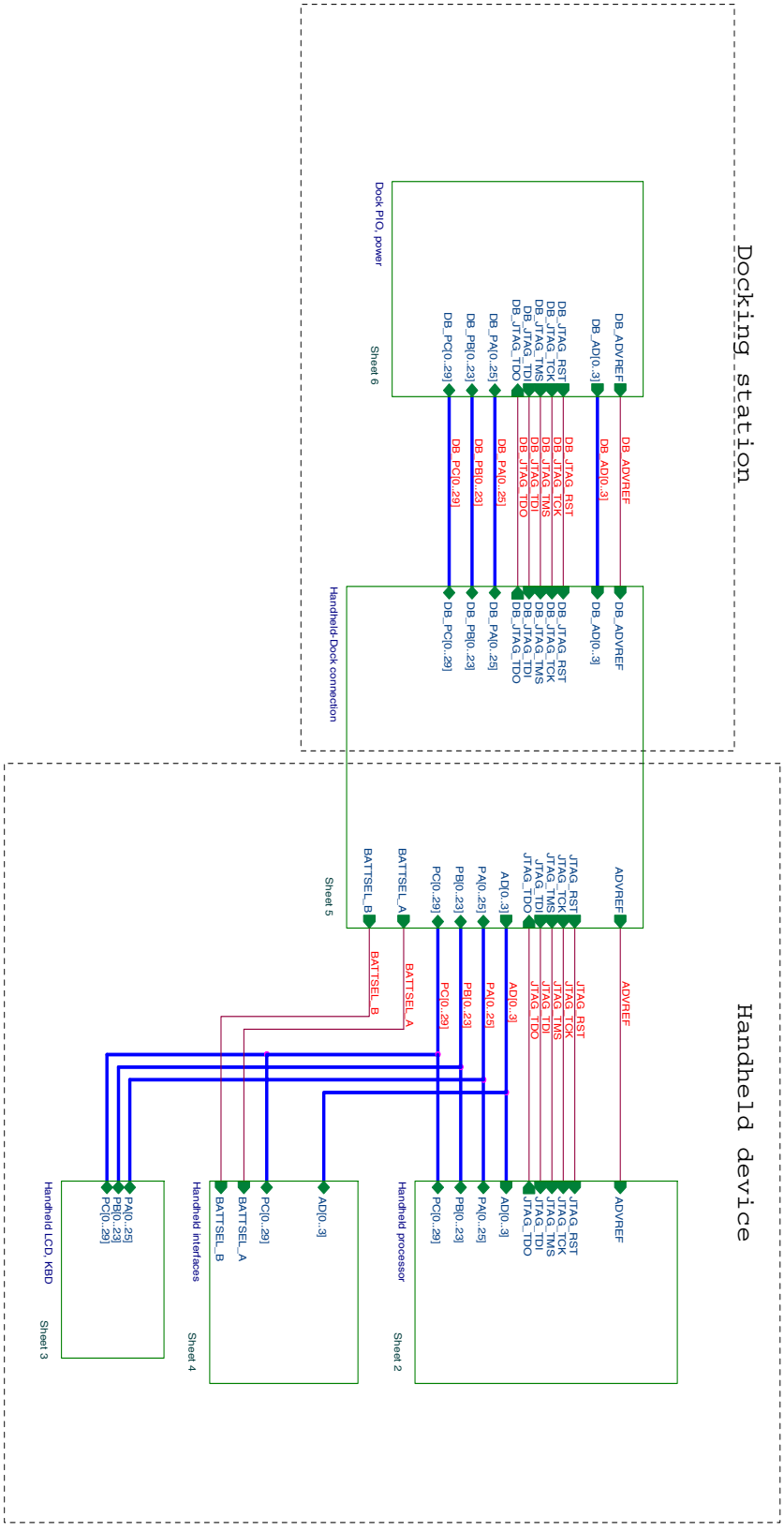
The user has the possibility to fit 2 x 1.5V AAA battery cells in the handheld board clip sockets in order to use the HB in stand-alone mode (application software programmed in the AT91SAM7L microcontroller embedded flash).

2.6 Getting Started

The AT91SAM7L-EK evaluation kit is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this CD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM7L-EK.

2.7 AT91SAM7L-EK Block Diagram

Figure 2-3. AT91SAM7L-EK Block Diagram



Section 3

Board Description

The following paragraphs list the features available on the AT91SAM7L-EK and onto which board a particular feature has been fitted:

- The Handheld Board (HB)
- The Docking Board (DB)

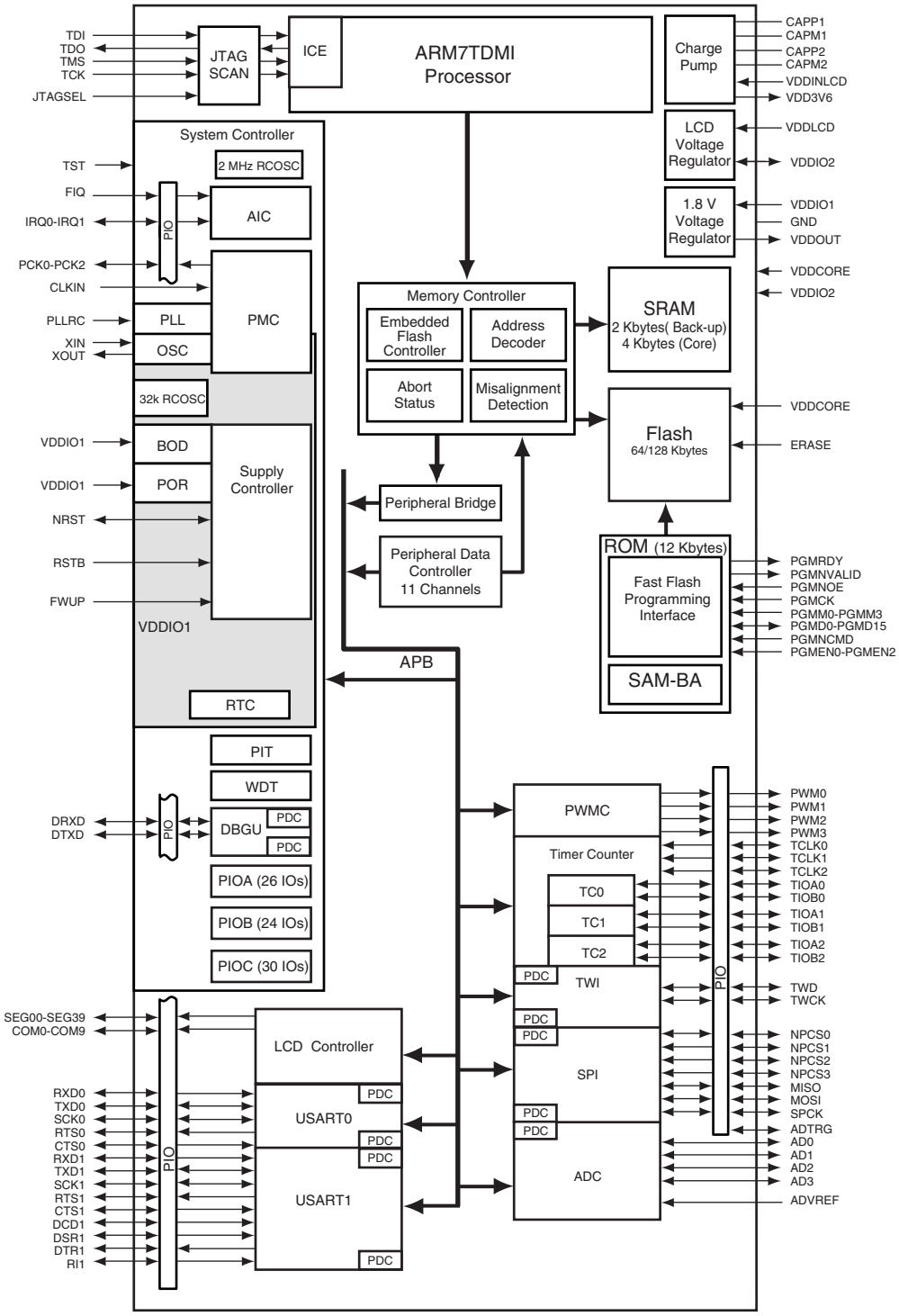
3.1 AT91SAM7L Microcontroller

- **Incorporates the ARM7TDMI® ARM® Thumb® Processor**
  - **High-performance 32-bit RISC Architecture**
  - **High-density 16-bit Instruction Set**
  - **Leader in MIPS/Watt**
  - **EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support**
- **Internal High-speed Flash**
  - **128 Kbytes (AT91SAM7L128), Organized in 512 Pages of 256 Bytes Single Plane**
  - **64 Kbytes (AT91SAM7L64), Organized In 256 Pages of 256 Bytes Single Plane**
  - **Single Cycle Access at Up to 15 MHz in Worst Case Conditions**
  - **128-bit Read Access**
  - **Page Programming Time: 4.6 ms, Including Page Auto Erase, Full Erase Time: 10 ms**
  - **10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit**
  - **Fast Flash Programming Interface for High Volume Production**
- **Enhanced Embedded Flash Controller (EEFC)**
  - **Interface of the Flash Block with the 32-bit Internal Bus**
  - **Increases Performance in ARM and Thumb Mode with 128-bit Wide Memory Interface**
- **Internal High-speed SRAM, Single-cycle Access at Maximum Speed**
  - **6 kbytes**
    - **2 Kbytes Directly on Main Supply That Can Be Used as Backup SRAM**
    - **4 Kbytes in the Core**
- **Memory Controller (MC)**
  - **Enhanced Embedded Flash Controller, Abort Status and Misalignment Detection**
- **Reset Controller (RSTC)**
  - **Based on Brownout Reset and Low-power Factory-calibrated Brownout Detector**
  - **Provides External Reset Signal Shaping and Reset Source Status**
- **Clock Generator (CKGR)**
  - **Low-power 32 kHz RC Oscillator, 32 kHz On-chip Oscillator, 2 MHz Fast RC Oscillator and one PLL**
- **Supply Controller (SUPC)**
  - **Minimizes Device Power Consumption**
  - **Manages the Different Supplies On Chip**
  - **Supports Multiple Wake-up Sources**
- **Power Management Controller (PMC)**
  - **Software Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode**
  - **Three Programmable External Clock Signals**
  - **Handles Fast Start Up**

- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - Two-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
  - 12-bit Key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter may be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Clock (RTC)
  - Two Hundred Year Calendar with Alarm
  - Runs Off the Internal RC or Crystal Oscillator
- Three Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - Eighty Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Eleven Peripheral DMA Controller (PDC) Channels
- One Segmented LCD Controller
  - Display Capacity of Forty Segments and Ten Common Terminals
  - Software Selectable LCD Output Voltage (Contrast)
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Manchester Encoder/Decoder
  - Full Modem Line Support on USART1
- One Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master, Multi-Master and Slave Mode Support, All Atmel® Two-wire EEPROMs and I^2C compatible Devices Supported
  - General Call Supported in Slave Mode
- One 4-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA® Boot Assistant
  - Default Boot Program
  - Interface with SAM-BA Graphic User Interface
  - In Application Programming Function (IAP)
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- I/Os, including Four High-current Drive I/O lines, Up to 4 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 60 mA for the Core with Programmable Output Voltage
  - Single Supply 1.8V - 3.6V
  - Zero-power Power-on Reset and Brownout Detector, Fully Programmable
- Fully Static Operation: Up to 36 MHz at 85°C
- Available in a 128-lead LQFP Green and a 144-ball LFBGA Green Package

3.2 AT91SAM7L Block Diagram

Figure 3-1. AT91SAM7L BLock Diagram



3.3 Memory

- 128 Kbytes of Internal Flash (HB)
- 6 KBytes Internal High Speed SRAM (HB)

3.4 Clock Circuitry

- 32.768KHz standard crystal for the embedded oscillator (HB)
- Internal RC Oscillator (HB)

3.5 Reset Circuitry

- Internal Reset Controller with a bi-directional reset pin (HB)
- External reset push button (HB)

3.6 Supply Controller

- Programmable Supply Controller (HB)
- Force Wake-Up Push Button (HB)

3.7 Power Supply Circuitry

- Embedded 1.8V regulator (Drawing up to 60 mA for the Core) (HB)
- On board 2 x 1.5V AAA type battery cells (not delivered in the kit) (HB)
- On board 3.3V linear regulator (DB)
- One VCC/VBAT Power Supply Monitoring device (HB)

3.8 Remote Communication

- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket (DB)
- One IrDA transceiver (COM Port 0) (HB)

3.9 Analog Interface

- Four Analog Inputs up to ADVREF input (1.8V max) via one HE10 connector (DB)

3.10 User Interface

- One 35-key Keyboard (7x5 matrix) (HB)
- One 400-segment LCD Display (HB)
- One Temperature/Pressure Sensor (Weather Station Application) (HB)
- Two user's green LEDs (DB)
- One Yellow Power LED (software controlled) (DB)

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector (DB)
- DBGU COM Port (DB)

3.12 Expansion Slot

- One DataFlash, SD/MMC Card Slot (HB)
- One ZIGBEE interface connector (dedicated to an optional RZ502 board) (HB)
- All I/Os of the AT91SAM7L are routed to peripheral extension connectors (DB)

3.13 PIO Usage

- The following tables present the way the PIO lines multiplexing has been used on the AT91SAM7L-EK.

Table 3-1. PIOA Usage

I/O Line	Peripheral A	Peripheral B	Comments	Peripheral Usage		Powered By
PA0			COM0	LCD Display	COM0	VDDIO2
PA1			COM1	LCD Display	COM1	VDDIO2
PA2			COM2	LCD Display	COM2	VDDIO2
PA3			COM3	LCD Display	COM3	VDDIO2
PA4			COM4	LCD Display	COM4	VDDIO2
PA5			COM5	LCD Display	COM5	VDDIO2
PA6			SEG0	LCD Display	SEG0	VDDIO2
PA7			SEG1	LCD Display	SEG1	VDDIO2
PA8			SEG2	LCD Display	SEG2	VDDIO2
PA9			SEG3	LCD Display	SEG3	VDDIO2
PA10			SEG4	LCD Display	SEG4	VDDIO2
PA11			SEG5	LCD Display	SEG5	VDDIO2
PA12			SEG6	LCD Display	SEG6	VDDIO2
PA13			SEG7	LCD Display	SEG7	VDDIO2
PA14			SEG8	LCD Display	SEG8	VDDIO2
PA15			SEG9	LCD Display	SEG9	VDDIO2
PA16			SEG10	LCD Display	SEG10	VDDIO2
PA17			SEG11	LCD Display	SEG11	VDDIO2
PA18			SEG12	LCD Display	SEG12	VDDIO2
PA19			SEG13	LCD Display	SEG13	VDDIO2
PA20			SEG14	LCD Display	SEG14	VDDIO2
PA21			SEG15	LCD Display	SEG15	VDDIO2
PA22			SEG16	LCD Display	SEG16	VDDIO2

Table 3-1. PIOA Usage (Continued)

I/O Line	Peripheral A	Peripheral B	Comments	Peripheral Usage		Powered By
PA23			SEG17	LCD Display	SEG17	VDDI02
PA24			SEG18	LCD Display	SEG18	VDDI02
PA25			SEG19	LCD Display	SEG19	VDDI02

Table 3-2. PIOB Usage

I/O Line	Peripheral A	Peripheral B	Comments	Peripheral Usage		Powered by
PB0			SEG20	LCD Display	SEG20	VDDI02
PB1			SEG21	LCD Display	SEG21	VDDI02
PB2			SEG22	LCD Display	SEG22	VDDI02
PB3			SEG23	LCD Display	SEG23	VDDI02
PB4			SEG24	LCD Display	SEG24	VDDI02
PB5			SEG25	LCD Display	SEG25	VDDI02
PB6			SEG26	LCD Display	SEG26	VDDI02
PB7			SEG27	LCD Display	SEG27	VDDI02
PB8			SEG28	LCD Display	SEG28	VDDI02
PB9			SEG29	LCD Display	SEG29	VDDI02
PB10			SEG30	LCD Display	SEG30	VDDI02
PB11			SEG31	LCD Display	SEG31	VDDI02
PB12	NPCS3		SEG32	LCD Display	SEG32	VDDI02
PB13	NPCS2		SEG33	LCD Display	SEG33	VDDI02
PB14	NPCS1		SEG34	LCD Display	SEG34	VDDI02
PB15	RTS1		SEG35	LCD Display	SEG35	VDDI02
PB16	RTS0		SEG36	LCD Display	SEG36	VDDI02
PB17	DTR1		SEG37	LCD Display	SEG37	VDDI02
PB18	PWM0		SEG38	LCD Display	SEG38	VDDI02
PB19	PWM1		SEG39	LCD Display	SEG39	VDDI02
PB20	PWM2		COM6	LCD Display	COM6	VDDI02
PB21	PWM3		COM7	LCD Display	COM7	VDDI02
PB22	NPCS1	PCK1	COM8	LCD Display	COM8	VDDI02
PB23	PCK0	NPCS3	COM9	LCD Display	COM9	VDDI02

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Table 3-3. PIOC Usage

/O Line	Peripheral A	Peripheral B	Comments	Peripheral Usage		Powered by
PC0	CTS1	PWM2	WKUP0	Keypad	PC0 as Keypad ROW 0	VDDIO1
PC1	DCD1	TIOA2	WKUP1	Keypad	PC1 as Keypad ROW 1	VDDIO1
PC2	DTR1	TIOB2	WKUP2	Keypad	PC2 as Keypad ROW 2	VDDIO1
PC3	DSR1	TCLK1	WKUP3	Keypad	PC3 as Keypad ROW 3	VDDIO1
PC4	RI1	TCLK2	WKUP4	Keypad	PC4 as Keypad ROW 4	VDDIO1
PC5	IRQ1	NPCS2	WKUP5	ZIGBEE	IRQ1 with Wake-up Capability	VDDIO1
PC6	NPCS1	PCK2	WKUP6	ZIGBEE	NPCS1	VDDIO1
PC7	PWM0	TIOA0	High drive	Green User LED 1	PWM0	VDDIO1
PC8	PWM1	TIOB0	High drive	Green User LED 2/ZIGBEE (Shared PIO)	PWM1/PC8 as RSTN	VDDIO1
PC9	PWM2	SCK0	High drive	Yellow Power LED/ZIGBEE (Shared PIO)	PWM3/PC15 as SLP_TR	VDDIO1
PC10	TWD	NPCS3	High drive	Keypad	PC10 as Keypad COL 0	VDDIO1
PC11	TWCK	TCLK0	WKUP7	Keypad	PC11 as Keypad COL 1	VDDIO1
PC12	RXD0	NPCS3	WKUP8	IrDA RXD	RXD0	VDDIO1
PC13	TXD0	PCK0	WKUP9	IrDA TXD	TXD0	VDDIO1
PC14	RTS0	ADTRG	WKUP10	IrDA SD	PC14	VDDIO1
PC15	CTS0	PWM3	WKUP11	VCCSAMP (VCC Sample for Measure)	PC15 as VCCSAMP	VDDIO1
PC16	DRXD	NPCS1		Serial Debug Com Port	DRXD	VDDIO1
PC17	DTXD	NPCS2		Serial Debug Com Port	DTXD	VDDIO1
PC18	NPCS0	PWM0		Card Socket	NPCS0	VDDIO1
PC19	MISO	PWM1		Card Socket/Pressure Temperature Sensor/ZIGBEE	MISO	VDDIO1
PC20	MOSI	PWM2		Card Socket/Pressure Temperature Sensor/ZIGBEE	MOSI	VDDIO1
PC21	SPCK	PWM3		Card Socket/Pressure Temperature Sensor/ZIGBE	SPCK	VDDIO1
PC22	NPCS3	TIOA1		Pressure Temperature Sensor	NPCS3 (see AN510 INTERSEMA)	VDDIO1
PC23	PCK0	TIOB1		Pressure Temperature Sensor	PCK0	VDDIO1
PC24	RXD1	PCK1		Card Socket	PC24 as CARD DETECT	VDDIO1
PC25	TXD1	PCK2		Keypad	PC25 as Keypad COL 2	VDDIO1
PC26	RTS0	FIQ	WKUP12	Keypad	PC26 as Keypad COL 3	VDDIO1

Table 3-3. PIOC Usage (Continued)

/O Line	Peripheral A	Peripheral B	Comments	Peripheral Usage		Powered by
PC27	NPCS2	IRQ0	WKUP13	Keypad	PC27 as Keypad COL 4	VDDIO1
PC28	SCK1	PWM0	WKUP14	Keypad	PC28 as Keypad COL 5	VDDIO1
PC29	RTS1	PWM1	WKUP15	Keypad	PC29 as Keypad COL 6	VDDIO1

Section 4

Configuration

4.1 Configuration Jumpers

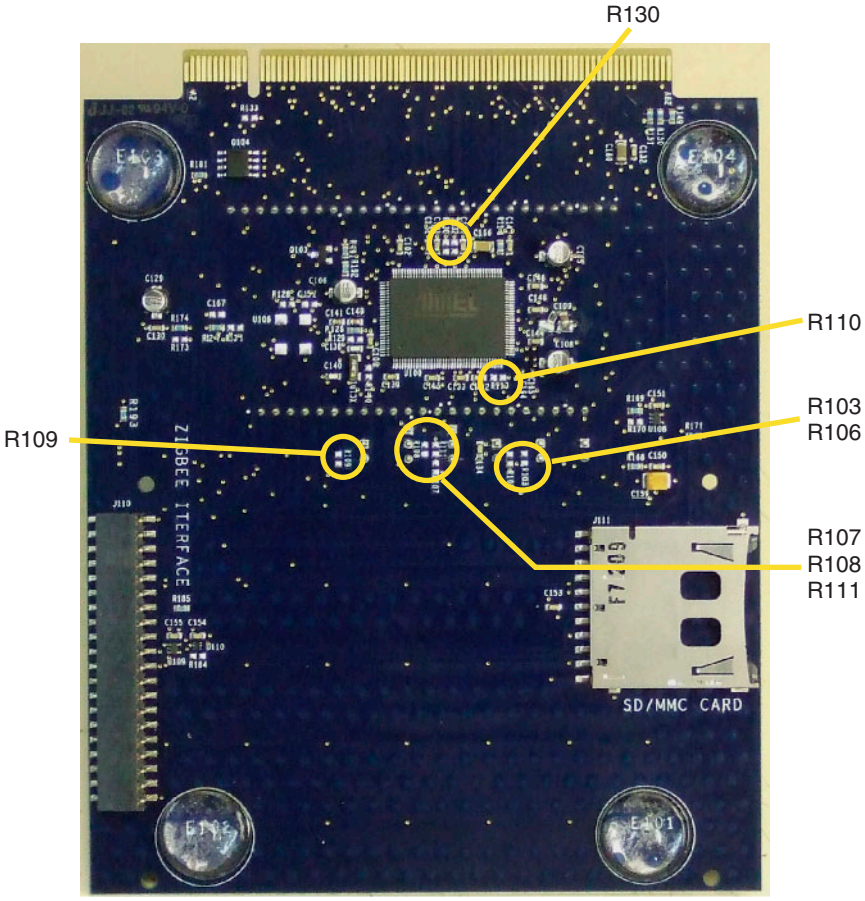
The configuration jumpers are all fitted on the handheld board.

Table 4-1. Configuration Jumper Settings (See Figure 4-1)

Designation	Default Setting	Feature
J101	Open	Erases all internal Flash memory and the NVM Configuration Bits when the board is powered. To do so, the user will have to close this for at least 220 ms.
J103	Closed	VDDCORE (Core Power Supply) Jumper (1)
J106	Closed	VDDIO1 (I/O Lines (PIOC) and Voltage Regulator Power Supply) Jumper (1)
J107	2 - 3	VDDINLCD (LCD Charge Pump Supply) Jumper Select 1 - 2: Powered by VCC (3.3V) 2 - 3: Not powered (connected to GND)
J108	2 - 3	VDDLCD (LCD Charge Pump Intermediate Voltage) Jumper Select 1 - 2: Powered by VDD3V6 (Output of the LCD Charge Pump) 2 - 3: Powered by VCC (3.3V)
J109	Closed	VDDIO2 (LCD I/O Lines Power Supply (PIOA and PIOB)/LCD Voltage Regulator Output) and VDDLCD (LCD Charge Pump Intermediate Voltage) Configuration Jumper • Closed: VDDIO2 and VDDLCD are powered by VCC (3.3V), the LCD Voltage Regulator is not used and in this case, J108 Jumper shall be put in 2 - 3 position. • Opened: the LCD Voltage Regulator is in use and provides VDDIO2. VDDLCD is provided by VDD3V6 or VCC, depending on J108 Configuration.

Note: 1. These jumpers are provided for use as power consumption measurement. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.

Figure 4-1. Jumper Location

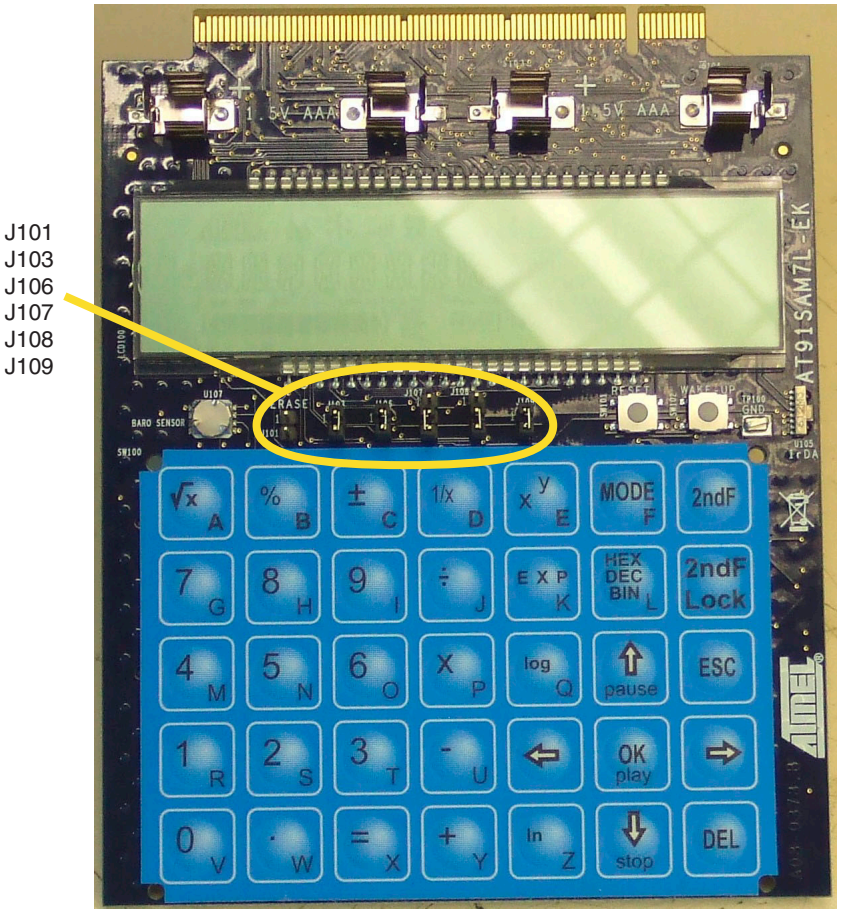


4.2 Configuration Straps on the Handheld Board

Table 4-2. Handheld Board Configuration Strap Settings (See Figure 4-2)

Designation	Default Setting	Feature
R130	Open	JTAGSEL Configuration: ICE Mode by Default, JTAG Mode if Soldered
R103	Open	Allows to strap J103: if fitted, connects permanently VDDCORE to VDDOUT
R106	Open	Allows to strap J106: if fitted, connects permanently VDDIO1 to VCC (3.3V)
R107	Open	Allows to strap J107 1 - 2 position: if fitted, connects permanently VDDINLCD to VCC (3.3V)
R108	Open	Allows to strap J108 1 - 2 position: if fitted, connects permanently VDDLCD to VDD3V6
R109	Open	Allows to strap J109: if fitted, connects permanently VDDLCD to VDDIO2
R110	Open	Allows to strap J108 2 - 3 position: if fitted, connects permanently VDDLCD to VCC (3.3V)
R111	Open	Allows to strap J107 2 - 3 position: if fitted, connects permanently VDDINLCD to GND
R184	Open	Allows to strap the U109/U110 device on the ZIGBEE INTERFACE. The configuration depends on the optional RZ502 board revision

Figure 4-2. Strap Location



4.3 Configuration Straps on the Docking Board

Table 4-3. Docking Board Configuration Straps

Designation	Default Setting	Feature
R208	Soldered	Enables the ICE NRST input by default (when soldered)

4.4 Miscellaneous Configuration

Table 4-4. Miscellaneous Configuration

Designation	Default Setting	Feature
TP100	N.A	GND Test point on the HB
TP250	N.A	GND Test point on the DB

4.5 Power Supply Schemes

The following figures illustrate the three typical power supply schematics of the AT91SAM7L related to J107, J108 and J109 jumper configurations.

Figure 4-3. The LCD Charge Pump supplies the LCD Voltage Regulator (J107 in 1 - 2 position, J108 in 1 - 2 position, J109 Opened)

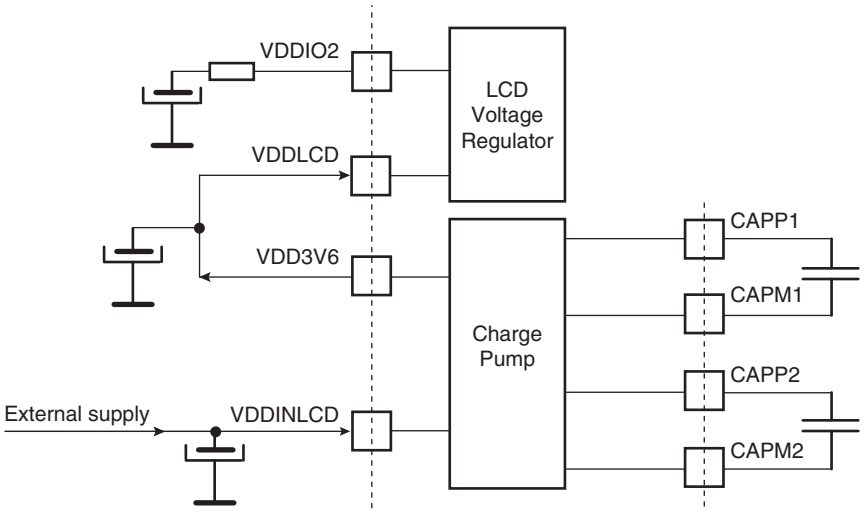


Figure 4-4. The LCD Voltage Regulator is externally supplied (J107 in 2 - 3 position, J108 in 2 - 3 position, J109 Opened)

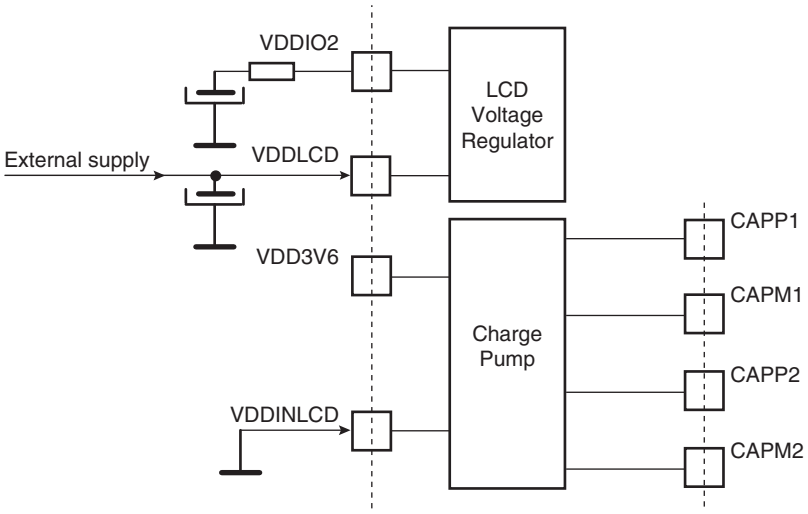
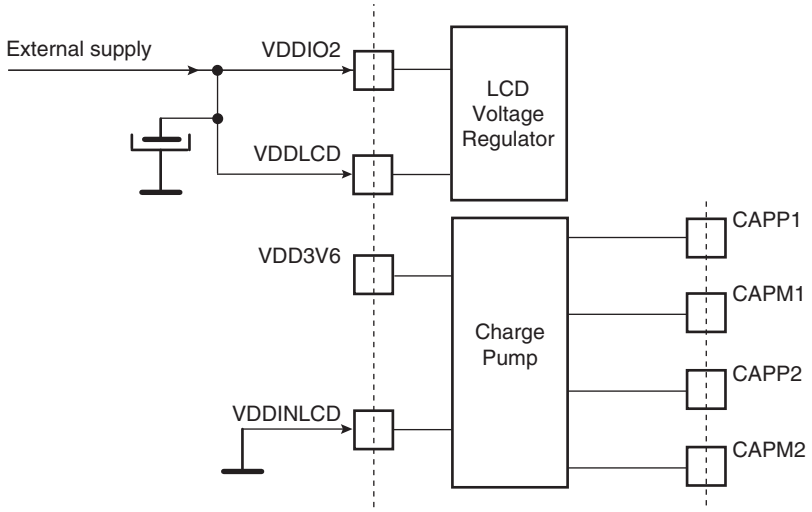


Figure 4-5. The LCD Charge Pump and the LCD Voltage Regulator are not used (J107 in 2 - 3 position, J108 in 2 - 3 position, J109 Closed, Default Configuration)



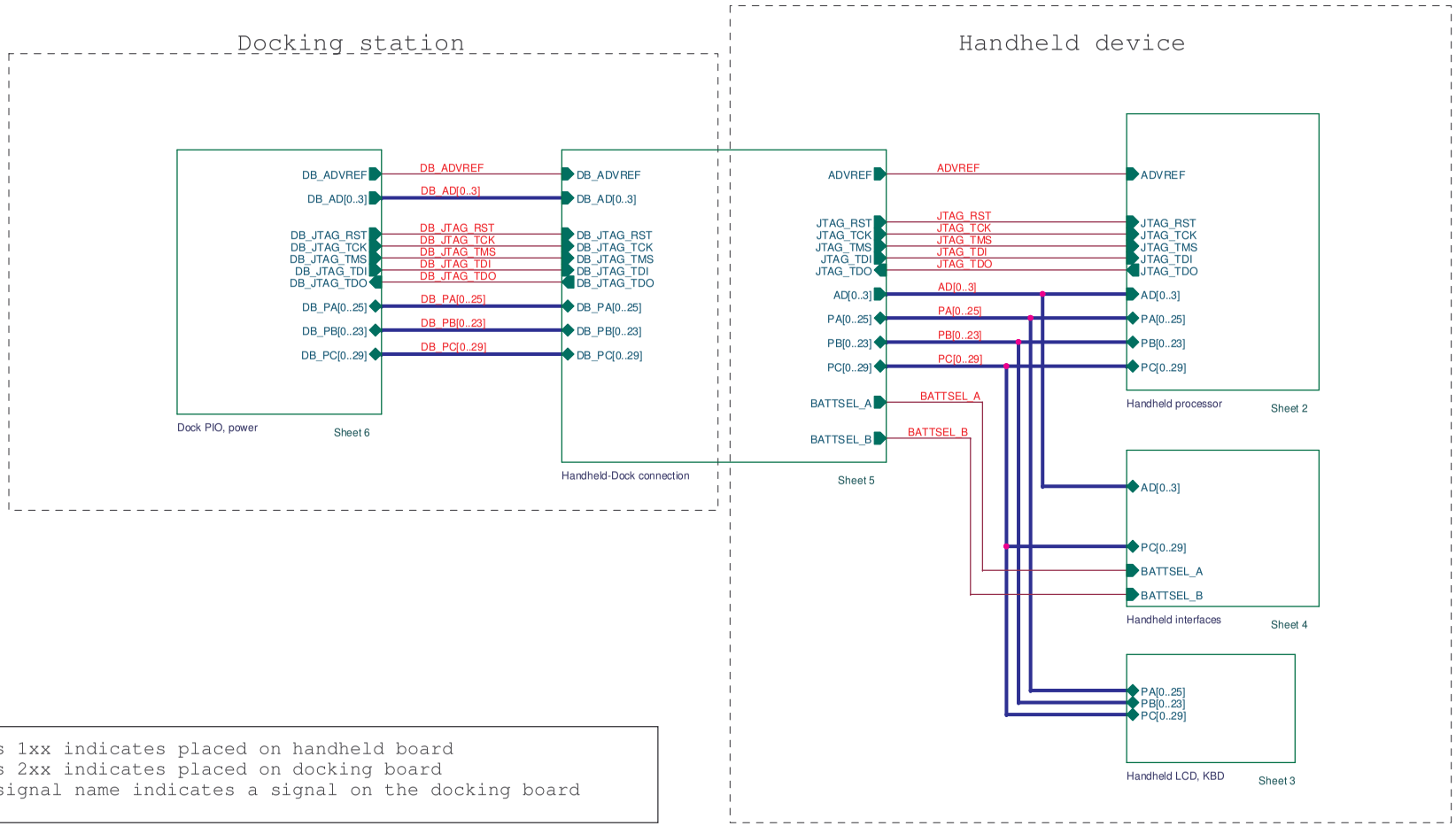
Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Top Level
- Handheld: Processor
- Handheld: LCD, KBD
- Handheld: Interfaces
- Handheld-dock Connection
- Dock: PIO, Power



Refdes 1xx indicates placed on handheld board
Refdes 2xx indicates placed on docking board
DB_x signal name indicates a signal on the docking board

Power symbols on handheld board

VCC HH_GND

Power symbols on docking board

DB_VCC DB_GND

REV	MODIF.	DES.	DATE	VER.	DATE
B	UPDATED	TMN	15-Nov-07	XXX	XX-XXX-XX
A	INIT EDIT	TMN	27-Aug-07	XXX	XX-XXX-XX

ATMEL ROUSSET

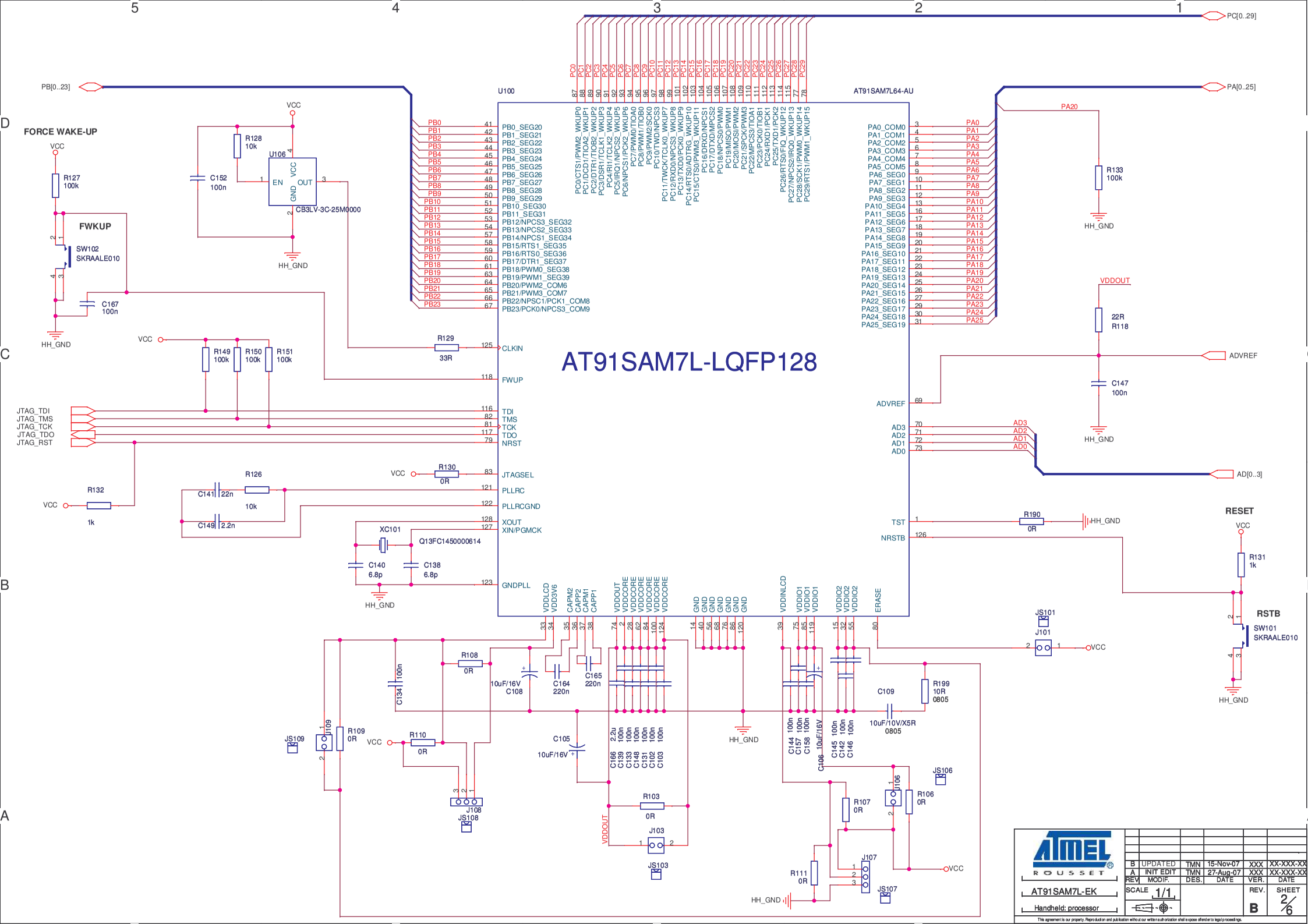
AT91SAM7L-EK

Top level

SCALE 1/1

REV. B

SHEET 1/6



REV	MODIF.	DES.	DATE	VER.	DATE
B	UPDATED	TMN	15-Nov-07	XXX	XX-XXX-XX
A	INIT EDIT	TMN	27-Aug-07	XXX	XX-XXX-XX

ATMEL ROUSSET

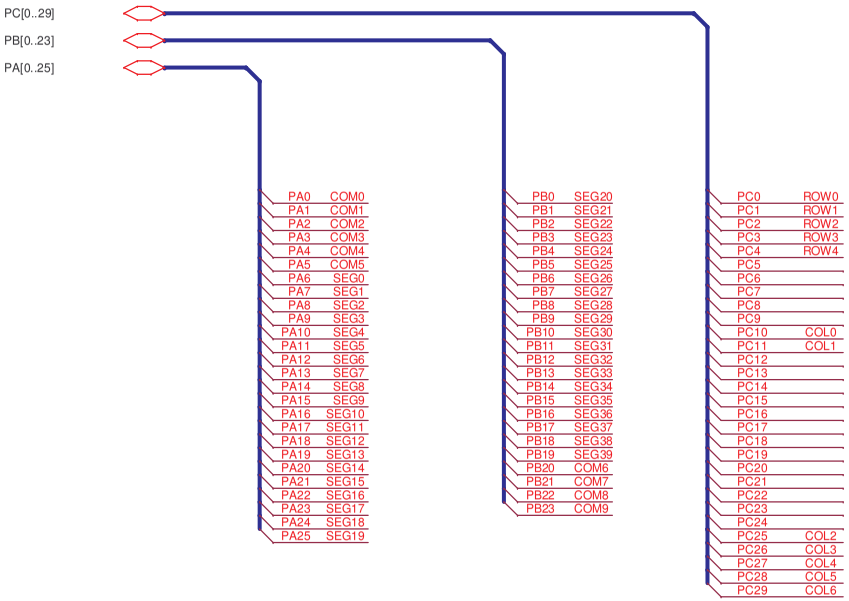
AT91SAM7L-EK

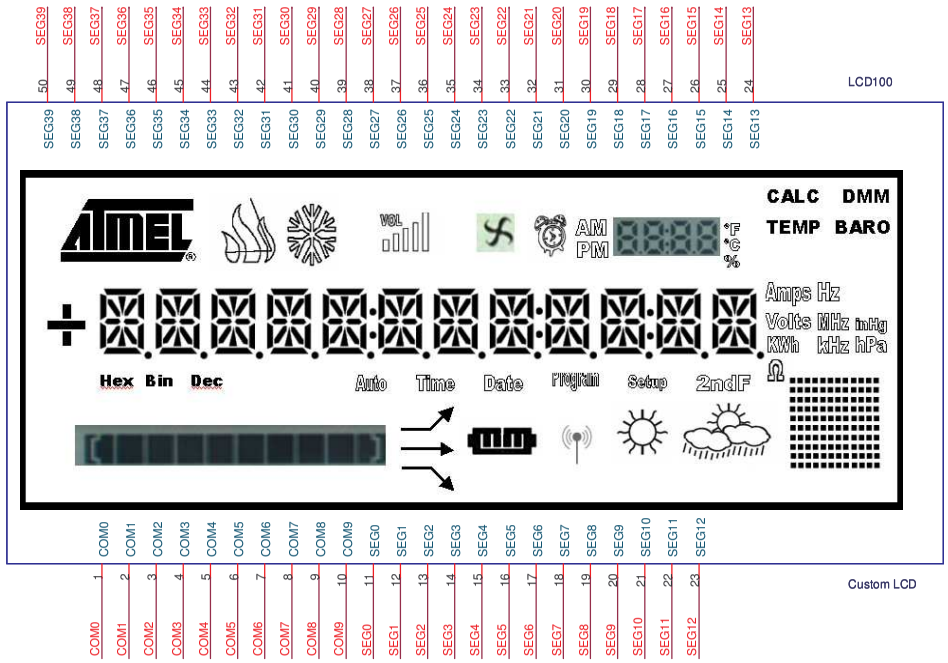
Handheld: processor

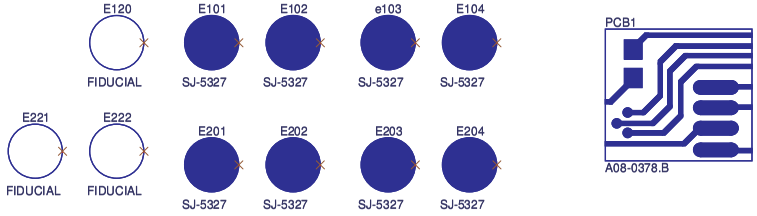
SCALE 1/1

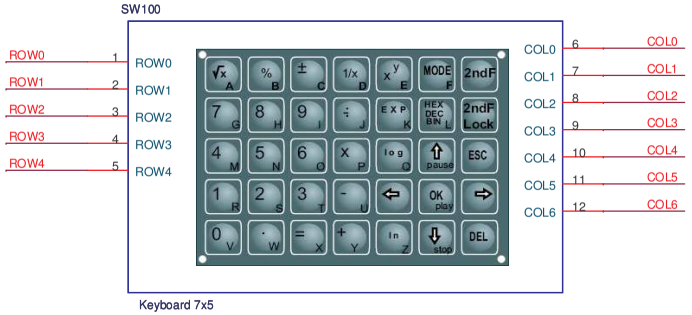
REV. B

SHEET 2/6









B	UPDATED	TMN	15-Nov-07	XXX	XX-XXX-XX
A	INIT EDIT	TMN	27-Aug-07	XXX	XX-XXX-XX
REV.	MODIF.	DES.	DATE	VER.	DATE

ROUSSET

AT91SAM7L-EK

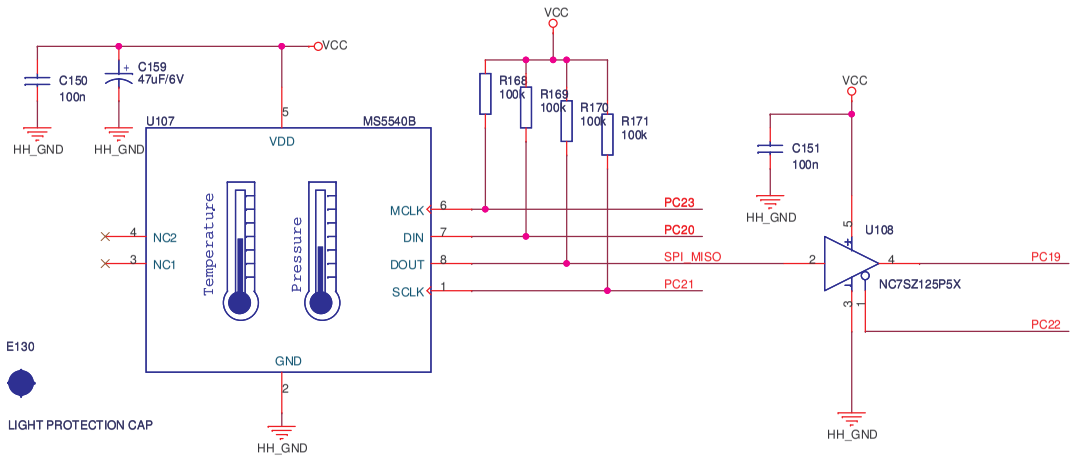
Handheld: LCD, KBD

SCALE 1/1

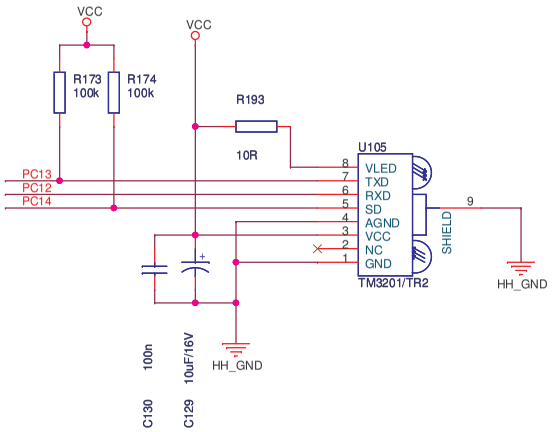
REV. B

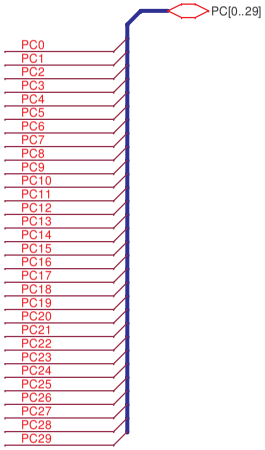
SHEET 3/6

WEATHER STATION
PRESSURE/TEMPERATURE SENSOR

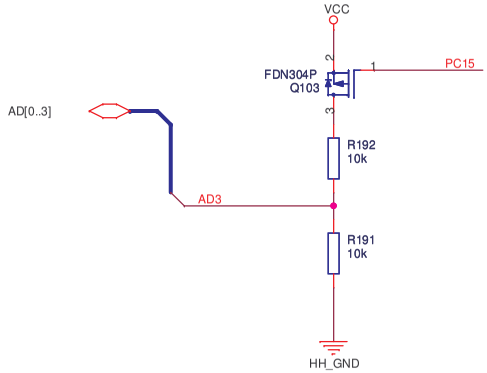


IrDA TRANSCEIVER

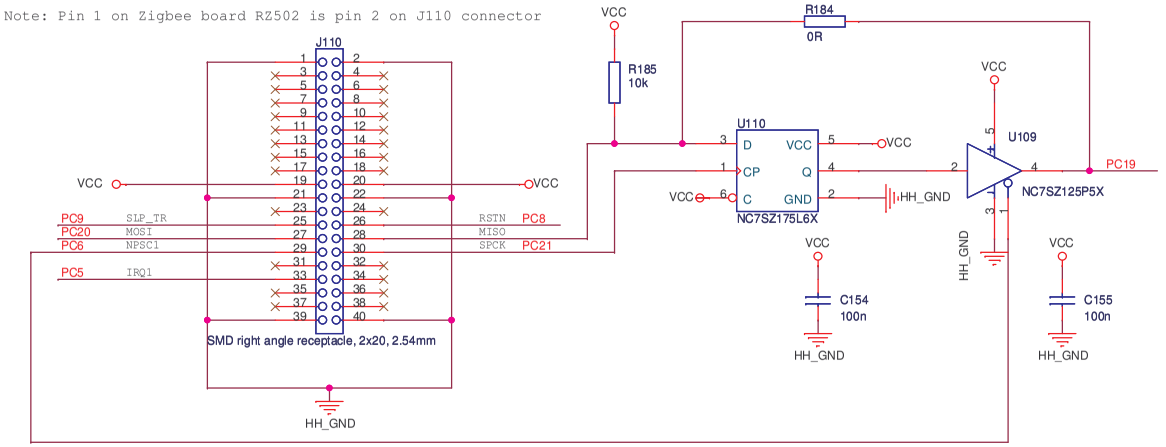




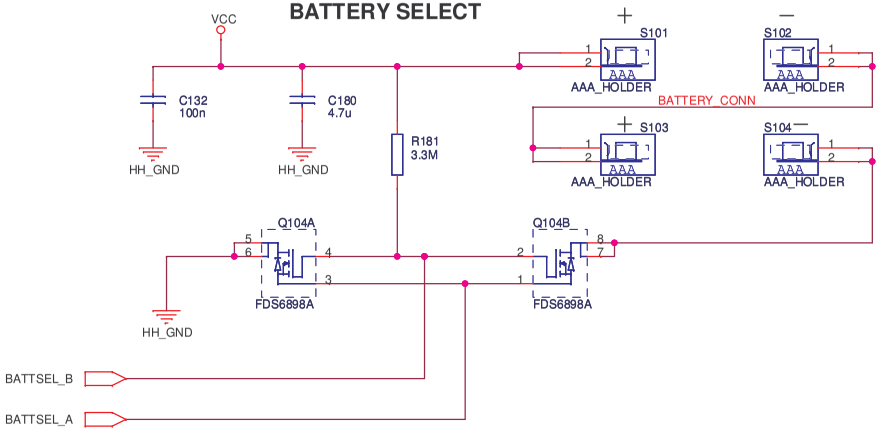
VCC/VBAT MONITOR



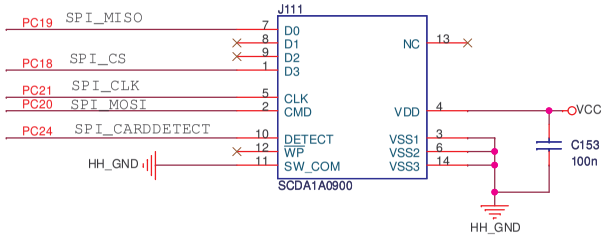
ZIGBEE INTERFACE



BATTERY SELECT



SD/MMC CARD



REV	MODIF.	DES.	DATE	VER.	DATE
B	UPDATED	TMN	15-Nov-07	XXX	XX-XXX-XX
A	INIT EDIT	TMN	27-Aug-07	XXX	XX-XXX-XX

AT91SAM7L-EK

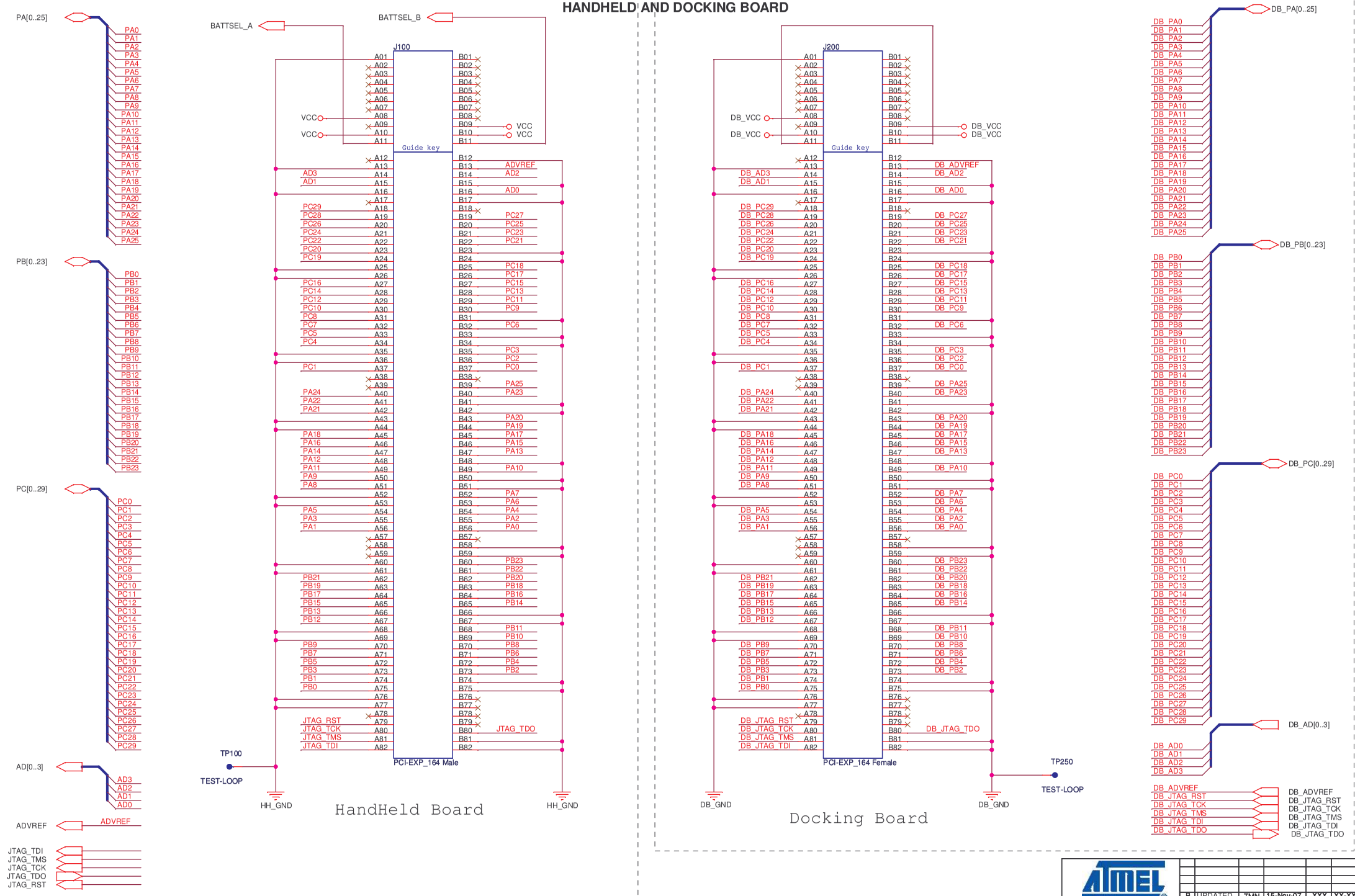
Handheld: interfaces

SCALE 1/1

REV. B

SHEET 4/6

PCI-STYLE CONNECTION BETWEEN HANDHELD AND DOCKING BOARD



REV	MODIF.	DES.	DATE	VER.	DATE
B	UPDATED	TMN	15-Nov-07	XXX	XX-XXX-XX
A	INIT EDIT	TMN	27-Aug-07	XXX	XX-XXX-XX

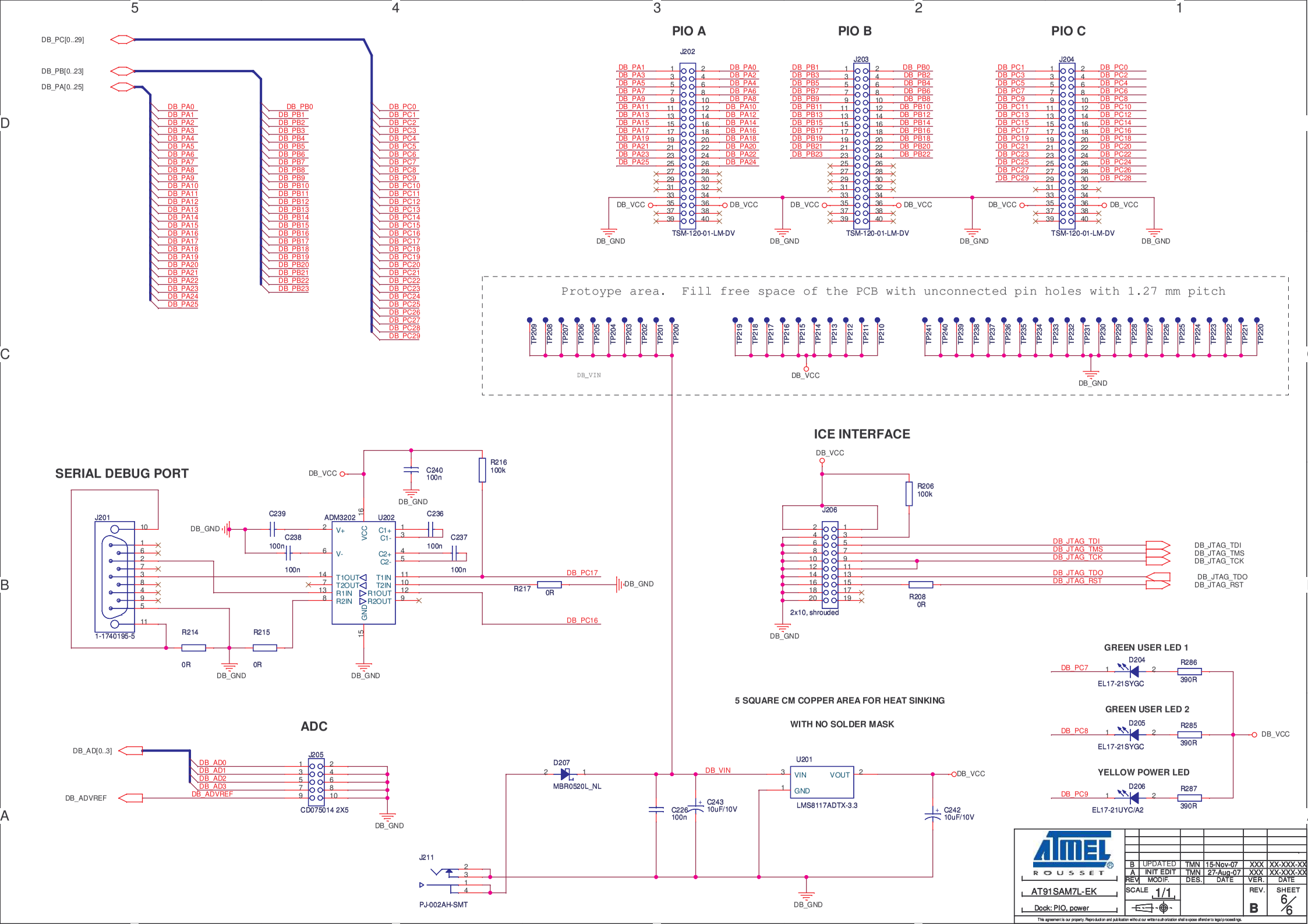
AT91SAM7L-EK

Handheld-Dock connection

SCALE 1/1

REV. B

SHEET 5/6


PIO A
PIO B
PIO C
J202
J203
J204
TSM-120-01-LM-DV
Protoype area. Fill free space of the PCB with unconnected pin holes with 1.27 mm pitch
SERIAL DEBUG PORT
ADM3202
U202
J201
1-1740195-5
ICE INTERFACE
J206
2x10, shrouded
ADC
J205
CD075014 2X5
5 SQUARE CM COPPER AREA FOR HEAT SINKING
WITH NO SOLDER MASK
U201
LMS8117ADTX-3.3
MBR0520L_NL
PJ-002AH-SMT
GREEN USER LED 1
GREEN USER LED 2
YELLOW POWER LED
EL17-21SYGC
EL17-21UYC/A2
AT91SAM7L-EK
Dock: PIO, power
ROUSSET
B UPDATED TMN 15-Nov-07 XXX XX-XXX-XX
A INIT EDIT TMN 27-Aug-07 XXX XX-XXX-XX
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. B
SHEET 6/6

Section 6

Errata

6.1 Optimal Operation

For optimal operation of the AT91SAM7L microcontroller within a standard application, please apply the following recommendations:

- Add a 100KΩ pulldown on CLKIN input (pin 125). Take care to place it very close to that pin.
- Change ADVREF load resistor (R118) value to 180.
- Add a 100KΩ pullup on PIO line PC22.

Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6370	First Issue	

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Atmel techincal support

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