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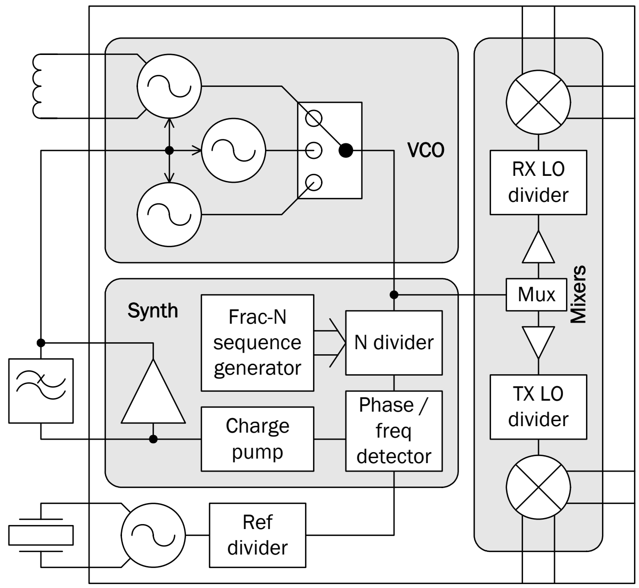
RF2051

HIGH PERFORMANCE WIDEBAND RF SYNTHESIZER/VCO WITH INTEGRATED RF MIXERS

RoHS Compliant and Pb-Free Product
Package: QFN, 32-Pin, 5mmx5mm



Functional Block Diagram

Features

- 30MHz to 2.5GHz Frequency Range
- Fractional-N Synthesizer
- Very Fine Frequency Resolution 1.5Hz for 26MHz Reference
- Low Phase Noise VCO
- Two High-Linearity RF Mixers
- Integrated LO Buffers
- Mixer Input IP3 +18dBm
- Mixer Bias Adjustable for Low Power Operation
- Full Duplex Mode
- 2.7V to 3.6V Power Supply
- Low Current Consumption 55mA to 75mA at 3V
- 3-Wire Serial Interface

Applications

- CATV Head-Ends
- Digital TV Up/Down Converters
- Digital TV Repeaters
- Multi-Dwelling Units
- Cellular Repeaters
- Frequency Band Shifters
- UHF/VHF Radios
- Diversity Receivers
- Software Defined Radios
- Satellite Communications
- Super-Heterodyne Radios

Product Description

The RF2051 is a low power, high performance, wideband RF frequency conversion chip with integrated local oscillator (LO) generation and a pair of RF mixers. The RF synthesizer includes an integrated fractional-N phase locked loop with voltage controlled oscillators (VCOs) and dividers to produce a low-phase noise LO signal with a very fine frequency resolution. The buffered LO output drives the built-in RF mixers which convert the signal into the required frequency band. The mixer bias current can be programmed dependent on the required performance and available supply current. The LO generation blocks have been designed to continuously cover the frequency range from 300MHz to 2400MHz. The RF mixers are very broad band and operate from 30MHz to 2500MHz at the input and output, enabling both up and down conversion. An external crystal of between 10MHz and 52MHz or an external reference source of between 10MHz and 104MHz can be used with the RF2051 to accommodate a variety of reference frequency options.

All on-chip registers are controlled through a simple three-wire serial interface. The RF2051 is designed for 2.7V to 3.6V operation for compatibility with portable, battery powered devices. It is available in a plastic 32-pin, 5mmx5mm QFN package.

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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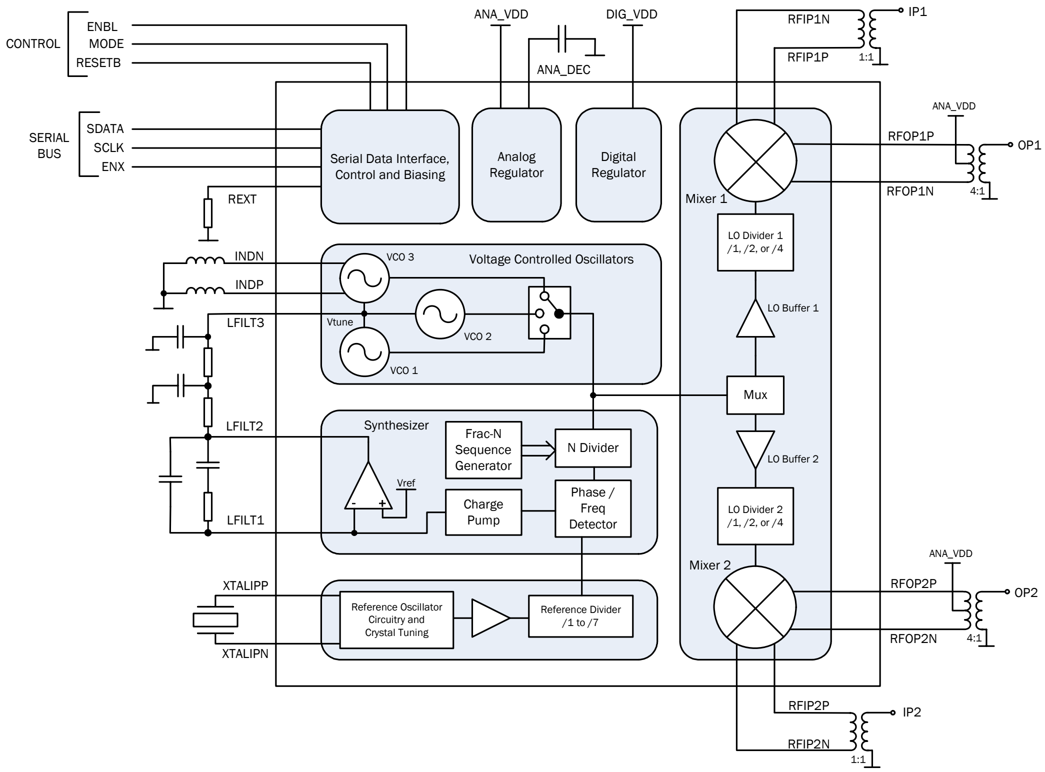
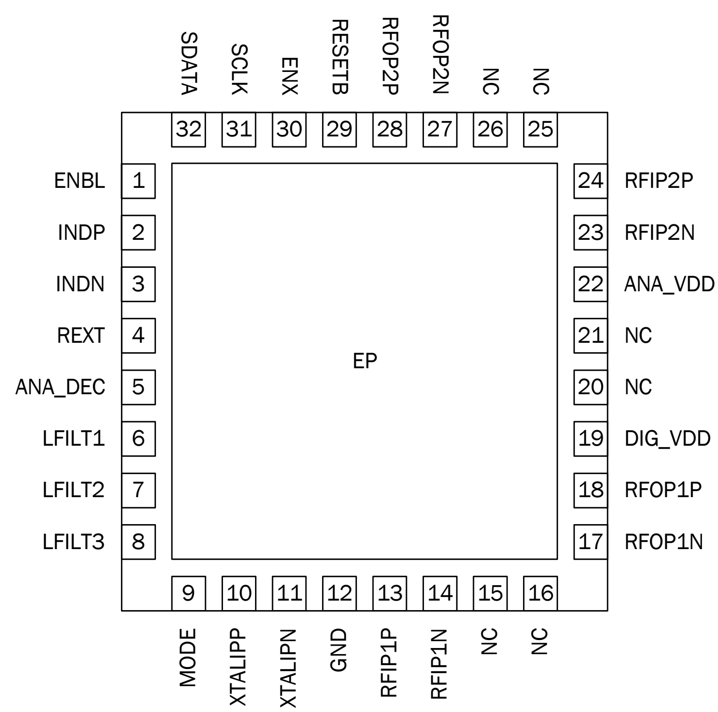
Detailed Functional Block Diagram



Pin Out



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Pin	Function	Description
1	ENBL	Ensure that the ENBL high voltage level is not greater than V_{DD}. An RC low-pass filter could be used to reduce digital noise.
2	INDP	VCO 3 differential inductor. Normally a micro-strip inductor is used to set the VCO 3 frequency range 1200MHz to 1600MHz.
3	INDN	VCO 3 differential inductor. Normally a micro-strip inductor is used to set the VCO 3 frequency range 1200MHz to 1600MHz.
4	REXT	External bandgap bias resistor. Connect a 51kΩ resistor from this pin to ground to set the bandgap reference bias current. This could be a sensitive low frequency noise injection point.
5	ANA_DEC	Analog supply decoupling capacitor. Apply RF decoupling to a good quality ground as close to the pin as possible.
6	LFILT1	Phase detector output. Low-frequency noise-sensitive node.
7	LFILT2	Loop filter op-amp output. Low-frequency noise-sensitive node.
8	LFILT3	VCO control input. Low-frequency noise-sensitive node.
9	MODE	Mode select pin. An RC low-pass filter can be used to reduce digital noise.
10	XTALIPP	Reference crystal / reference oscillator input. Should be AC-coupled if an external reference is used. See note 3.
11	XTALIPN	Reference crystal / reference oscillator input. Should be AC-coupled to ground if an external reference is used. See note 3.
12	GND	Connect to ground.
13	RFIP1P	Differential input 1. See note 1.
14	RFIP1N	Differential input 1. See note 1.
15	NC	
16	NC	
17	RFOP1N	Differential output 1. See note 2.
18	RFOP1P	Differential output 1. See note 2.
19	DIG_VDD	Digital supply. Should be decoupled as close to the pin as possible.
20	NC	
21	NC	
22	ANA_VDD	Analog supply. Should be decoupled as close to the pin as possible.
23	RFIP2N	Differential input 2. See note 1.
24	RFIP2P	Differential input 2. See note 1.
25	NC	
26	NC	
27	RFOP2N	Differential output 2. See note 2.
28	RFOP2P	Differential output 2. See note 2.
29	RESETB	Chip reset (active low). Connect to DIG_VDD if external reset is not required.
30	ENX	Serial interface select (active low). An RC low-pass filter could be used to reduce digital noise.
31	SCLK	Serial interface clock. An RC low-pass filter could be used to reduce digital noise.
32	SDATA	Serial interface data. An RC low-pass filter could be used to reduce digital noise.
EP	Exposed pad	Connect to ground. This is the ground reference for the circuit. All decoupling should be connected here through low impedance paths.

Note 1: The signal should be connected to this pin such that DC current cannot flow into or out of the chip, either by using AC coupling capacitors or by use of a transformer (see evaluation board schematic).

Note 2: DC current needs to flow from ANA_VDD into this pin, either through an RF inductor, or transformer (see evaluation board schematic).

Note 3: Alternatively an external reference can be AC-coupled to pin 11 XTALIPN, and pin 10 XTALIPP decoupled to ground. This may make PCB routing simpler.

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +3.6	V
Input Voltage (V_{IN}), any Pin	-0.3 to V_{DD}+0.3	V
RF/IF Mixer Input Power	+15	dBm
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

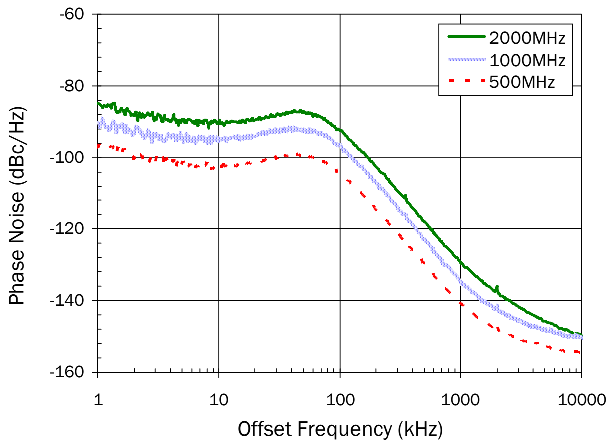
RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD Requirements					
Human Body Model					
General	2000			V	
RF Pins	1000			V	
Machine Model					
General	200			V	
RF Pins	100			V	
Operating Conditions					
Supply Voltage (V_{DD})	2.7	3.0	3.6	V	
Temperature (T_{OP})	-40		+85	°C	
Logic Inputs/Outputs					V_{DD}=Supply to DIG_VDD pin
Input Low Voltage	-0.3		+0.5	V	
Input High Voltage	1.5		V_{DD}	V	
Input Low Current	-10		+10	uA	Input=0V
Input High Current	-10		+10	uA	Input=V_{DD}
Output Low Voltage	0		0.2*V_{DD}	V	
Output High Voltage	0.8*V_{DD}		V_{DD}	V	
Load Resistance	10			kΩ	
Load Capacitance			20	pF	
Static					
Programmable Supply Current (I_{DD})					
Low Current Setting		55		mA	Only one mixer operating.
High Linearity Setting		75		mA	Only one mixer operating.
Standby		3		mA	Reference oscillator and bandgap only.
Power Down Current		140		μA	ENBL=0 and REF_STBY=0
Mixer 1/2					Mixer output driving 4:1 balun.
Gain		-2		dB	Not including balun losses.
Noise Figure					
Low Current Setting		9.5		dB	
High Linearity Setting		12		dB	

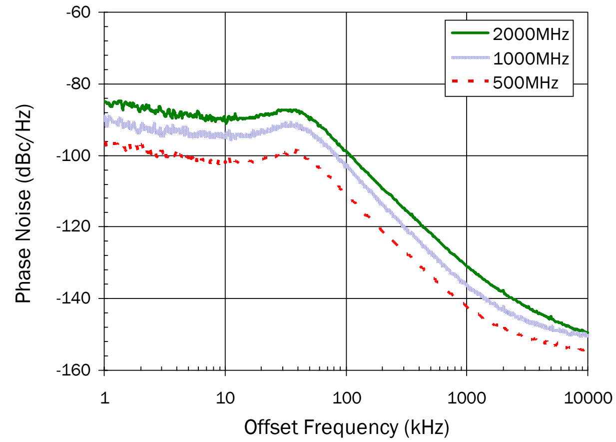
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Mixer 1/2, cont.					
IIP_3					
Low Current Setting		10		dBm	
High Linearity Setting		18		dBm	
Pin1dB					
Low Current Setting		+2		dBm	
High Linearity Setting		+12		dBm	
RF and IF Port Frequency Range	30		2500	MHz	
Mixer Input Return Loss		10		dB	100Ω differential
Voltage Controlled Oscillator					
Open Loop Phase Noise at 1MHz Offset					
2GHz LO Frequency		-130		dBc/Hz	
1GHz LO Frequency		-135		dBc/Hz	
500MHz LO Frequency		-140		dBc/Hz	
Reference Oscillator					
Xtal Frequency	10		52	MHz	
External Reference Frequency	10		104	MHz	
Reference Divider Ratio	1		7		
External Reference Input Level	500	800	1500	mV_{P-P}	AC-coupled
Local Oscillator					
Synthesizer Output Frequency	300		2400	MHz	Dependant on VCO 3 external inductor. After LO dividers.
Phase Detector Frequency			52	MHz	
Closed Loop Phase-Noise at 10kHz Offset					26MHz phase detector frequency
2GHz LO Frequency		-90		dBc/Hz	
1GHz LO Frequency		-95		dBc/Hz	
500MHz LO Frequency		-102		dBc/Hz	

Typical Performance Characteristics: Synthesizer and VCO - V_{DD}=3V, T_A=25°C, as measured on RF2051 evaluation board, for application schematic see page 36. Phase Detector Frequency=26MHz, Loop Bandwidth=60kHz.

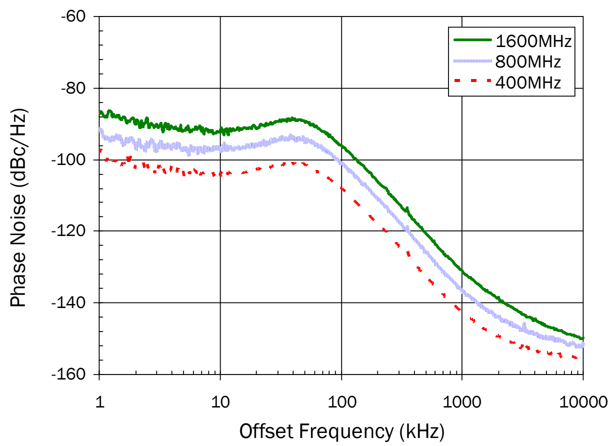
VCO1 With Active Loop Filter



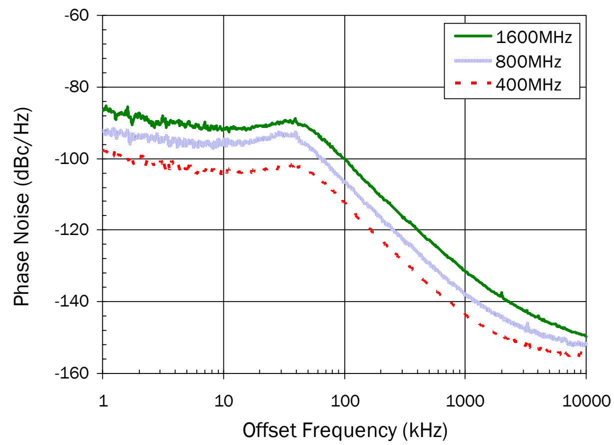
VCO1 With Passive Loop Filter



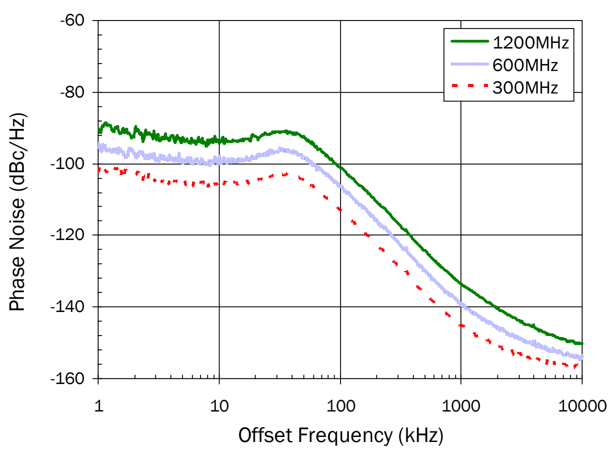
VCO2 With Active Loop Filter



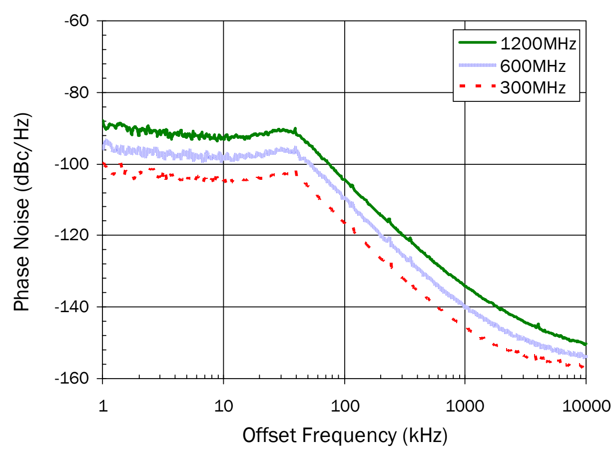
VCO2 With Passive Loop Filter



VCO3 With Active Loop Filter

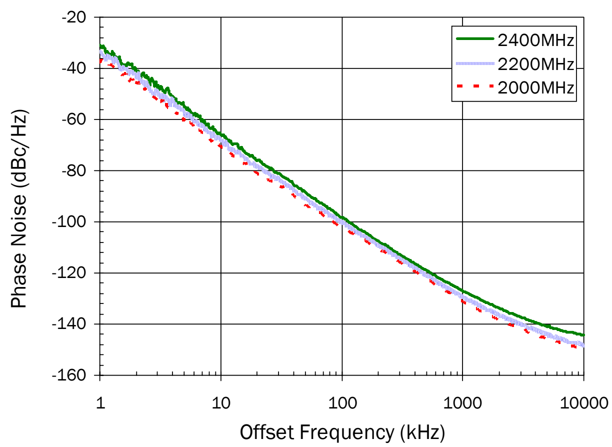


VCO3 With Passive Loop Filter

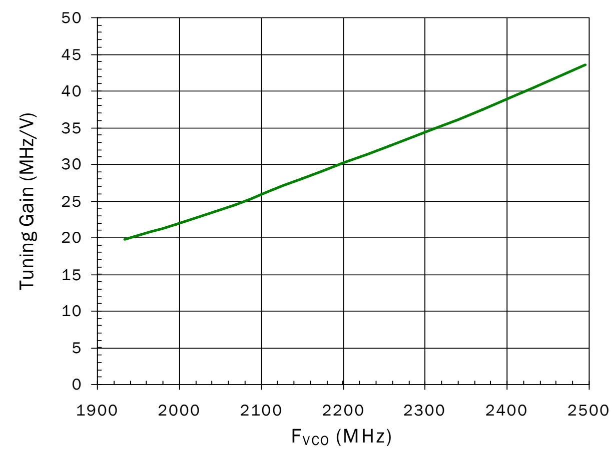


Typical Performance Characteristics: Synthesizer and VCO - V_{DD}=3V, T_A=25°C unless stated, as measured on RF2051 evaluation board, for application schematic see page 36.

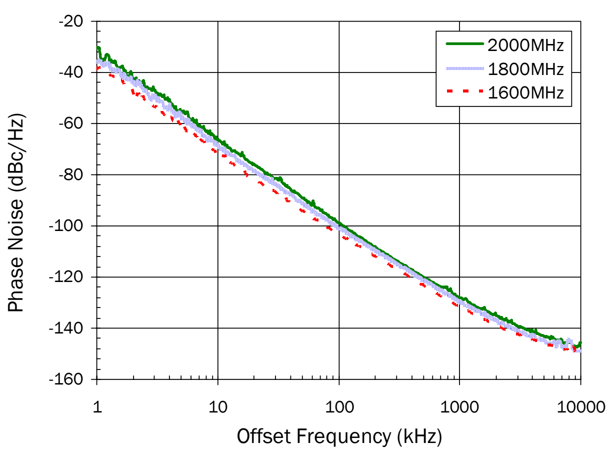
VCO1 Open Loop Phase Noise



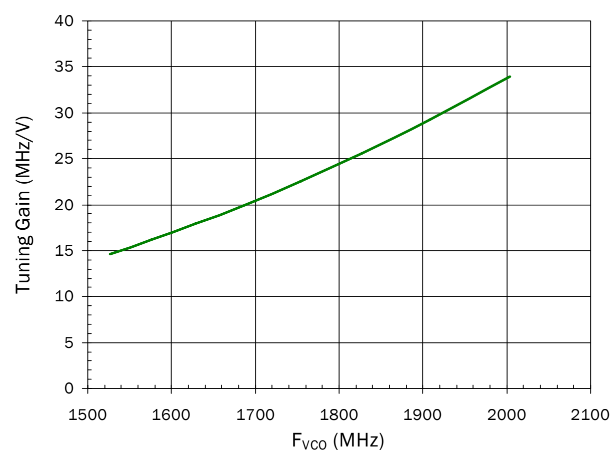
VCO1 Tuning Gain versus Frequency



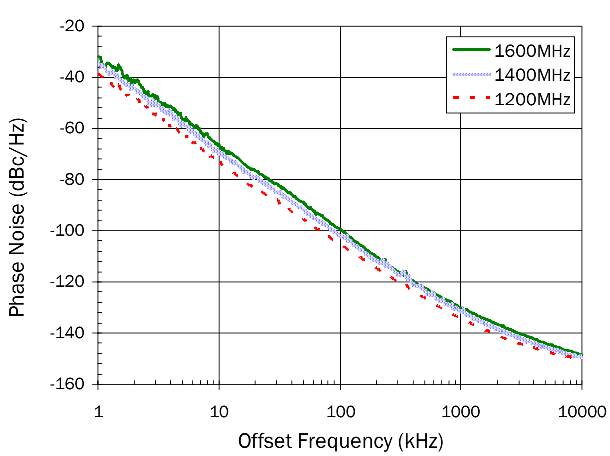
VCO2 Open Loop Phase Noise



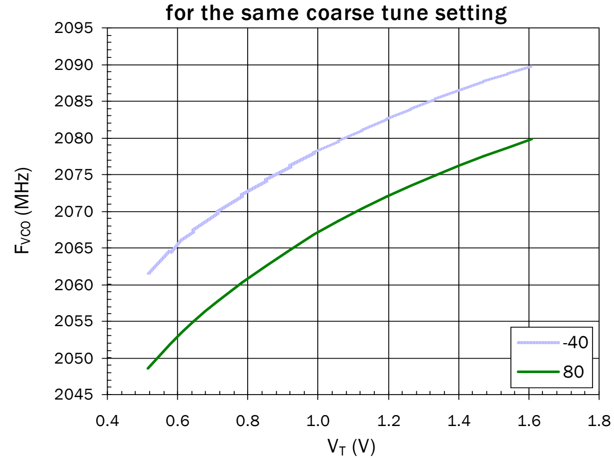
VCO2 Tuning Gain versus Frequency



VCO3 Open Loop Phase Noise

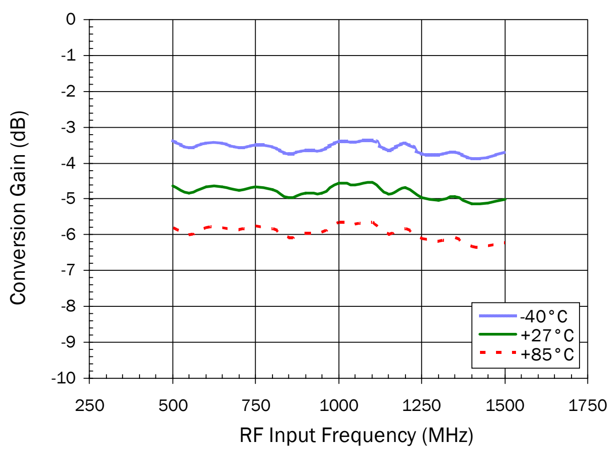


VCO1 F_{VCO} versus V_T
for the same coarse tune setting



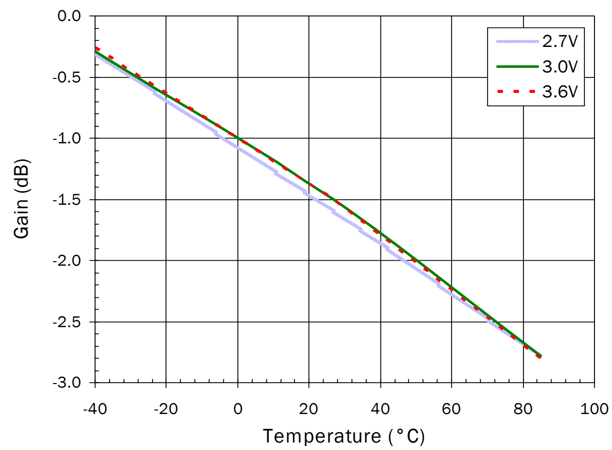
Typical Performance Characteristics: RF Mixers - V_{DD}=3V, T_A=25°C unless stated, as measured on RF2051 evaluation board, for application schematic see page 36.

Mixer 1 Conversion Gain, IF Output=100MHz

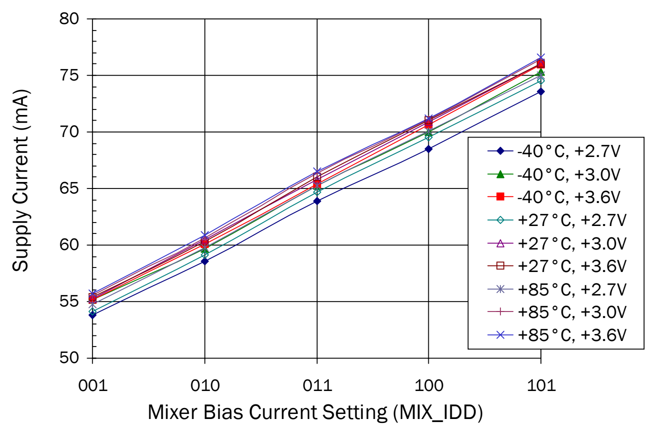


Gain versus Temperature and Supply Voltage

(excluding losses in PCB and Baluns)



Operating Current, One Mixer Enabled versus Temperature and Supply Voltage



RF2051 Typical Operating Current in mA in Full Duplex Mode (both mixers enabled)

MIX1_IDD	MIX2_IDD				
	001	010	011	100	101
001	70	75	80	85	90
010	75	81	86	91	95
011	81	86	91	96	101
100	86	91	97	101	106
101	92	97	102	107	112

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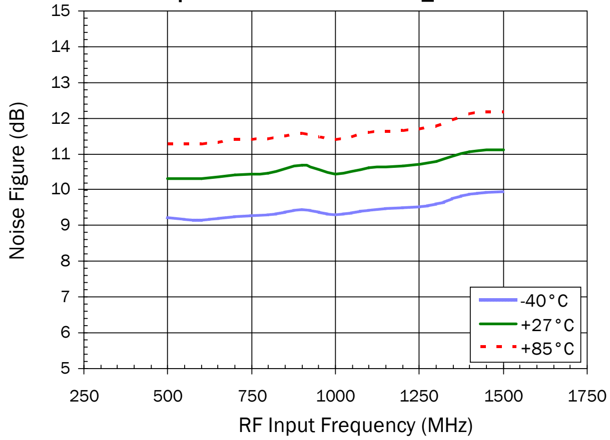
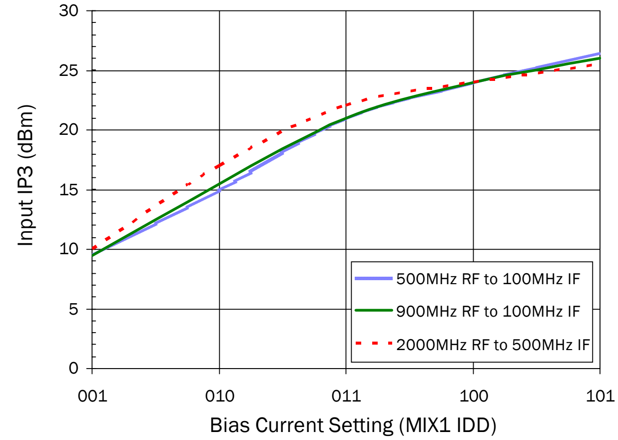
Typical Performance Characteristics: RF Mixers - V_{DD}=3V, T_A=25°C unless stated, as measured on RF2051 evaluation board, for application schematic see page 36.

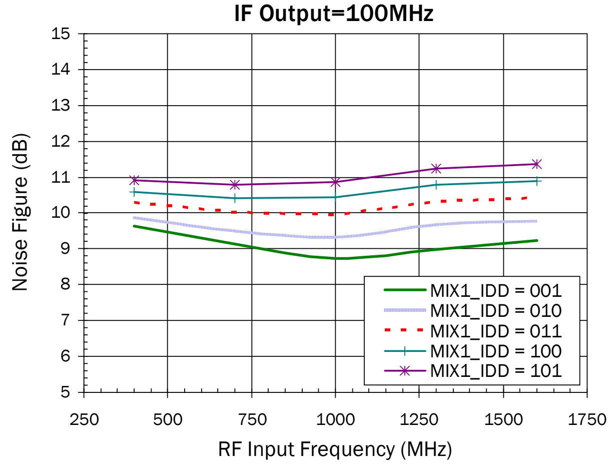
Mixer 1 Noise Figure versus Temperature
IF Output=100MHz and MIX1_IDD=100



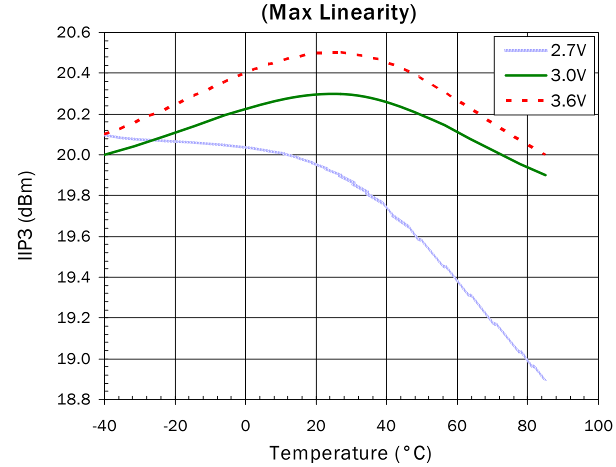
Mixer 1 Input IP3 versus Bias Current Setting



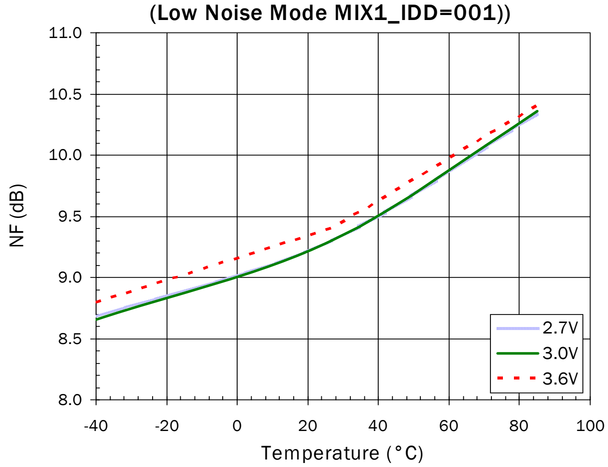
Mixer 1 Noise Figure versus Bias Current
IF Output=100MHz



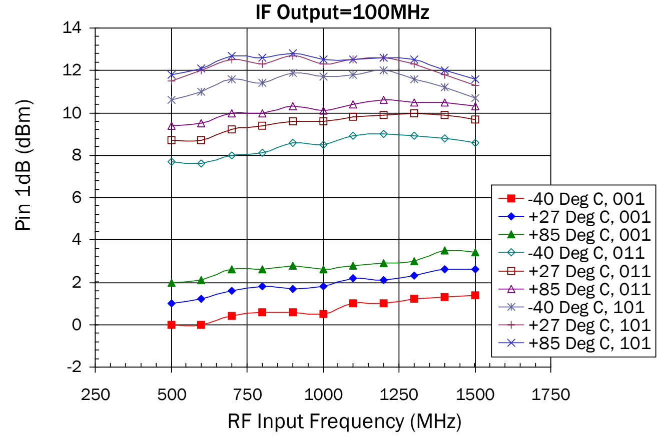
IIP3 versus Temperature and Supply Voltage
(Max Linearity)



NF versus Temperature and Supply Voltage
(Low Noise Mode MIX1_IDD=001))



Mixer 1 Input Power for 1dB Compression
versus Temperature and Bias Current Setting
IF Output=100MHz



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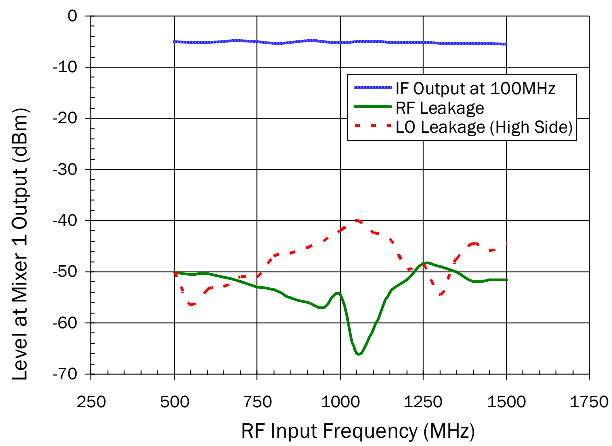
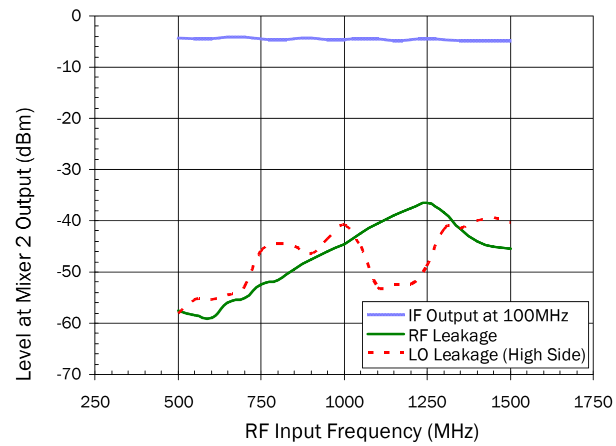
Typical Performance Characteristics: RF Mixers - V_{DD}=3V, T_A=25°C unless stated, as measured on RF2051 evaluation board, for application schematic see page 36.

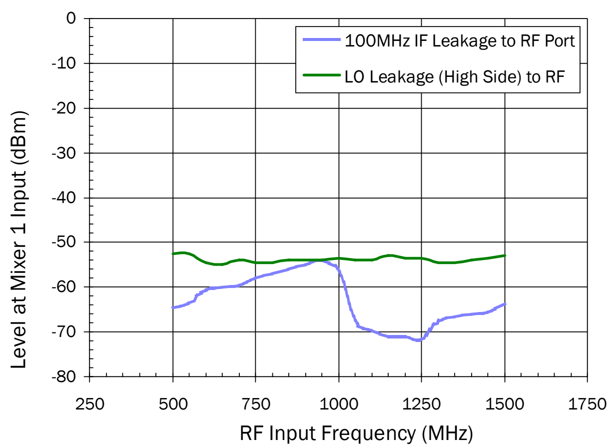
Mixer 1 Typical RF and LO Leakage at IF Output



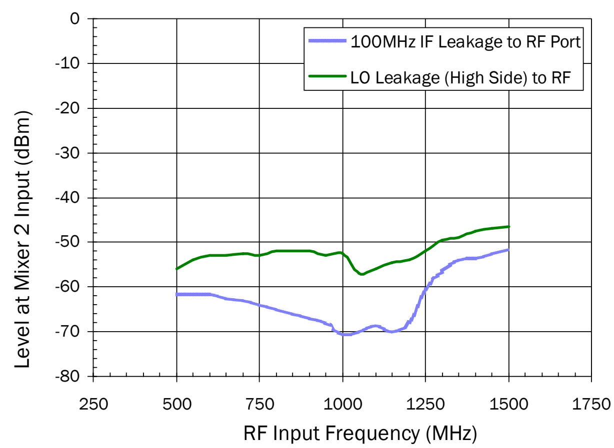
Mixer 2 Typical RF and LO Leakage at IF Output



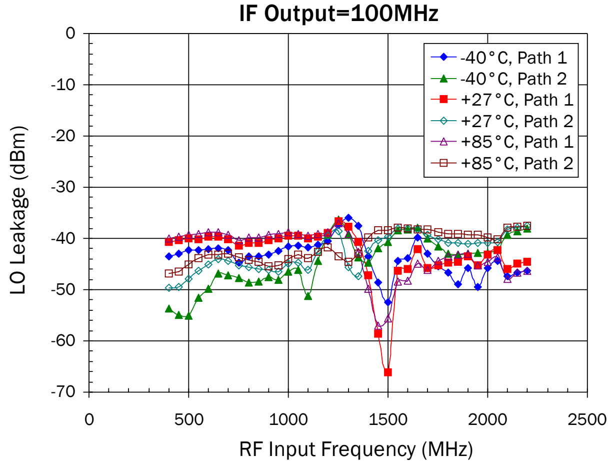
Mixer 1 Typical IF and LO Leakage at RF Input



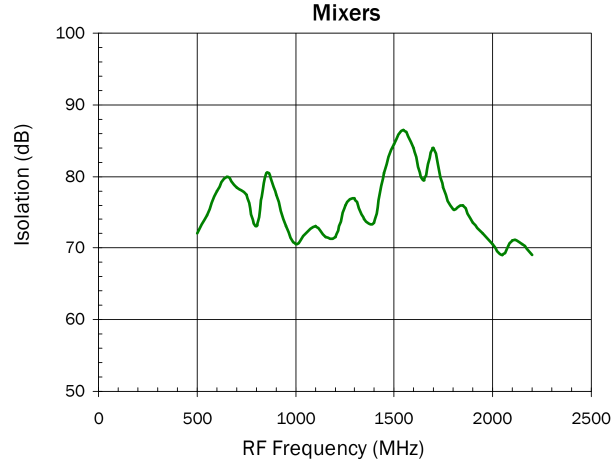
Mixer 2 Typical IF and LO Leakage at RF Input



Mixer Typical LO Leakage at IF Output
IF Output=100MHz



Full Duplex Mode Typical Isolation Between Mixers



Detailed Description

The RF2051 is a wideband RF frequency converter chip which includes a fractional-N phase-locked loop, a crystal oscillator circuit, a low noise VCO core, a LO signal multiplexer, two buffer circuits and two RF mixers. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. All on-chip registers are programmed through a simple three-wire serial interface.

VCO

The VCO core in the RF2051 consists of three VCOs which, in conjunction with the integrated 2/4 LO divider, cover the LO range from 300MHz to 2400MHz.

VCO	Tank Inductor	VCO Frequency Range	DIV 2	DIV 4
1	Internal	1800MHz to 2400MHz	900MHz to 1200MHz	450MHz to 600MHz
2	Internal	1500MHz to 2100MHz	750MHz to 1050MHz	375MHz to 525MHz
3	External	1200MHz to 1600MHz*	600MHz to 800MHz	300MHz to 400MHz

*The frequency of VCO3 is set by external inductors and can be varied by the user.

VCO 1, 2, and 3 are selected using the PLL1x0:P1_VCOSEL and PLL2x0:P2_VCOSEL control words. Each VCO has 128 overlapping bands to achieve an acceptable VCO gain (20MHz/V nom) and hence a good phase noise performance across the whole tuning range. The chip automatically selects the correct VCO band ("VCO coarse tuning") to generate the desired LO frequency based on the values programmed into the PLL1 and PLL2 registers banks. For information on how to program the desired LO frequency into the PLL1 and PLL2 banks refer to page 12.

The automatic VCO band selection is triggered every time the ENBL pin is taken high. Once the band has been selected the PLL will lock onto the correct frequency. During the band selection process fixed capacitance elements are progressively connected to the VCO resonant circuit until the VCO is oscillating at approximately the correct frequency. The output of this band selection is made available in the RB1:CT_CAL read-back register. A value of 127 or 0 in this register indicates that the selection was unsuccessful, this is usually due to the wrong VCO being selected so the user is trying to program a frequency that is outside of the VCO operating range. A value between 1 and 126 indicates a successful calibration, the actual value being dependent on the desired frequency as well as process variation for a particular device. The band selection takes approximately 1500 cycles of the phase detector clock (about 50us with a 26MHz clock). The band select process will center the VCO tuning voltage at about 1.2V, compensating for manufacturing tolerances and process variation as well as environmental factors including temperature. For applications where the synthesizer is always on and the LO frequency is fixed, the synthesizer will maintain lock over a +/-60°C temperature range. However it is recommended to re-initiate an automatic band selection for every 30 degrees change in temperature in order to maintain optimal synthesizer performance. This assumes an active loop filter. If start-up time is a critical parameter, and the user is always programming the same frequency for the PLL, the calibration result may be read back from the RB1:CT_CAL register, and written to the PLL1x2:P1_CT_DEF or PLL2x2:P2_CT_DEF registers (depending on desired PLL register bank). The calibration function must then be disabled by setting the PLL1x0:P1_CT_EN and/or PLL2x0:P2_CT_EN control words to 0. For further information please refer to the RF205x Calibration User Guide.

The LO divide ratio is set by the PLL1x0:P1_LODIV and PLL2x0:P2_LODIV control words.

The LO is routed to mixer1, mixer2, or both depending on the state of the MODE pin and the value of CFG1:FULLD.

The current in the VCO core can be programmed using the PLL1x1:P1_VCOI or PLL2x1:P2_VCOI control words. This allows optimization of VCO performance for a particular frequency. For applications where the required LO frequency is above 2GHz it is recommended that the LO buffer current be increased by setting CFG5:LO1_I and CFG5:LO2_I to 1100 (hex value C).

Fractional-N PLL

The IC contains a charge-pump based fractional-N phase locked loop (PLL) for controlling the three VCOs. The PLL includes automatic calibration systems to counteract the effects of process and environmental variations, ensuring repeatable lock-time and noise performance. The PLL is intended to use a reference frequency signal of 10MHz to 104MHz. A reference divider (divide by 1 to divide by 7) is supplied and should be programmed to limit the frequency at the phase detector to a maximum of 52MHz. The reference divider bypass is controlled by bit CLK DIV_BYP, set low to enable the reference divider and set high for divider bypass (divide by 1). The remaining three bits CLK DIV<15:13> set the reference divider value, divide by 2 (010) to 7 (111) when the reference divider is enabled.

Two PLL programming banks are provided, the first bank is preceded by the label PLL1 and the second bank is preceded by the label PLL2. For the RF2051 these banks are used to program mixer 1 and mixer 2 respectively, and are selected automatically as the mixer is selected (using the MODE pin).

The PLL will lock the VCO to the frequency F_{VCO} according to:

$$F_{VCO} = N_{EFF} * F_{OSC} / R$$

where N_{EFF} is the programmed fractional N divider value, F_{OSC} is the reference input frequency, and R is the programmed R divider value (1 to 7).

The N divider is a fractional divider, containing a dual-modulus prescaler and a digitally spur-compensated fractional sequence generator to allow fine frequency steps. The N divider is programmed using the N and NUM bits as follows:

First determine the desired, effective N divider value, N_{EFF}:

$$N_{EFF} = F_{VCO} * R / F_{OSC}$$

N(9:0) should be set to the integer part of N_{EFF}. NUM should be set to the fractional part of N_{EFF} multiplied by $2^{24} = 16777216$.

Example: VCO1 operating at 2220MHz, 23.92MHz reference frequency, the desired effective divider value is:

$$N_{EFF} = F_{VCO} * R / F_{OSC} = 2220 * 1 / 23.92 = 92.80936454895.$$

The N value is set to 92, equal to the integer part of N_{EFF}, and the NUM value is set to the fractional portion of N_{EFF} multiplied by 2^{24}:

$$NUM = 0.80936454895 * 2^{24} = 13{,}578{,}884.$$

Converting N and NUM into binary results in the following:

N = 0 0101 1100
NUM = 1100 1111 0011 0010 1000 0100

So the registers would be programmed:

P1_N (or P2_N) = 0 0101 1100
P1_NUM_MSB (or P2_NUM_MSB) = 1100 1111 0011 0010
P1_NUM_LSB (or P2_NUM_LSB) = 1000 0100

The maximum N_{EFF} is 511, and the minimum N_{EFF} is 12. The minimum step size is $F_{OSC}/R * 2^{24}$. Thus for a 23.92MHz reference, the frequency step size would be 1.4Hz. The minimum reference frequency that could be used to program a frequency of 2400MHz (using VCO1) is 2400/511, 4.697MHz (approx).

Phase Detector and Charge Pump

The chip provides a current output to drive an external loop filter. An on-chip operational amplifier can be used to design an active loop filter or a passive design can be implemented. The maximum charge pump output current is set by the value contained in the P1_CP_DEF/P2_CP_DEF field and CP_LO_I.

In the default state (P1_CP_DEF/P2_CP_DEF=31 and CP_LO_I=0) the charge pump current (ICPset) is 120uA. If CP_LO_I is set to 1 this current is reduced to 30uA.

The charge pump current can be altered by changing the value of P1_CP_DEF/P2_CP_DEF. The charge pump current is defined as:

ICP= ICPset*CP_DEF / 31

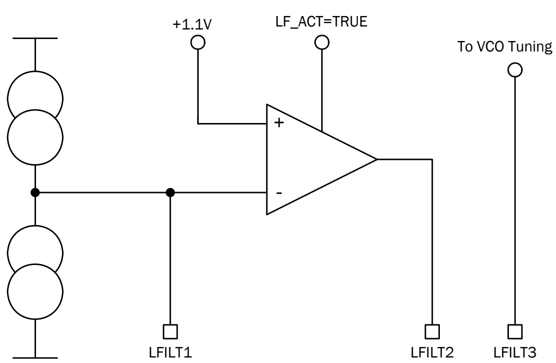
If automatic loop bandwidth correction is enabled the charge pump current is set by the calibration algorithm based upon the VCO gain. For more information on the VCO gain calibration, which is disabled by default, please refer to the RF205x Calibration User Guide.

The phase detector will operate with a maximum input frequency of 52MHz.

Note that for high phase detector frequencies, the divider ratio decreases. For $N<28$ the FLL_FACT register needs to be changed to 00 from the default value of 01. This is to ensure correct VCO band selection.

Loop Filter

The PLL may be designed to use an active or a passive loop filter as required. The internal configuration of the chip is shown below. If the CFG1:LF_ACT bit is asserted high, the op-amp will be enabled. If the CFG1:LF_ACT bit is asserted low, the internal op-amp is disabled and a high impedance is presented to the LFILT1 pin. The RF205x Programming Tool software can assist with loop filter designs. Because the op-amp is used in an inverting configuration in active mode, when the passive loop filter mode is selected the phase-detector polarity should be inverted. For active mode, CFG1:PDP=1, for passive mode, CFG1:PDP=0.



The charge pump output voltage compliance range is typically +0.7V to +1.5V. For applications using a passive loop filter VCO coarse tuning must be performed regularly enough to ensure that the VCO tuning voltage falls within this compliance range at all temperatures. The active loop filter maintains the charge pump output voltage in the center of the compliance range, and the op-amp provides a wider VCO tuning voltage range, typical 0V to +2.9V.

Crystal Oscillator

The PLL may be used with an external reference source, or its own crystal oscillator. If an external source (such as a TCXO) is being used it should be AC-coupled into one of the XO inputs, and the other input should be AC-coupled to ground.

A crystal oscillator typically takes many milliseconds to settle, and so for applications requiring rapid pulsed operation of the PLL (such as a TDMA system, or Rx/Tx half-duplex system) it is necessary to keep the XO running between bursts. However, when the PLL is used less frequently, it is desirable to turn off the XO to minimize current draw. The REFSTBY register is provided to allow for either mode of operation. If REFSTBY is programmed high, the XO will continue to run even when ENBL is asserted low. Thus the XO will be stable and a clock is immediately available when ENBL is asserted high, allowing the chip to assume normal operation. On cold start, or if REFSTBY is programmed low, the XO will need a warm-up period before it can provide a stable clock. The length of this warm-up period will be dependant on the crystal characteristics.

The crystal oscillator circuit contains internal loading capacitors. No external loading capacitors are required, dependant on the crystal loading specification. The internal loading capacitors are a combination of fixed capacitance, and an array of switched capacitors. The switched capacitors can be used to tune the crystal oscillator onto the required center frequency and minimize frequency error. The PCB stray capacitance and oscillator input and output capacitance will also contribute to the crystal's total load capacitance. The register settings in the CFG4 register for the switched capacitors are as follows:

- Coarse Tune XO_CT (4 bits) 15 * 0.55 pF, default 0100
- Fine Step XO_CR_S (1 bit) 1 * 0.25 pF, default 0

The on chip fixed capacitance is approximately 4.2 pF.

Wideband Mixer

The RF2051 includes two wideband, double-balanced Gilbert cell mixers. They support RF/IF frequencies of 30 MHz to 2500 MHz using the internal VCO to provide the LO frequency of 300 MHz to 2400 MHz. Each mixer has an input port and an output port that can be used for either IF or RF, i.e. for up conversion or down conversion. The mixer current can be programmed to between 15 mA and 35 mA depending on linearity requirements, using the MIX1_IDD<3.0> word for mixer 1 and the MIX2_IDD<3.0> word for mixer 2, both of which are in the CFG2 register. The majority of the mixer current is sourced through the output pins via either a centre-tapped balun or an RF choke in the external matching circuitry to the supply.

The RF mixer input and output ports are differential and require simple matching circuits optimized to the specific application frequencies. A conversion gain of approximately -3 dB to 0 dB is achieved with 100 Ω differential input impedance, and the outputs driving 200 Ω differential load impedance. Increasing the mixer output load increases the conversion gain.

The mixer has a broadband common gate input. The input impedance is dominated by the resistance set by the mixer 1/gm term, which is inversely proportional to the mixer current setting. The resistance will be approximately 85 Ω at the default mixer current setting (100). There is also some shunt capacitance at the mixer input, and the inductance of the bond wires to consider at higher frequencies.

The mixer output is high impedance, consisting of a resistance of approximately 2 kΩ in parallel with some capacitance. The mixer output does not need to be matched as such, just to see a resistive load. A higher resistance load will give higher output voltage and gain. A shunt inductor can be used to resonate with the mixer output capacitance at the frequency of interest. This inductor may not be required at lower frequencies where the impedance of the output capacitance is less significant. At higher output frequencies the inductance of the bond wires becomes more significant.

For more information about the mixer port impedances and matching, please refer to the RF205x Family Application Note on Matching Circuits and Baluns.

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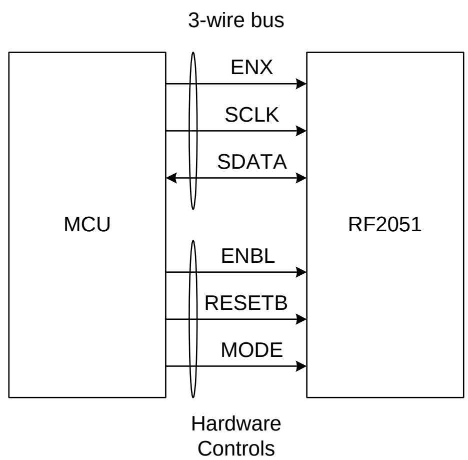
The mixer layout and pin placement has been optimized for high mixer-to-mixer isolation of typically 60dB. The mixers can be set up to operate in half-duplex mode (1 mixer active) or full duplex mode (both mixers active). The mode selection is done via hardware control of the MODE pin and by setting the FULLD bit in the CFG1 register as shown in the table below. When in full-duplex mode, one can either use PLL register bank 1 or 2, the LO signal is routed to both mixers.

Mode Pin	FULLD Bit	Active PLL Register Bank	Active Mixer
Low	0	1	1
High	0	2	2
Low	1	1	Both
High	1	2	Both

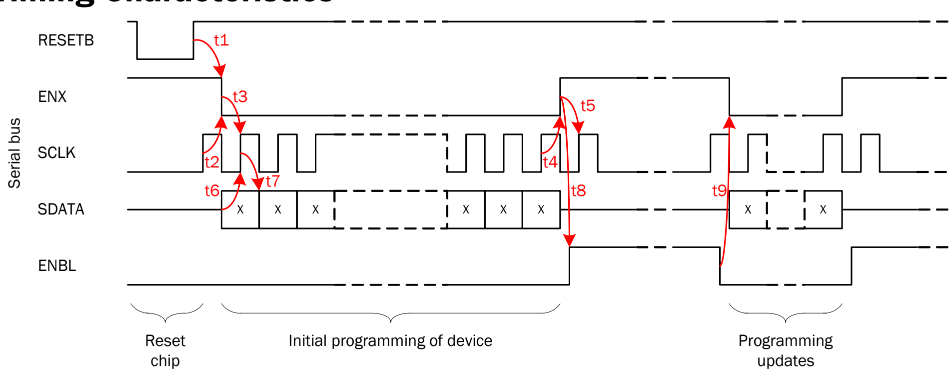
General Programming Information

Serial Interface

All on-chip registers in the RF2051 are programmed using a 3-wire serial bus which supports both write and read operations. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. Certain functions and operations require the use of hardware controls via the ENBL, MODE, and RESETB pins in addition to programming via the serial bus.



Serial Data Timing Characteristics



Parameter	Description	Time
t1	Reset delay	>5ns
t2	Programming setup time	>5ns
t3	Programming hold time	>5ns
t4	ENX setup time	>5ns
t5	ENX hold time	>5ns
t6	Data setup time	>5ns
t7	Data hold time	>5ns
t8	ENBL setup time	>0ns
t9	ENBL hold time	>0ns

Write

Initially ENX is high and SDATA is high impedance. The write operation begins with the controller starting SCLK. On the first falling edge of SCLK the baseband asserts ENX low. The second rising edge of SCLK is reserved to allow the SDI to initialize, and the third rising edge is used to define whether the operation will be a write or a read operation. In write mode the baseband will drive SDATA for the entire telegram. RF2051 will read the data bit on the rising edge of SCLK.

The next 7 data bits are the register address, MSB first. This is followed by the payload of 16 data bits for a total write mode transfer of 24 bits. Data is latched into RF2051 on the last rising edge of SCLK (after ENX is asserted high).

For more information, please refer to the timing diagram on page 16.

The maximum clock speed for a register write is 19.2MHz. A register write therefore takes approximately 1.3us. The data is latched on the rising edge of the clock. The datagram consists of a single start bit followed by a '0' (to indicate a write operation). This is then followed by a seven bit address and a sixteen bit data word.

Note that since the serial bus does not require the presence of the crystal clock, it is necessary to insert an additional rising clock edge before the ENX line is set low to ensure the address/data are read correctly.

Read

Initially ENX is high and SDATA is high impedance. The read operation begins with the controller starting SCLK. The controller is in control of the SDATA line during the address write operation. On the first falling edge of SCLK the baseband asserts ENX low. The second rising edge of SCLK is reserved to allow the SDI to initialize, and the third rising edge is used to define whether the operation will be a write or a read operation. In read mode the baseband will drive SDATA for the address portion of the telegram, and then control will be handed over to RF2051 for the data portion. RF2051 will read the data bits of the address on the rising edge of SCLK. After the address has been written, control of the SDATA line is handed over to RF2051. One and a half clocks are reserved for turn-around, and then the data bits are presented by RF2051. The data is set up on the rising edge of SCLK, and the controller latches the data on the falling edge of SCLK. At the end of the data transmission, RF2051 will release control of the SDATA line, and the controller asserts ENX high. The SDATA port on RF2051 transitions from high impedance to low impedance on the first rising edge of the data portion of the transaction (for example, 3 rising edges after the last address bit has been read), so the controller chip should be presenting a high impedance by that time.

For more information, please refer to the timing diagram on page 16.

The maximum clock speed for a register read is 19.2MHz. A register read therefore takes approximately 1.4us. The address is latched on the rising edge of the clock and the data output on the falling edge. The datagram consists of a single start bit followed by a '1' (to indicate a read operation), followed by a seven bit address. A 1.5 bit delay is introduced before the sixteen bit data word representing the register content is presented to the receiver.

Note that since the serial bus does not require the presence of the crystal clock, it is necessary to insert an additional rising clock edge before the ENX line is set low to ensure the address is read correctly.

Hardware Control

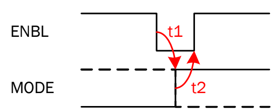
Three hardware control pins are provided: ENBL, MODE, and RESETB.

ENBL Pin

The ENBL pin has two functions: to enable the analog circuits in the chip and to trigger the VCO band selection as described in the VCO section on page 11.

ENBL Pin	REFSTBY Bit	XO and Bias Block	Analogue Block	Digital Block
Low	0	Off	Off	On
Low	1	On	Off	On
High	0	On	On	On
High	1	On	On	On

As outlined in the VCO section the chip has a built-in automatic VCO band selection to tune the selected VCO to the desired frequency. The band selection is initiated when the ENBL pin is taken high. Every time the frequency of the synthesizer is re-programmed, the ENBL has to be inserted high to initiate the automatic VCO band selection (VCO coarse tune).



Parameter	Description	Time
t1	MODE setup time	>5ns
t2	MODE hold time	>5ns

RESETB Pin

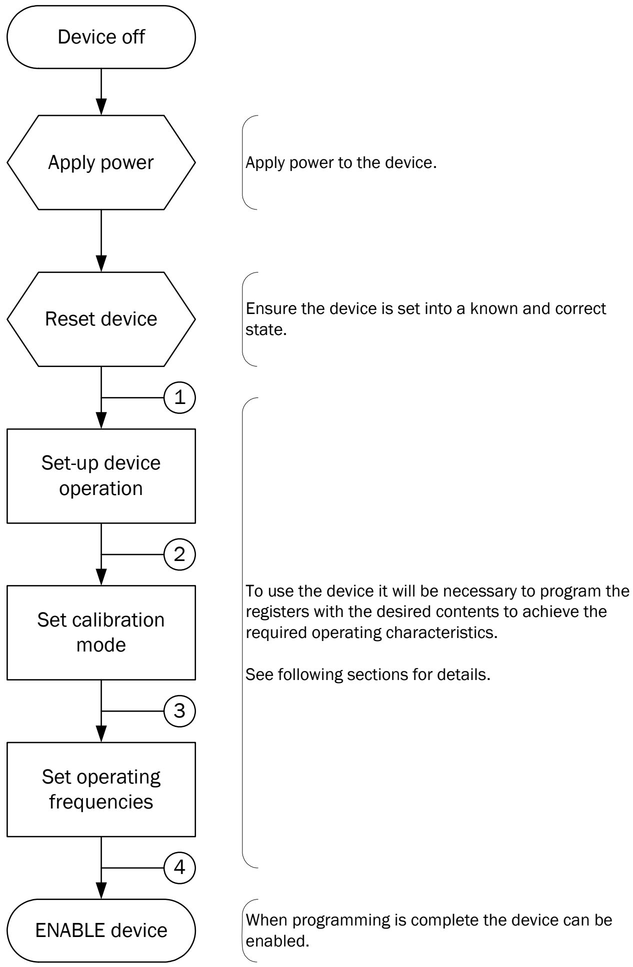
The RESETB pin is a hardware reset control that will reset all digital circuits to their start-up state when asserted low. The device includes a power-on-reset function, so this pin should not normally be required, in which case it should be connected to the positive supply.

MODE Pin

The MODE pin controls which mixer(s) and PLL programming register bank is active. See the PLL and Mixer description sections for details.

Programming the RF2051

The figure below shows an overview of the device programming.



Note: The set-up processes 1 to 2, 2 to 3, and 3 to 4 are explained further below.

Additional information on device use and programming can be found on the RF205X family page of the RFMD web site (http://www.rfmd.com/rf205x). The following documents may be particularly helpful:

- RF205x Frequency Synthesizer User Guide
- RF205x Calibration User Guide

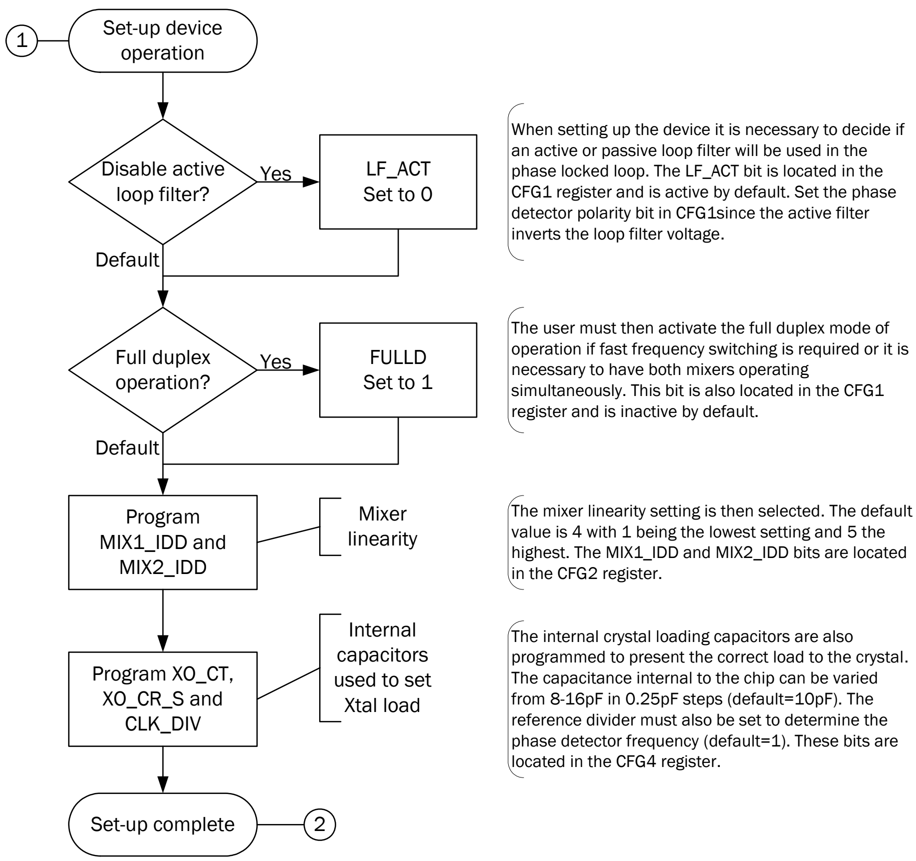
Start-up

When starting up and following device reset then REFSTBY=0, REFSTBY should be asserted high approximately 500µs before ENBL is taken high. This is to allow the XO to settle and will depend on XO characteristics. The various calibration routines will also take some time depending on whether they are enabled or not. Coarse tuning calibration takes about 50µs and VCO tuning gain compensation takes about 100µs. Additionally, time for the PLL to settle will be required. All of these timings will be dependant upon application specific factors such as loop filter bandwidth, reference clock frequency, XO characteristics and so on. The fastest turn-on and lock time will be obtained by leaving REFSTBY asserted high, disabling all calibration routines, and setting the PLL loop bandwidth as wide as possible.

The device can be reset into its initial state (default settings) at any time by performing a hard reset. This is achieved by setting the RESETB pin low for at least 100ns.

Setting Up Device Operation

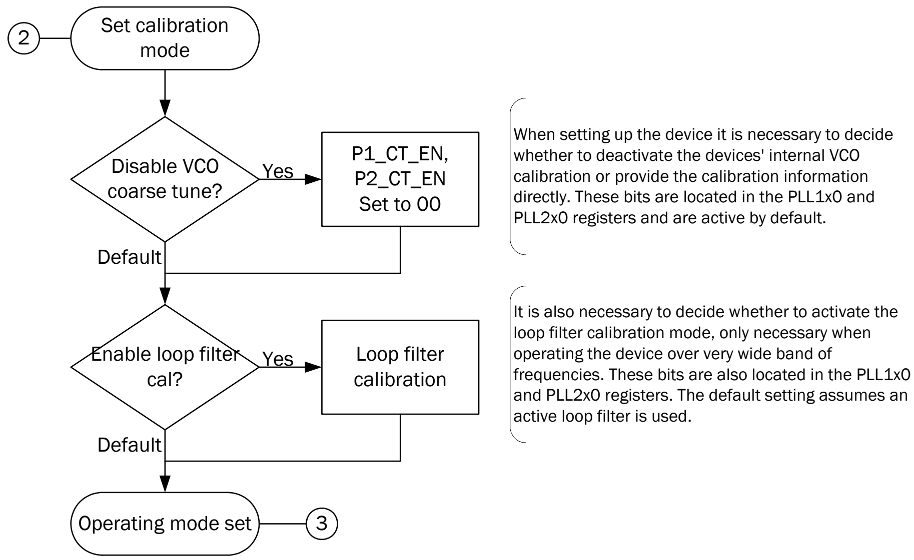
The device offers a number of operating modes which need to be set up in the device before it will work as intended. This is achieved as follows.



Three registers need to be written, taking 3.9us at the maximum clock speed. If the device is used with an active filter in simplex operation it will not be necessary to program CFG1 reducing the programming time to 2.6us.

Setting Up VCO Coarse Tuning and Loop Filter Calibration

If the user wishes to disable the VCO coarse tune calibration or enable the loop filter calibration then the following programming operation will need to take place.

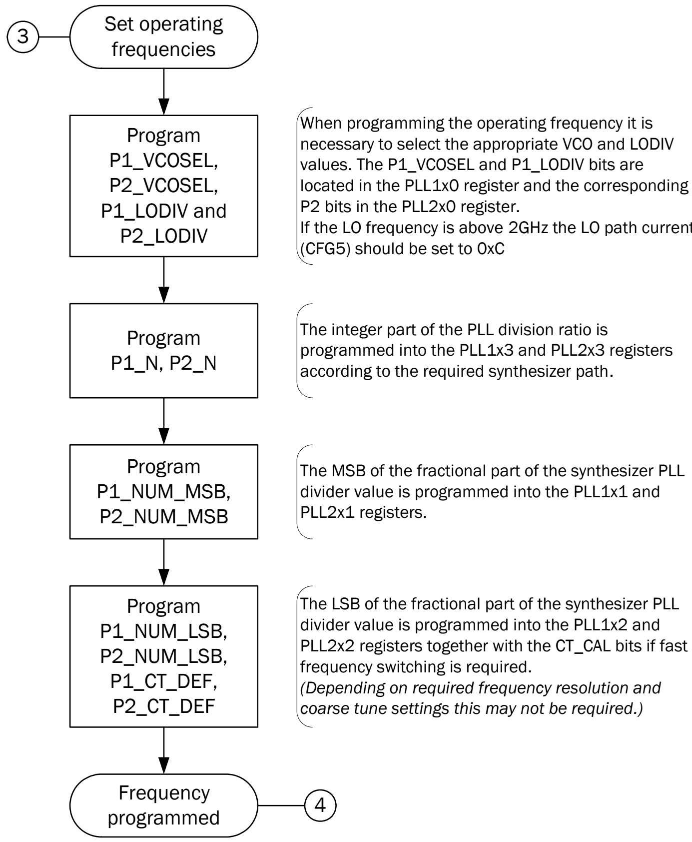


Two registers need to be written taking 2.6us at maximum clock speed if the course tuning is deactivated or the loop filter calibration activated. Since it is necessary to program these registers when setting the operating frequency (see next section) this operation usually carries no overhead.

The coarse tune calibration takes approximately 50us when using a 26MHz reference clock (it will take proportionally longer if a slower clock is used, and vice versa).

Setting The Operating Frequency

Setting the operating frequency of the device requires a number of registers to be programmed.



A total of four registers must be programmed to set the device operating frequency for each path within the device. This will take 5.2us for each path at maximum clock speed.

To change the frequency of the VCO it will be necessary to repeat these operations. However, if the frequency shift is small it may not be necessary to reprogram the VCOSEL and LODIV bits reducing the register writes to three per path.

For an example on how to determine the integer and fractional parts of the synthesizer PLL division ratio please refer to the detailed description of the PLL on page 12.

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Programming Registers

Register Map Diagram

Reg. Name	R/W	Add	Data															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG1	R/W	00	LD_EN	LD_LEV	TVCO					PDP	LF_ACT	CPL		CT_POL	Res	EXT_VCO	FULLD	CP_LO_I
CFG2	R/W	01	MIX1_IDD			MIX1_VB		MIX2_IDD			MIX2_VB		Res	KV_RNG	NBR_CT_AVG		NBR_KV_AVG	
CFG3	R/W	02	TKV1				TKV2				Res				FLL_FACT		CT_CPOL	REFSTBY
CFG4	R/W	03	CLK_DIV_BYPASS				XO_CT				XO_I2	XO_I1	XO_CR_S	TCT				
CFG5	R/W	04	LO1_I				LO2_I				T_PH_ALGN							
CFG6	R/W	05	SU_WAIT										Res					
PLL1x0	R/W	08	P1_VCOSEL		P1_CT_EN		P1_KV_EN		P1_LODIV		Res		P1_CP_DEF					
PLL1x1	R/W	09	P1_NUM_MSB															
PLL1x2	R/W	0A	P1_NUM_LSB								P1_CT_DEF							Res
PLL1x3	R/W	0B	P1_N									Res				P1_VCOI		
PLL1x4	R/W	0C	P1_DN									P1_CT_GAIN			P1_KV_GAIN			Res
PLL1x5	R/W	0D	P1_N_PHS_ADJ									Res		P1_CT_V				
PLL2x0	R/W	10	P2_VCOSEL		P2_CT_EN		P2_KV__EN		P2_LODIV		Res		P2_CP_DEF					
PLL2x1	R/W	11	P2_NUM_MSB															
PLL2x2	R/W	12	P2_NUM_LSB								P2_CT_DEF							Res
PLL2x3	R/W	13	P2_N									Res				P2_VCOI		
PLL2x4	R/W	14	P2_DN									P2_CT_GAIN			P2_KV_GAIN			Res
PLL2x5	R/W	15	P2_N_PHS_ADJ									Res		P2_CT_V				
GPO	R/W	18	Res	P1_GPO1	Res	P1_GPO3	P1_GPO4	Res				P2_GPO1	Res	P2_GPO3	P2_GPO4	Res		
CHIPREV	R	19	PARTNO								REVNO							
RB1	R	1C	LOCK	CT_CAL							CP_CAL						Res	
RB2	R	1D	V0_CAL								V1_CAL							
RB3	R	1E	RSM_STATE						Res									
TEST	R	1F	TEN	TMUX			CPU	CPD	FNZ	LDO_BYP	TSEL	Res	DACTEST		Res			

CFG1 (00h) - Operational Configuration Parameters

#	Bit Name	Default		Function
15	LD_EN	1	9	Enable lock detector circuitry
14	LD_LEV	0		Modify lock range for lock detector
13	TVCO(4:0)	0		VCO warm-up time=TVCO/(FREF=256)
12		0		
11		0	1	
10		0		
9		0		
8	PDP	1		Phase detector polarity: 0=positive, 1=negative
7	LF_ACT	1	C	Active loop filter enable, 1=Active 0=Passive
6	CPL(1:0)	1		Charge pump leakage current: 00=no leakage, 01=low leakage, 10=mid leakage, 11=high leakage
5		0		
4	CT_POL	0		Polarity of VCO coarse-tune word: 0=positive, 1=negative
3		0	0	
2	EXT_VCO	0		0=Normal operation 1=external VCO (VCO3 disabled, KV_CAL and CT_CAL must be disabled)
1	FULLD	0		0=Half duplex, mixer is enabled according to MODE pin, 1=Full duplex, both mixers enabled
0	CP_LO_I	0		0=High charge pump current, 1=low charge pump current

CFG2 (01h) - Mixer Bias and PLL Calibration

#	Bit Name	Default		Function
15	MIX1_IDD	1	8	Mixer 1 current setting: 000=0mA to 111=35mA in 5mA steps
14		0		
13		0		
12	MIX1_VB	0		Mixer 1 voltage bias.
11		1	C	
10	MIX2_IDD	1		Mixer 2 current setting: 000=0mA to 111=35mA in 5mA steps
9		0		
8		0		
7	MIX2_VB	0	5	Mixer 2 voltage bias
6		1		
5		0		
4	KV_RNG	1		Sets accuracy of voltage measurement during KV calibration: 0=8bits, 1=9bits
3	NBR_CT_AVG	1	8	Number of averages during CT cal
2		0		
1	NBR_KV_AVG	0		Number of averages during KV cal
0		0		

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CFG3 (02h) - PLL Calibration

#	Bit Name	Default		Function
15	TKV1	0	0	Settling time for first measurement in LO KV compensation
14		0		
13		0		
12		0		
11	TKV2	0	4	Settling time for second measurement in LO KV compensation
10		1		
9		0		
8		0		
7		0	0	
6		0		
5		0		
4		0		
3	FLL_FACT	0	4	Default setting 01. Needs to be set to 00 for N<28. This case can arise when higher phase detector frequencies are used.
2		1		
1	CT_CPOL	0		
0	REFSTBY	0		Reference oscillator standby mode 0=XO is off in standby mode, 1=XO is on in standby mode

CFG4 (03h)

#	Bit Name	Default		Function
15	CLK_DIV	0	1	Reference divider, divide by 2 (010) to 7 (111) when reference divider is enabled
14		0		
13		0		
12	CLK_DIV_BYPASS	1		Reference divider enabled=0, divider bypass (divide by 1)=1
11	XO_CT	1	8	Crystal oscillator coarse tune (approximately 0.5pF steps from 8pF to 16pF)
10		0		
9		0		
8		0		
7	XO_I2	0	0	Crystal oscillator current setting
6	XO_I1	0		
5	XO_CR_S	0		Crystal oscillator additional fixed capacitance (approximately 0.25pF)
4	TCT	0		Duration of coarse tune acquisition
3		1	F	
2		1		
1		1		
0		1		

CFG5 (04h) - LO Bias

#	Bit Name	Default		Function
15	LO1_I	0	0	Local oscillator Path1 current setting
14		0		
13		0		
12		0		
11	LO2_I	0	0	Local oscillator Path2 current setting
10		0		
9		0		
8		0		
7	T_PH_ALGN	0	0	Phase alignment timer
6		0		
5		0		
4		0		
3		0	4	
2		1		
1		0		
0		0		

CFG6 (05h) - Start-up Timer

#	Bit Name	Default		Function
15	SU_WAIT	0	0	Crystal oscillator settling timer.
14		0		
13		0		
12		0		
11		0	1	
10		0		
9		0		
8		1		
7		0	0	
6		0		
5		0		
4		0		
3		0	0	
2		0		
1		0		
0		0		

PLL1x0 (80h) - VCO, LO Divider and Calibration Select

#	Bit Name	Default		Function
15	P1_VCOSEL	0	7	Path 1 VCO band select: 00=VCO1, 01=VCO2, 10=VCO3, 11=Reserved
14		1		
13	P1_CT_EN	1		Path 1 VCO coarse tune: 00=disabled, 11=enabled
12		1		
11	P1_KV_EN	0	1	Path 1 VCO tuning gain calibration: 00=disabled, 11=enabled
10		0		
9	P1_LODIV	0		Path 1 local oscillator divider: 00=divide by 1, 01=divide by 2, 10=divide by 4, 11=reserved
8		1		
7		0	1	
6		0		
5	P1_CP_DEF	0		Charge pump current setting If P1_KV_EN=11 this value sets charge pump current during KV compensation only
4		1		
3		1	F	
2		1		
1		1		
0		1		

PLL1x1 (09h) - MSB of Fractional Divider Ratio

#	Bit Name	Default		Function
15	P1_NUM_MSB	0	6	Path 1 VCO divider numerator value, most significant 16 bits
14		1		
13		1		
12		0		
11		0	2	
10		0		
9		1		
8		0		
7		0	7	
6		1		
5		1		
4		1		
3		0	6	
2		1		
1		1		
0		0		

PLL1x2 (0Ah) - LSB of Fractional Divider Ratio and CT Default

#	Bit Name	Default		Function
15	P1_NUM_LSB	0	2	Path 1 VCO divider numerator value, least significant 8 bits
14		0		
13		1		
12		0		
11		0	7	
10		1		
9		1		
8		1		
7	P1_CT_DEF	0	7	Path 1 VCO coarse tuning value, used when P1_CT_EN=00
6		1		
5		1		
4		1		
3		1	E	
2		1		
1		1		
0		0		

PLL1x3 (0Bh) - Integer Divider Ratio and VCO Current

#	Bit Name	Default		Function
15	P1_N	0	2	Path 1 VCO divider integer value
14		0		
13		1		
12		0		
11		0	3	
10		0		
9		1		
8		1		
7		0	0	
6		0		
5		0		
4		0		
3		0	2	
2		0		Path 1 VCO bias setting: 000=minimum value, 111=maximum value
1		1		
0		0		

PLL1x4 (0Ch) - Calibration Settings

#	Bit Name	Default		Function
15	P1_DN	0	1	Path 1 frequency step size used in VCO tuning gain calibration
14		0		
13		0		
12		1		
11		0	7	
10		1		
9		1		
8		1		
7		1	E	
6	P1_CT_GAIN	1		Path 1 coarse tuning calibration gain
5		1		
4		0		
3	P1_KV_GAIN	0	4	Path 1 VCO tuning gain calibration gain
2		1		
1		0		
0		0		

PLL1x5 (0Dh) - More Calibration Settings

#	Bit Name	Default		Function
15	P1_N_PHS_ADJ	0	0	Path 1 frequency step size used in VCO tuning gain calibration
14		0		
13		0		
12		0		
11		0	0	
10		0		
9		0		
8		0		
7		0	1	
6		0		
5		0		
4	P1_CT_V	1		Path 1 course tuning voltage setting when performing course tuning calibration.
3		0	0	
2		0		
1		0		
0		0		

PLL2x0 (10h) - VCO, LO Divider and Calibration Select

#	Bit Name	Default		Function
15	P2_VCOSEL	0	7	Path 2 VCO band select: 00=VCO1,
14		1		
13	P2_CT_EN	1		Path 2 VCO coarse tune: 00=disabled, 11=enabled
12		1		
11	P2_KV_EN	0	1	Path 2 VCO tuning gain calibration: 00=disabled, 11=enabled
10		0		
9	P2_LODIV	0		Path 2 local oscillator divider: 00=divide by 1, 01=divide by 2, 10=divide by 4, 11=reserved
8		1		
7			1	
6				
5	P2_CP_DEF	0		Charge pump current setting. If P2_KV_EN=11 this value sets charge pump current during KV compensation only
4		1		
3		1	F	
2		1		
1		1		
0		1		

PLL2x1 (11h) - MSB of Fractional Divider Ratio

#	Bit Name	Default		Function
15	P2_NUM_MSB	0	6	Path 2 VCO divider numerator value, most significant 16 bits
14		1		
13		1		
12		0		
11		0	2	
10		0		
9		1		
8		0		
7		0	7	
6		1		
5		1		
4		1		
3		0	6	
2		1		
1		1		
0		0		

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PLL2x1 (12h) - LSB of Fractional Divider Ratio and CT Default

#	Bit Name	Default		Function
15	P2_NUM_LSB	0	2	Path 2 VCO divider numerator value, least significant 8 bits.
14		0		
13		1		
12		0		
11		0	7	
10		1		
9		1		
8		1		
7	P2_CT_DEF	0	7	Path 2 VCO coarse tuning value, used when P1_CT_EN=00
6		1		
5		1		
4		1		
3		1	E	
2		1		
1		1		
0		0		

PLL2x3 (13h) - Integer Divider Ratio and VCO Current

#	Bit Name	Default		Function
15	P2_N	0	2	Path 2 VCO divider integer value
14		0		
13		1		
12		0		
11		0	3	
10		0		
9		1		
8		1		
7		0	0	
6		0		
5		0		
4		0		
3		0	2	
2	P2_VCOI	0		Path 1 VCO bias setting: 000=minimum value, 111=maximum value
1		1		
0		0		

PLL2x4 (14h) - Calibration Settings

#	Bit Name	Default		Function
15	P2_DN	0	1	Path 2 frequency step size used in VCO tuning gain calibration
14		0		
13		0		
12		1		
11		0	7	
10		1		
9		1		
8		1		
7		1	E	
6	P2_CT_GAIN	1		Path 2 coarse tuning calibration gain
5		1		
4		0		
3	P2_KV_GAIN	0	4	Path 2 VCO tuning gain calibration gain
2		1		
1		0		
0		0		

PLL2x5 (15h) - More Calibration Settings

#	Bit Name	Default		Function
15	P2_N_PHS_ADJ	0	0	Path 2 synthesizer phase adjustment
14		0		
13		0		
12		0		
11		0	0	
10		0		
9		0		
8		0		
7		0	1	
6		0		
5		0		
4	P2_CT_V	1		Path 2 course tuning voltage setting when performing course tuning calibration
3		0	0	
2		0		
1		0		
0		0		

GPO (18h) - Internal Control Output Settings

#	Bit Name	Default		Function
15		0	0	
14	P1_GPO1	0		Setting of GPO1 when path 1 is active, used internally only
13		0		
12	P1_GPO3	0		Setting of GPO3 when path 1 is active, used internally only
11	P1_GPO4	0	0	Setting of GPO4 when path 1 is active, used internally only
10		0		
9		0		
8		0		
7		0	0	
6	P2_GPO1	0		Setting of GPO1 when path 2 is active, used internally only
5		0		
4	P2_GPO3	0		Setting of GPO3 when path 2 is active, used internally only
3	P2_GPO4	0	0	Setting of GPO4 when path 2 is active, used internally only
2		0		
1		0		
0		0		

CHIPREV (19h) - Chip Revision Information

#	Bit Name	Default		Function
15	PARTNO	0	0	RFMD Part number for device
14		0		
13		0		
12		0		
11		0	0	
10		0		
9		0		
8		0		
7	REVNO	X	X	Part revision number
6		X		
5		X		
4		X		
3		X	X	
2		X		
1		X		
0		X		

RB1 (1Ch) - PLL Lock and Calibration Results Read-back

#	Bit Name	Default		Function
15	LOCK	X	X	PLL lock detector, 0=PLL locked, 1=PLL unlocked
14	CT_CAL	X		CT setting (either result of course tune calibration, or CT_DEF, depending on state of CT_EN). Also depends on the MODE of the device
13		X		
12		X		
11		X	X	
10		X		
9		X		
8		X		
7	CP_CAL	X	X	CP setting (either result of KV cal, or CP_DEF, depending on state of KV_EN). Also depends on the MODE of the device
6		X		
5		X		
4		X		
3		X	X	
2		X		
1		0		
0		0		

RB2 (1Dh) - Calibration Results Read-Back

#	Bit Name	Default		Function
15	VO_CAL	X	X	The VCO voltage measured at the start of a VCO gain calibration
14		X		
13		X		
12		X		
11		X	X	
10		X		
9		X		
8		X		
7	V1_CAL	X	X	The VCO voltage measured at the end of a VCO gain calibration
6		X		
5		X		
4		X		
3		X	X	
2		X		
1		X		
0		X		

RB3 (1Eh) - PLL state Read-Back

#	Bit Name	Default		Function
15	RSM_STATE	X	X	State of the radio state machine
14		X		
13		X		
12		X		
11		X	X	
10		X		
9		0		
8		0		
7		0	0	
6		0		
5		0		
4		0		
3		0	0	
2		0		
1		0		
0		0		

TEST (1Fh) - Test Modes

#	Bit Name	Default		Function
15	TEN	0	0	Enables test mode
14	TMUX	0		Sets test multiplexer state
13		0		
12		0		
11	CPU	0	0	Set charge pump to pump up, 0=normal operation 1=pump down
10	CPD	0		Set charge pump to pump down, 0=normal operation 1=pump down
9	FNZ	0		0=normal operation, 1=fractional divider modulator disabled
8	LDO_BYP	0		On chip low drop out regulator bypassed
7	TSEL	0	0	
6		0		
5		0		
4	DACTEST	0		DAC test
3		0	0	
2		0		
1		0		
0		0		

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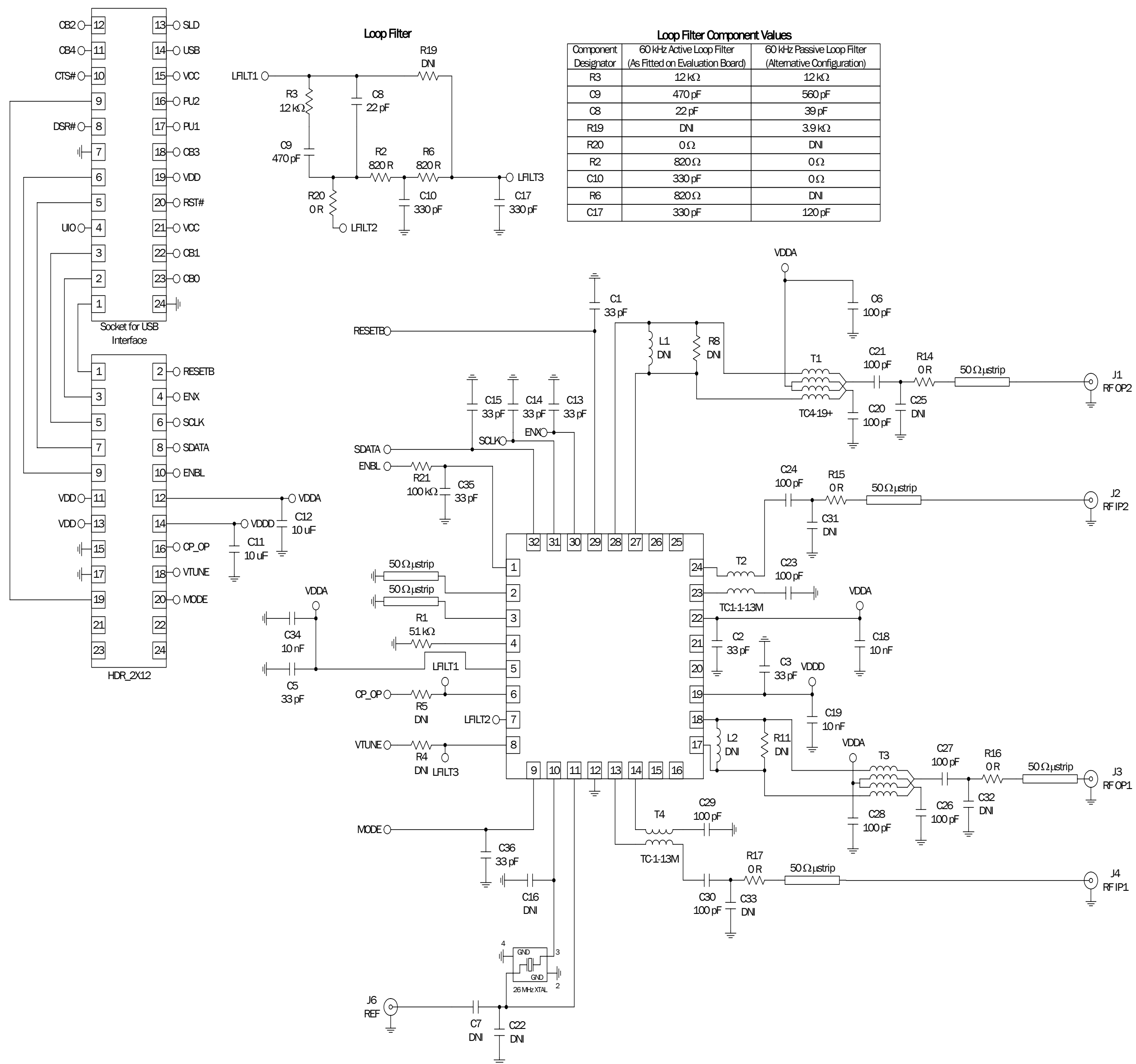
Evaluation Board

The following diagrams show the schematic and PCB layout of the RF2051 evaluation board.The standard evaluation board has been configured for wideband operation. Application notes have been produced showing how the device is matched and on balun implementations for narrowband applications. The evaluation board is provided as part of a design kit (DK2051), along with the necessary cables and programming software tool to enable full evaluation of the RF2051.

Evaluation Board Schematic



Loop Filter Component Values

Component Designator	60 kHz Active Loop Filter (As Fitted on Evaluation Board)	60 kHz Passive Loop Filter (Alternative Configuration)
R3	12 kΩ	12 kΩ
C9	470 pF	560 pF
C8	22 pF	39 pF
R19	DNI	3.9 kΩ
R20	0 Ω	DNI
R2	820 Ω	0 Ω
C10	330 pF	0 Ω
R6	820 Ω	DNI
C17	330 pF	120 pF

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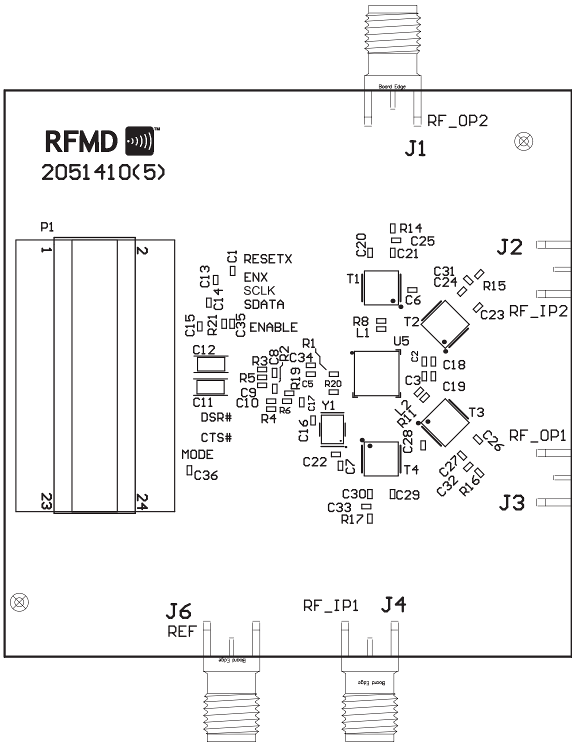
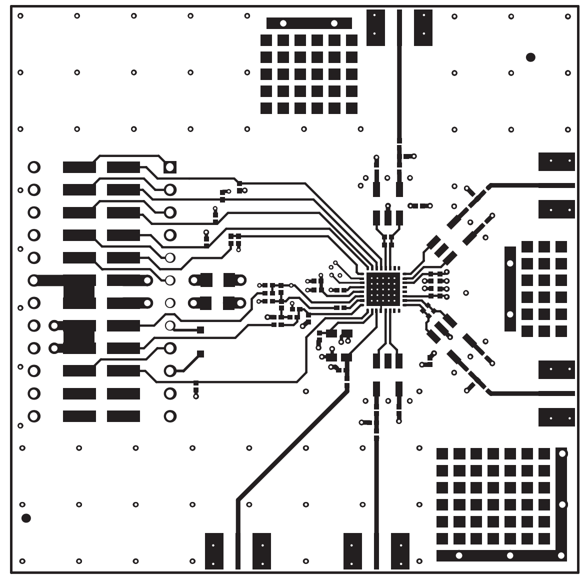
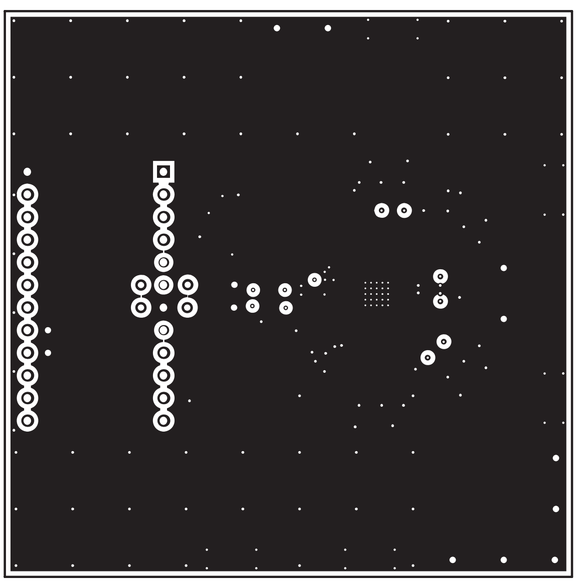
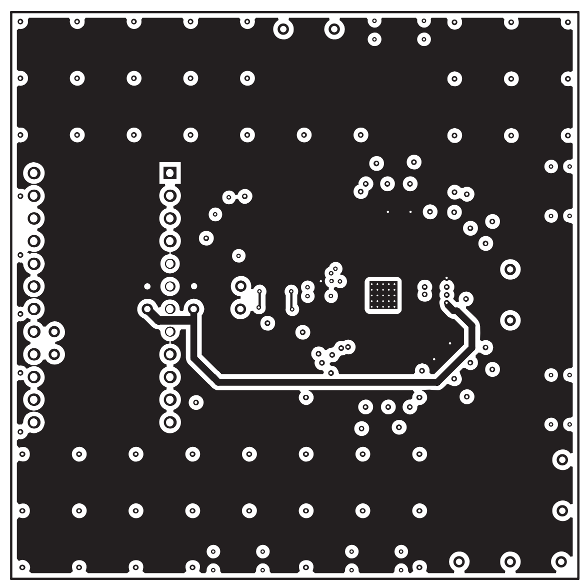
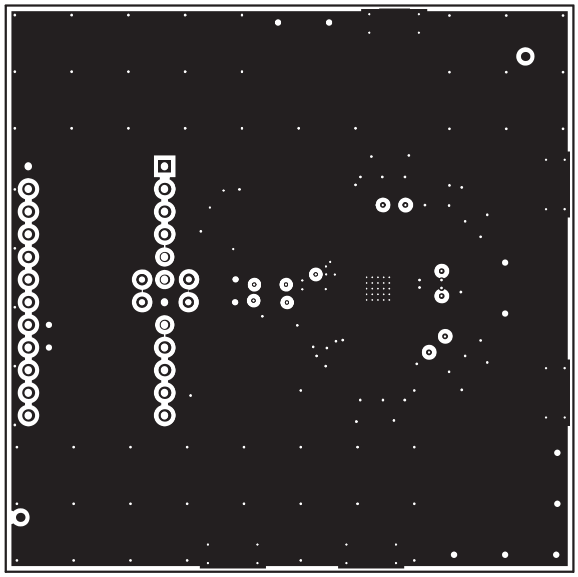
Evaluation Board Layout
Board Size 2.5"x2.5"
Board Thickness 0.040", Board Material FR-4



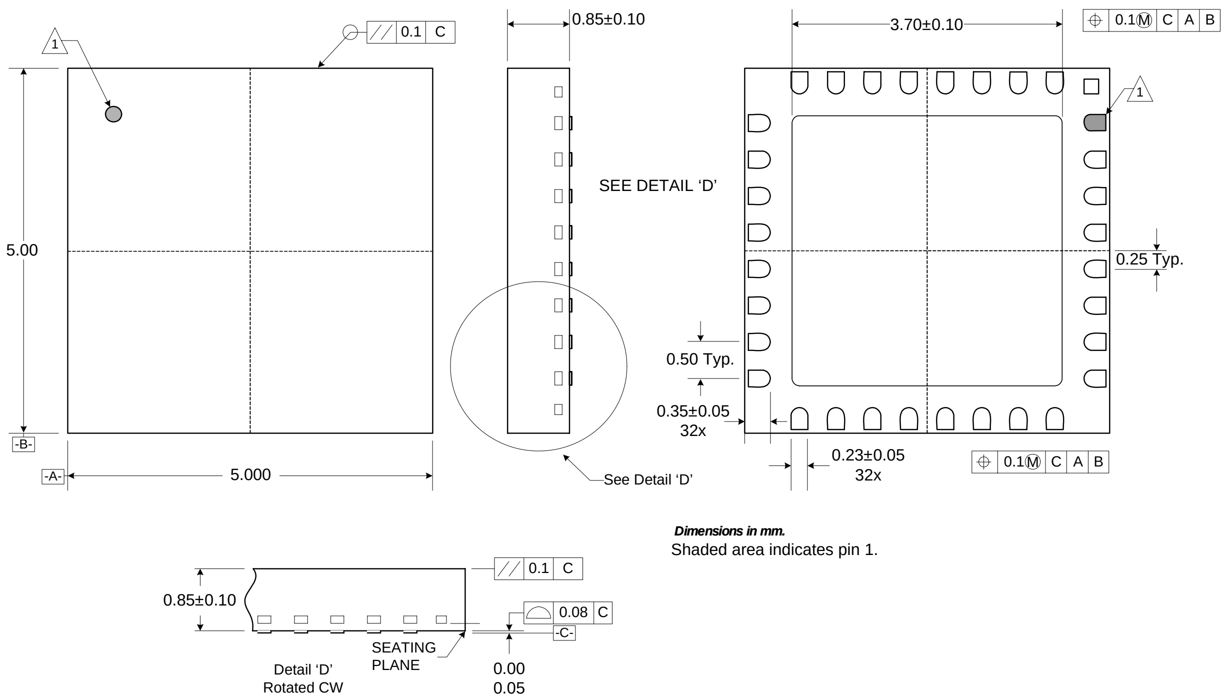








Package Drawing
QFN, 32-Pin, 5mmx5mm



Support and Applications Information

Application notes and support material can be downloaded from the product web page: www.rfmd.com/rf205x.

Ordering Information

Part Number	Package	Quantity
RF2051	32-Pin QFN	25pcs sample bag
RF2051SB	32-Pin QFN	5pcs sample bag
RF2051SR	32-Pin QFN	100pcs reel
RF2051TR7	32-Pin QFN	750pcs reel
RF2051TR13	32-Pin QFN	2500pcs reel
DK2051	Complete Design Kit	1 box