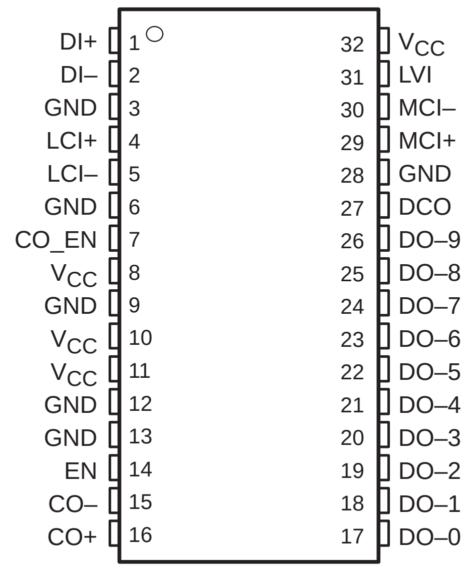
- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Supports Deserialization of One Serial Link Data Channel Input at Rates up to 200 Mbps**
- **PLL Lock/Valid Input Provided to Enable Parallel Data and Clock Outputs**
- **Cascadable With Additional SN65LVDS152 MuxIt Receiver–Deserializers for Wider Parallel Output Data Channel Widths**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI TIA/EIA-644-A**
- **LVDS Input and Output ESD Protection Exceeds 12 kV HBM**
- **LVTTL Compatible Inputs for Lock/Valid and Enables Are 5-V Tolerant**
- **Operates With 3.3-V Supply**
- **Packaged in 32-Pin DA Thin Shrink Small-Outline Package With 26-Mil Terminal Pitch**

SN65LVDS152DA
(Marked as 65LVDS152)
(TOP VIEW)



description

MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user selectable, allowing for higher transmission efficiencies than with other existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644-A) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications: the SN65LVDS150 phase locked loop frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

The SN65LVDS152 consists of three LVDS differential transmission line receivers, an LVDS differential transmission line driver, a 10-bit serial-in/parallel-out shift register, plus associated input and output buffers. It receives serialized data over an LVDS transmission line link, deserializes (demultiplexes) it, and delivers it on parallel data outputs, DO–0 through DO–9. Data received over the link is clocked at a factor of M times the original parallel data frequency. The multiplexing ratio M, or number of bits per data clock cycle, is programmed with configuration pins (M1 → M5) on the companion SN65LVDS150 MuxIt programmable PLL frequency multiplier. Up to 10 bits of data may be deserialized and output by each SN65LVDS152. Two or more SN65LVDS152 units may be connected in series (cascaded) to accommodate wider parallel data paths for higher serialization values. The range of multiplexing ratio M supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier is between 4 and 40**.** Table 1 shows some of the combinations of LCI and MCI supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier.

description (continued)

Data is serially shifted into the SN65LVDS152 shift register on the falling edges of the M-clock input (MCI). The data is latched out in parallel from the SN65LVDS152 shift register on the second rising edge after the first falling edge of the M-clock following a rising edge of the link clock input (LCI). The SN65LVDS152 includes LVDS differential line receivers for both the serialized link data stream (DI) and link clock (LCI). High-speed signals from the SN65LVDS150 MuxIt programmable frequency multiplier (MCI), plus the input and output for cascaded data (DI, CO) are carried over differential connections to minimize skew and jitter. Examples of operating waveforms for values of M = 4 and M = 10 are provided in Figure 1.

The enable input (EN) along with internal power-on reset (POR) controls the outputs. When Vcc is below 1.5 volts, or when EN is low, outputs are disabled. When V_{CC} is above 3 V and EN is high, outputs are enabled and operating to specifications.

Parallel data bits are output from DO–n outputs in an order dependent on the value of the multiplexing ratio (frequency multiplier value) M. For values of M from 4 through 10, the cascade output (CO+/–) is not used, and only the top M parallel outputs (DO–9 through DO–[10–M]) are used. The data bit output on DO–9 corresponds to the data bit input on DI–[M–1] of the SN65LVDS151 serializer. Likewise, the data bit output on DO–[10–M] will correspond to the data bit input on DI–0 of the SN65LVDS151 serializer.

For values of M greater than 10, the cascade output (CO+/–) is used to connect multiple SN65LVDS152 deserializers. In this case the higher-order unit(s) output 10 bits each of the highest numbered bits that are input into the SN65LVDS151 serializer(s). The lowest numbered input bits are output on the lowest-order SN65LVDS152 deserializer in descending order from output DO–9. The number of bits is equal to M mod(10). Table 2 reflects this information, where X = M mod(10)

Table 1. Example Combinations of LCI and MCI Supported by the SN65LVDS150 MuxIt Programmable PLL Frequency Multiplier

	LCI, MHz		MCI, MHz	
M	MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
4	5	50	20	200
10	5	20	50	200
20	5	10	100	200
40	5	5	200	200

Table 2. Output Data BIts as a Function of Multiplier Value M

	X = 1	X = 2	X = 3	X = 4	X = 5	X = 6	X = 7	X = 8	X = 9	X = 0
DO–9 output bit	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6	DI–7	DI–8	DI–9
DO–8 output bit	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6	DI–7	DI–8
DO–7 output bit	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6	DI–7
DO–6 output bit	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6
DO–5 output bit	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5
DO–4 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4
DO–3 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3
DO–2 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2
DO–1 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1
DO–0 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0

Additional information on output bit ordering in cascaded applications can be found in the MuxIt Application Report.

description (continued)

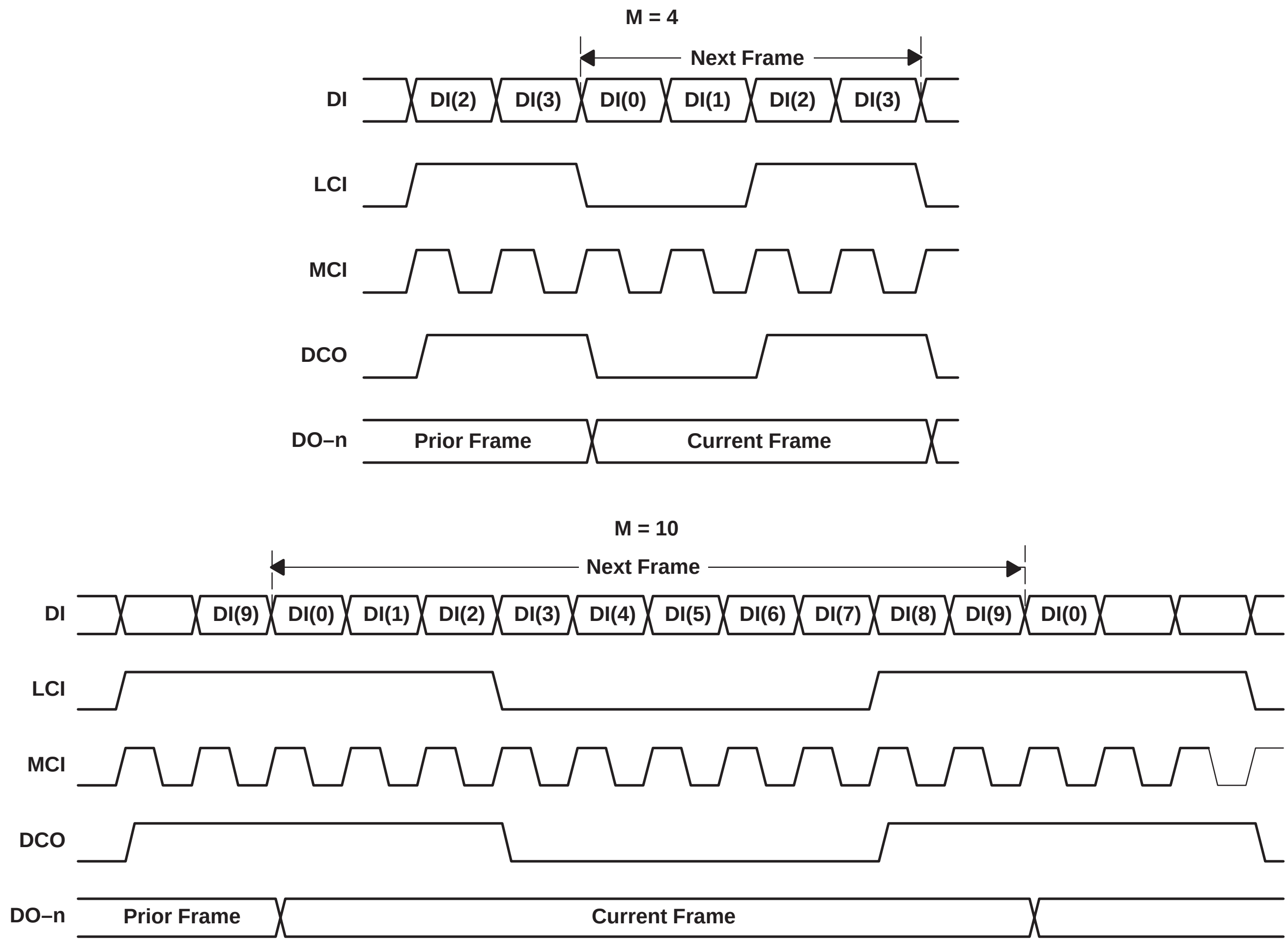
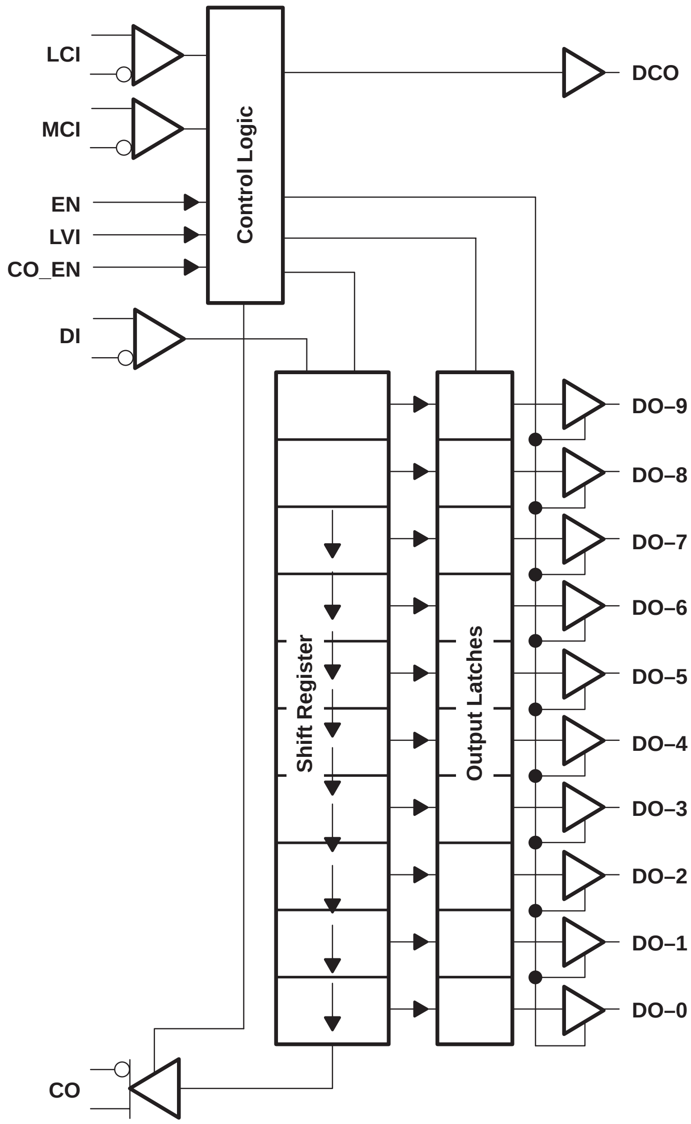
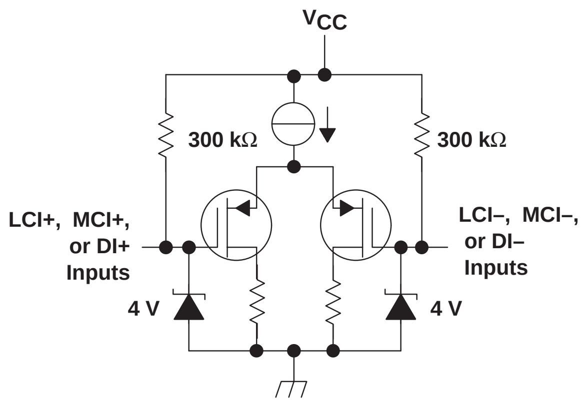


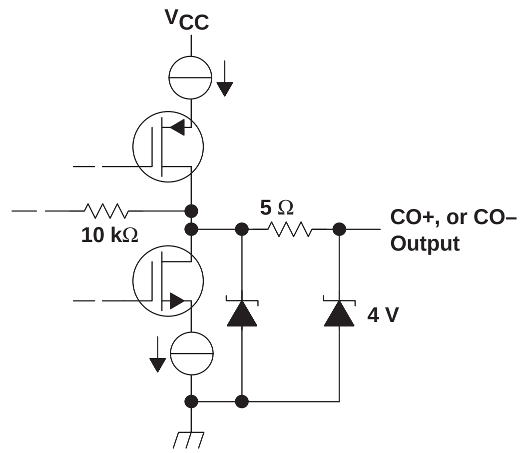
Figure 1. Operating Waveform Examples

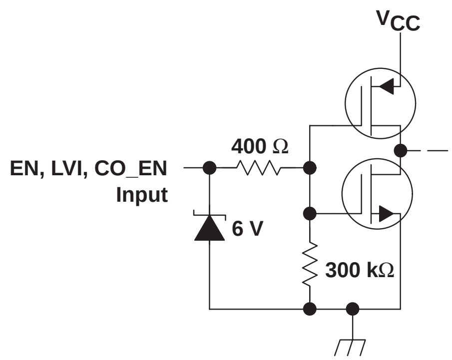
functional block diagram

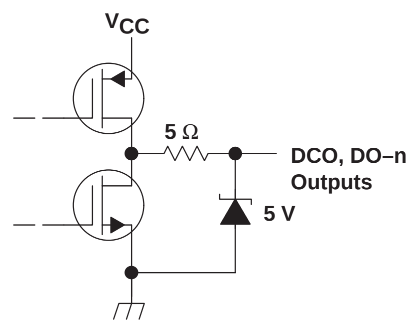


equivalent input and output schematic diagrams









Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	LEVEL	DESCRIPTION
CO–, CO+	15, 16	Output	LVDS	Cascade output. This is used to connect to additional SN65LVDS152 units when the multiplexing ratio M (and M-clock) value is greater than 10.
CO_EN	7	Input	LVTTL	Cascade output enable. Used to control the CO output. A high-level input enables the CO output, a low-level input disables the CO output.
DCO	27	Output	LVTTL	Data clock output. This is the recovered (original frequency) clock that is synchronized to the deserialized parallel data.
DI+, DI–	1, 2	Input	LVDS	Link data input. This is the data being received from the source end of the serialized link. Also used for cascade data input from additional SN65LVDS152 units when the multiplexing ratio M value is greater than 10.
EN	14	Input	LVTTL	Enable. Used to control overall device operation. A high-level input enables the device. A low-level input disables the device by resetting the internal latches and forcing the CO and LVTTL outputs to a high-impedance state.
GND	3, 6, 9, 12, 13, 28	Power	NA	Circuit ground
LCI+, LCI–	4, 5	Input	LVDS	Link clock input. This is the data block synchronization clock received from the source end of the serialized link.
LVI	31	Input	LVTTL	Lock/valid input. This is a signal required for proper MuxIt system operation. It is to be directly connected to the LVO output of an SN65LVDS150. It is used to inhibit the operation of this device until after the PLL has stabilized. A low level input disables the data and clock outputs, a high level input enables the outputs
MCI+, MCI–	29,30	Input	LVDS	M-clock input. This is the high frequency multiplied clock input from the local PLL frequency multiplier. It synchronizes the reception of the link data
DO–0–DO–9	17–26	Output	LVTTL	Parallel data outputs. Data from the serial shift register is transferred to the output data latches in synchronization with the rising edge of LCI.
V_{CC}	8, 10, 11, 32	Power	NA	Supply voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 4 V
Input voltage range: EN, LVI, CO_EN . . . . –0.5 V to 5.5 V
LCI±, MCI±, DI±, CO± . . . . –0.5 V to 4 V
Electrostatic discharge, human body model (see Note 2): LCI±, MCI±, DI±, CO±, and GND . . . . ±12 kV
All pins . . . . ±2 kV
Charged-device model (see Note 3): All pins . . . . ±500 V
Continuous power dissipation . . . . See Dissipation Rating Table
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114–B.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DA	1453 mW	11.6 mW/°C	756 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	EN, LVI, CO_EN	2		V_{CC}	V
Low-level input voltage, V_{IL}	EN, LVI, CO_EN			0.8	V
Magnitude of differential input voltage, $\|V_{ID}\|$	LCI±, MCI±, DI±	0.1		0.6	V
Common-mode input voltage, V_{IC}	LCI±, MCI±, DI±	$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$	V
				$V_{CC} - 0.8$	V
Operating free-air temperature, T_A		–40		85	°C

timing requirements

PARAMETERS		TEST CONDITIONS	MIN	MAX	UNIT
$t_{su(1)}$	Clock setup time, MCI↓ before LCI↑	See Figure 2	0		ns
$t_{su(2)}$	Clock setup time, LCI↑ before MCI↓	See Figure 2	1		ns
$t_{su(3)}$	Link data setup time, DI before MCI↓	See Figure 3	0.3		ns
$t_{h(3)}$	Link data hold time, DI after MCI↓	See Figure 3	0.5		ns

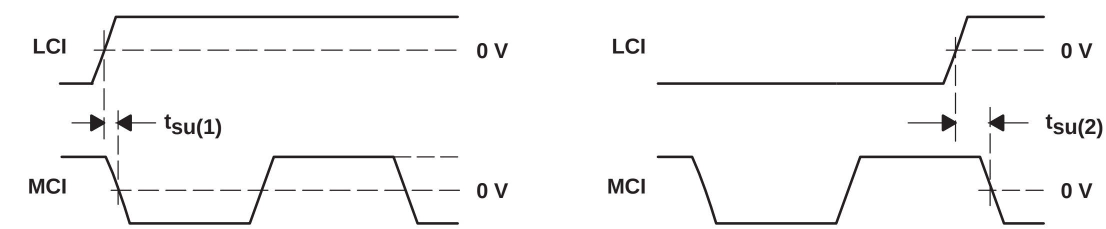


Figure 2

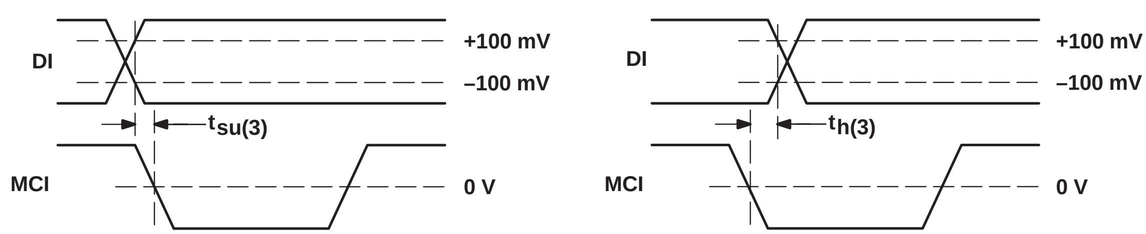


Figure 3. Input Data and M-Clock Setup and Hold Time Waveforms

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold		See Figure 4			100	mV
V_{ITH-}	Negative-going differential input voltage threshold			–100			
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude		R_L = 100 Ω, V_{ID} = ±100 mV, See Figures 5 and 6	247	340	454	mV
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage magnitude between logic states			–50		50	mV
$V_{OC(SS)}$	Steady-stade common-mode output voltage		See Figure 7	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak change common-mode output voltage				50	150	mV
V_{OH}	High-level output voltage	DO-n, DCO	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.4	
I_{CC}	Supply current		Enabled, R_L = 100 Ω,		14	25	mA
			Disabled		0.5	1	
			$f_{(MCI)}$ = 200 MHz, $f_{(LCI)}$ = 20 MHz, R_L = 100 Ω, DI–n= 1010101010 at 200 Mbit/s		35	60	
I_I	Input current	LCI, MCI, DI inputs	V_I = 0 V	–2		–20	µA
			V_I = 2.4 V	–1.2			
I_{ID}	Differential input current	LCI, MCI, DI inputs	V_{IC} = 0.05 V to 2.35 V, V_{ID} = ±0.1 V	–2		2	µA
$I_{I(OFF)}$	Power-off input current	LCI, MCI, DI inputs	V_{CC} = 0 V , V_I = 3.6 V			20	µA
I_{IH}	High-level input current	EN, LVI, CO_EN	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current	EN, LVI, CO_EN	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	CO	V_{O+} or V_{O-} = 0 V	–10		10	mA
			V_{OD} = 0 V	–10		10	mA
I_{OZ}	High-impedance output current	CO	V_O = 0 V or V_{CC}	–5		5	µA
		DO-n, DCO		–5		5	
$I_{O(OFF)}$	Power-off output current	CO	V_{CC} = 1.5 V , V_O = 3.6 V	–5		5	µA
C_I	Input capacitance	LCI, MCI, DI inputs	V_{ID} = (0.4sin(4E6πt) + 0.5) V		3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(1)}$	Propagation delay time, LCI↑ to DCO↑	See Figure 8		2	3	ns
$t_{d(2)}$	Delay time, MCI↑ to DO–n			3.3	5.5	
$t_{su(4)}$	Set-up time, DO-n valid to DCO↑		5			
$t_{h(4)}$	Hold time, DCO↑ to DO-n valid		5			
$t_{d(3)}$	Delay time, MCI↓ to CO	See Figure 9		2.9	4.5	ns
t_r	Differential output signal rise time, CO	R_L = 100 Ω, C_L = 10 pF, See Figure 10	0.3	0.8	1.5	ns
	Output signal rise time, DCO, DO-n	C_L = 10 pF, See Figure 11		0.6	1.5	
t_f	Differential output signal fall time, CO	R_L = 100 Ω, C_L = 10 pF, See Figure 10	0.3	0.8	1.5	ns
	Output signal fall time, DCO, DO-n	C_L = 10 pF, See Figure 11		0.6	1.5	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$), CO	R_L = 100 Ω, C_L = 10 pF, See Figure 10		0	300	ps
t_{PZH}	Propagation delay time, high-impedance to high-level output (DCO only)	EN to DCO, DO-n, C_L = 10 pF, See Figure 12		5	15	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output			5	15	
t_{PHZ}	Propagation delay time, high-level to high-impedance output			5	15	
t_{PLZ}	Propagation delay time, low-level to high-impedance output			6	15	
t_{PZH}	Propagation delay time, high-impedance to high-level output (DCO only)	LVI to DCO, DO-n C_L = 10 pF, See Figure 12		5	15	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output			5	15	
t_{PHZ}	Propagation delay time, high-level to high-impedance output			5	15	
t_{PLZ}	Propagation delay time, low-level to high-impedance output			5	15	

PARAMETER MEASUREMENT INFORMATION

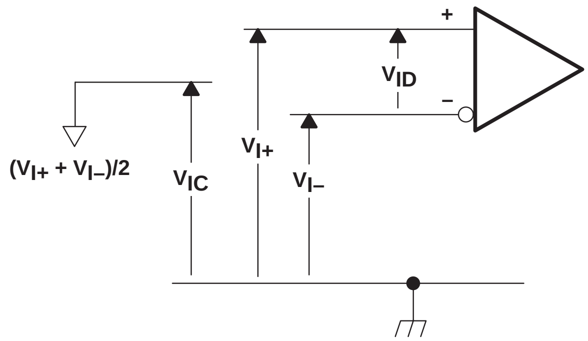


Figure 4. Receiver Voltage Definitions

Table 3. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{I+}	V_{I-}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

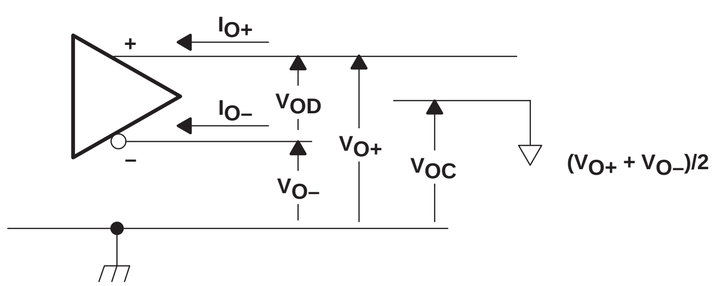


Figure 5. Driver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION

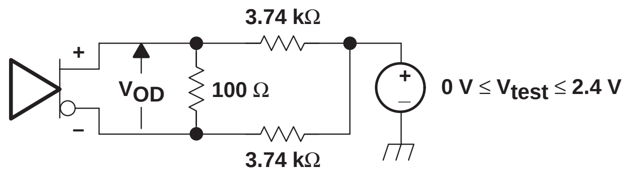
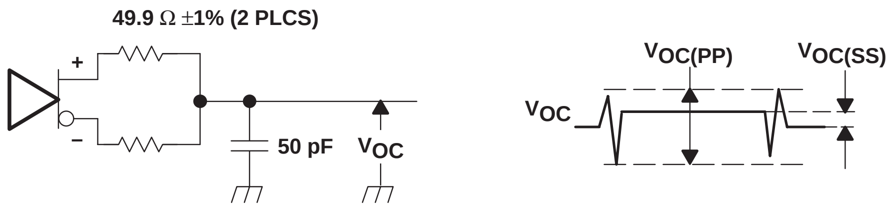


Figure 6. V_{OD} Test Circuit



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 5 GHz.

Figure 7. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

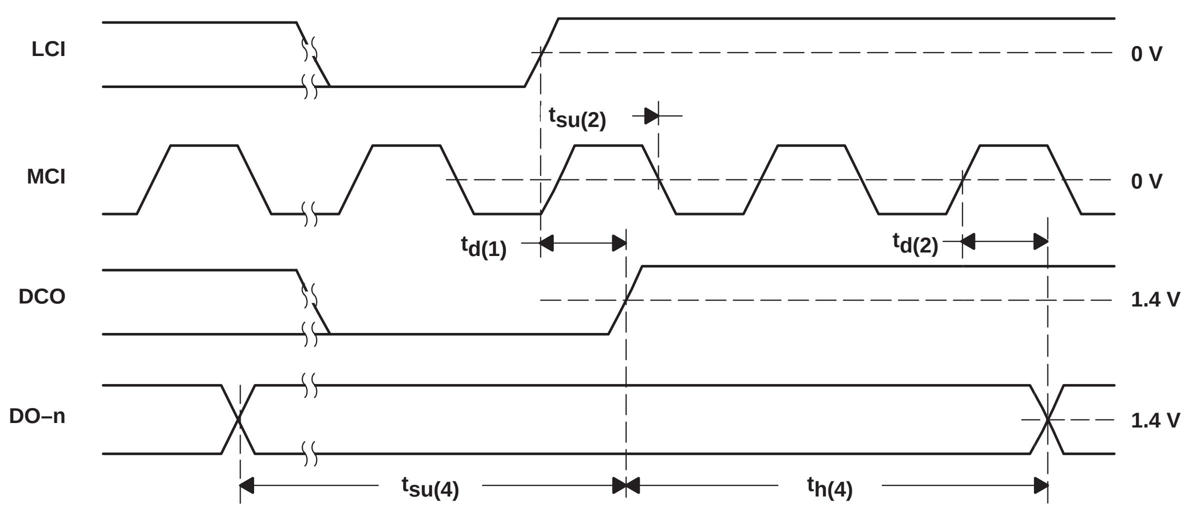


Figure 8. Data Clock and Data Output Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

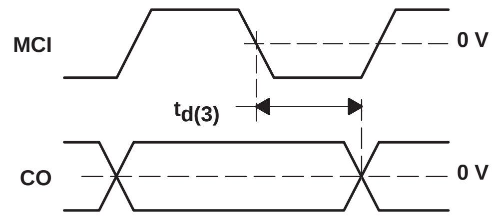
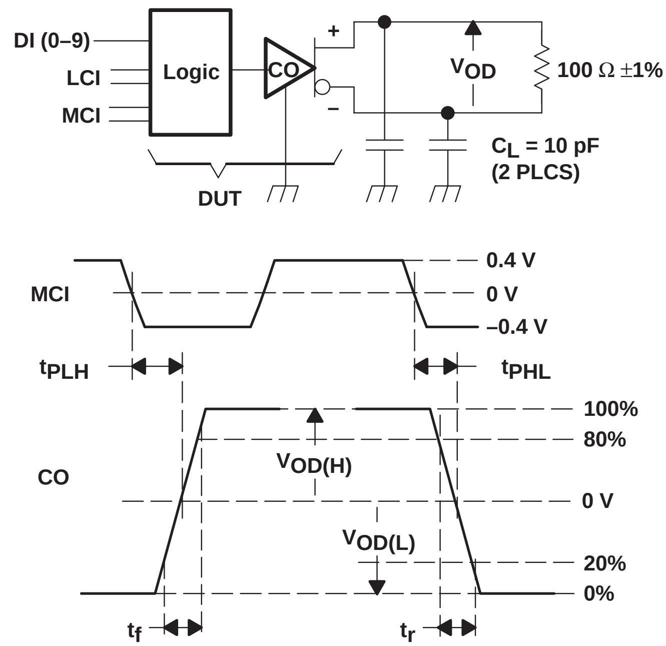
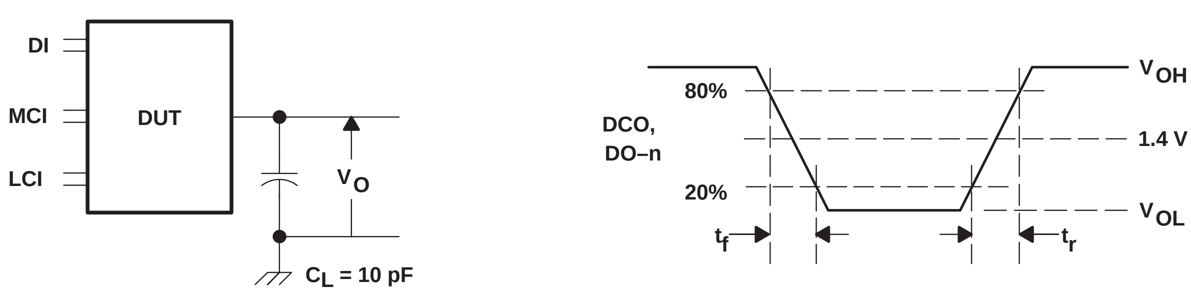


Figure 9. MCI to CO Timing Waveforms



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 100 Mpps, Pulse width = 5 ± 0.1 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

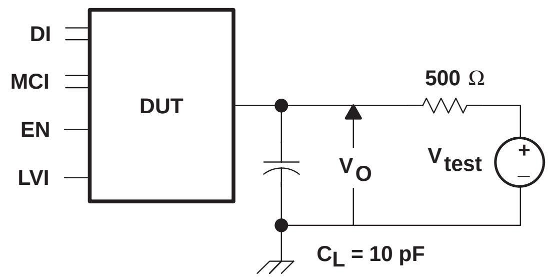
Figure 10. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



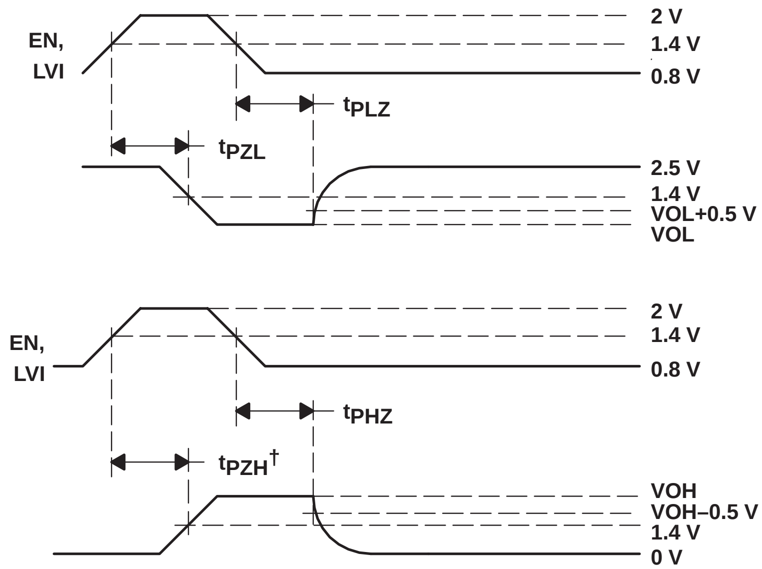
NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, MCI pulse repetition rate (PRR) = 50 Mpps, Pulse width = 10 ± 0.2 ns . LCI pulse repetition rate (PRR) = 5 Mpps, pulsewidth = 100 ±2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 11. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: V_{TEST} = 2.5 V for t_{PZL} or t_{PLZ}, V_{TEST} = 0 V for t_{PZH} or t_{PHZ}. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.



† DCO only

Figure 12. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

**AVERAGE SUPPLY CURRENT
vs
FREQUENCY**

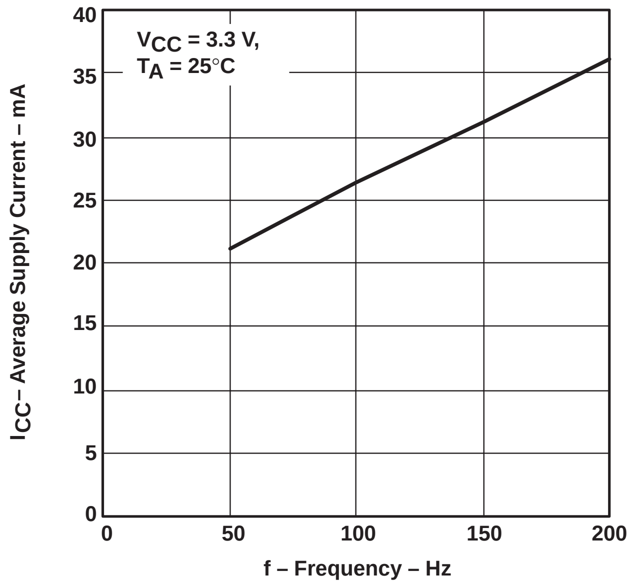
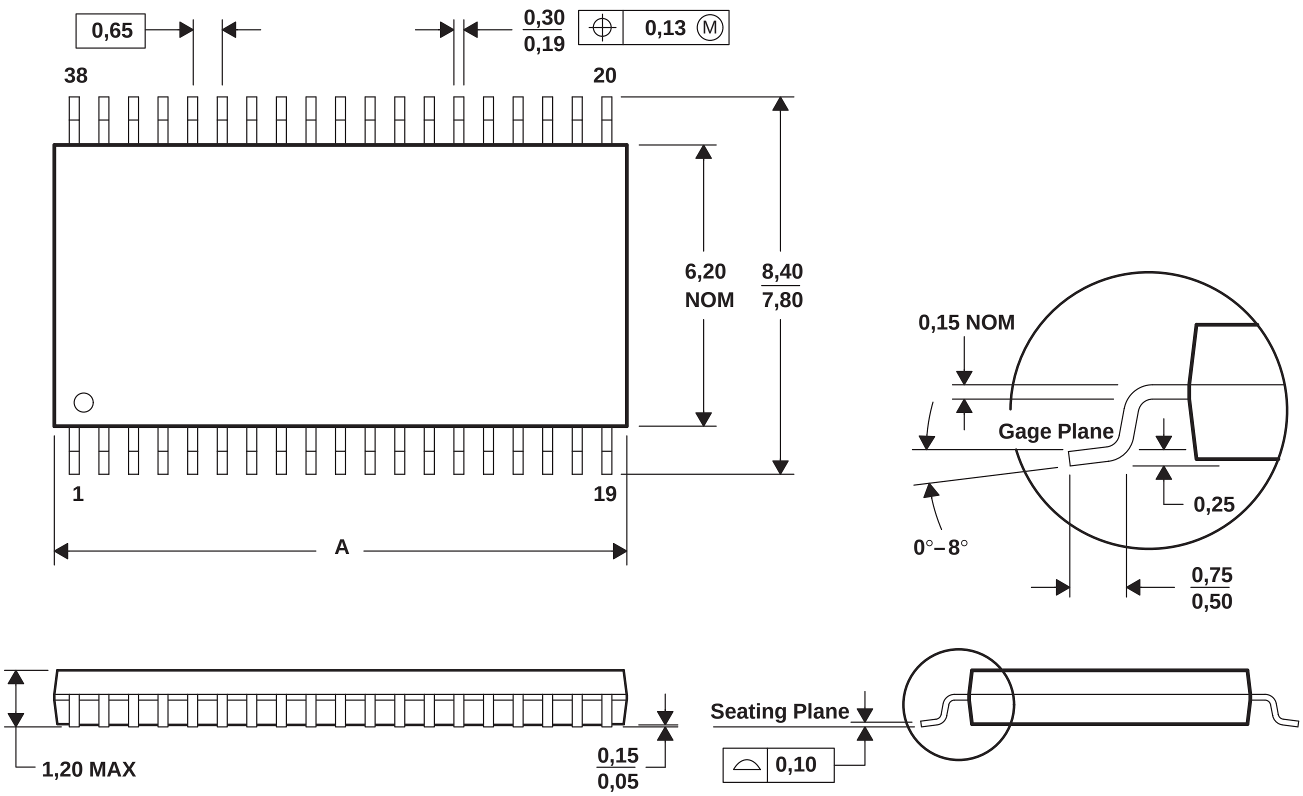


Figure 13. Average Supply Current vs Frequency

MECHANICAL DATA

DA (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

38 PINS SHOWN



PINS ** / DIM	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

4040066 / D 11/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153