

NC7SB3157, FSA3157

Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

Features

- Useful in both analog and digital applications
- Space-saving, SC70 6-lead surface mount package
- Ultra-small, MicroPak™ Pb-free leadless package
- Low On Resistance: <math><10\Omega</math> on typical at 3.3V V_{CC}
- Broad V_{CC} operating range: 1.65V to 5.5V
- Rail-to-rail signal handling
- Power-down, high-impedance control input
- Over-voltage tolerance of control input to 7.0V
- Break-before-make enable circuitry
- 250 MHz, 3dB bandwidth

General Description

The NC7SB3157 / FSA3157 is a high-performance, single-pole / double-throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The control input tolerates voltages up to 5.5V, independent of the V_{CC} operating range.

Ordering Information

Part Number	Top Mark	Pb-Free	Package Description	Packing Method
NC7SB3157P6X	B7A	Yes	6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package	3000 Units on Tape and Reel
NC7SB3157L6X	BB	Yes	6-Lead, MicroPak 1.0mm Wide Package	5000 Units on Tape and Reel
FSA3157P6X	B7A	Yes	6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package	3000 Units on Tape and Reel
FSA3157L6X	BB	Yes	6-Lead, MicroPak 1.0mm Wide Package	5000 Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Logic Symbol

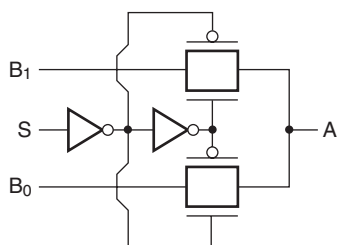
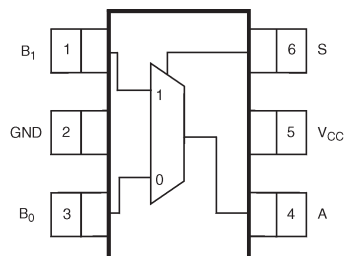


Figure 1. Logic Symbol

Connection Diagrams



2. Pin Assignments SC70

Analog Symbol

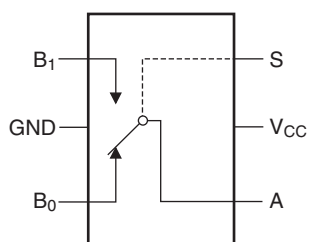


Figure 3. Analog Symbol

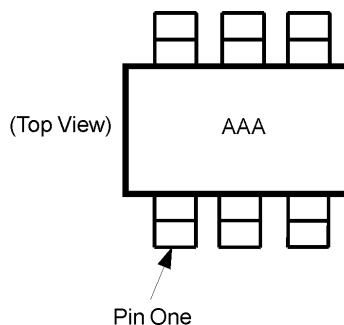


Figure 4. Pin One Orientation

Function Table

Input (S)	Function
Logic Level Low	B ₀ Connected to A
Logic Level High	B ₁ Connected to A

Note:

Orientation of top mark determines pin one location. Read the top product code mark left to right and pin one is the lower left pin (see Figure 4).

Pin Descriptions

Pin Names	Description
A, B ₀ , B ₁	Data Ports
S	Control Input

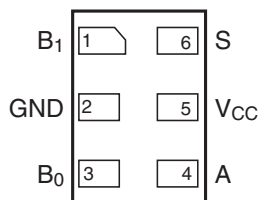


Figure 5. Pad Assignments for MicroPak™

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
V_S	DC Switch Voltage ⁽¹⁾	-0.5V to $V_{CC} + 0.5V$
V_{IN}	DC Input Voltage ⁽¹⁾	-0.5V to +7.0V
I_{IK}	DC Input Diode Current at $V_{IN} < 0V$	-50mA
I_{OUT}	DC Output Current	128mA
I_{CC}/I_{GND}	DC V_{CC} or Ground Current	$\pm 100mA$
T_{STG}	Storage Temperature Range	-65°C to +150°C
T_J	Junction Temperature Under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation at +85°C	180mW
ESD	Electrostatic Discharge, Human Body Model	4000V

Note:

- The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	
V_{CC}	Supply Voltage Operating	1.65V to 5.5V	
V_{IN}	Control Input Voltage ⁽²⁾	0V to V_{CC}	
V_{IN}	Switch Input Voltage ⁽²⁾	0V to V_{CC}	
V_{OUT}	Output Voltage ⁽²⁾	0V to V_{CC}	
T_A	Operating Temperature	-40°C to +85°C	
t_r, t_f	Input Rise and Fall Time	Control Input $V_{CC} = 2.3V-3.6V$	0ns/V to 10ns/V
		Control Input $V_{CC} = 4.5V-5.5V$	0ns/V to 5ns/V
θ_{JA}	Thermal Resistance	350°C/W	

Note:

- Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage		1.65 – 1.95	0.75 V _{CC}			0.75 V _{CC}		V
			2.3 – 5.5	0.7 V _{CC}			0.7 V _{CC}		
V _{IL}	Low Level Input Voltage		1.65 – 1.95			0.25 V _{CC}		0.25 V _{CC}	V
			2.3 – 5.5			0.3 V _{CC}		0.3 V _{CC}	
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5V	0 – 5.5		±0.05	±0.1		±1	μA
I _{OFF}	Off State Leakage Current	0 ≤ A, B ≤ V _{CC}	1.65 – 5.5		±0.05	±0.1		±1	μA
R _{ON}	Switch On Resistance ⁽³⁾	V _{IN} = 0V, I _O = 30mA	4.5		3.0	7.0		7.0	Ω
		V _{IN} = 2.4V, I _O = -30mA			5.0	12.0		12.0	
		V _{IN} = 4.5V, I _O = -30mA		7.0	15.0		15.0		
		V _{IN} = 0V, I _O = 24mA	3.0		4.0	9.0		9.0	
		V _{IN} = 3V, I _O = -24mA			10.0	20.0		20.0	
		V _{IN} = 0V, I _O = 8mA	2.3		5.0	12.0		12.0	
		V _{IN} = 2.3V, I _O = -8mA			13.0	30.0		30.0	
		V _{IN} = 0V, I _O = 4mA	1.65		6.5	20.0		20.0	
V _{IN} = 1.65V, I _O = -4mA		17.0		50.0		50.0			
I _{CC}	Quiescent Supply Current; All Channels On or Off	V _{IN} = V _{CC} or GND I _{OUT} = 0	5.5			1		10	μA
	Analog Signal Range		V _{CC}	0		V _{CC}	0	V _{CC}	V
R _{RANGE}	On Resistance Over Signal Range ^(3, 7)	I _A = -30mA, 0 ≤ V _{Bn} ≤ V _{CC}	4.5					25.0	Ω
		I _A = -24mA, 0 ≤ V _{Bn} ≤ V _{CC}	3.0					50.0	
		I _A = -8mA, 0 ≤ V _{Bn} ≤ V _{CC}	2.3					100	
		I _A = -4mA, 0 ≤ V _{Bn} ≤ V _{CC}	1.65					300	
ΔR _{ON}	On Resistance Match Between-Channels ^(3, 4, 4)	I _A = -30mA, V _{Bn} = 3.15	4.5		0.15				Ω
		I _A = -24mA, V _{Bn} = 2.1	3.0		0.2				
		I _A = -8mA, V _{Bn} = 1.6	2.3		0.5				
		I _A = -4mA, V _{Bn} = 1.15	1.65		0.50				
R _{flat}	On Resistance Flatness ^(3, 4, 6)	I _A = -30mA, 0 ≤ V _{Bn} ≤ V _{CC}	5.0		6.0				Ω
		I _A = -24mA, 0 ≤ V _{Bn} ≤ V _{CC}	3.3		12.0				
		I _A = -8mA, 0 ≤ V _{Bn} ≤ V _{CC}	2.5		28.0				
		I _A = -4mA, 0 ≤ V _{Bn} ≤ V _{CC}	1.8		125				

Notes:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized, but not tested in production.
5. ΔR_{ON} = R_{ON} max – R_{ON} minimum measured at identical V_{CC}, temperature, and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
7. Guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t _{PHL} , t _{PLH}	Propagation Delay Bus-to-Bus ⁽⁸⁾	V _I = OPEN	1.65 – 1.95			3.5		3.5	ns	Figure 12 Figure 13
			2.3 – 2.7			1.2		1.2		
			3.0 – 3.6			0.8		0.8		
			4.5 – 5.5			0.3		0.3		
t _{PZL} , t _{PZH}	Output Enable Time Turn-On Time (A to B _n)	V _I = 2 x V _{CC} for t _{PZL} V _I = 0V for t _{PZH}	1.65 – 1.95	7.0		23.0	7.0	24.0	ns	Figure 12 Figure 13
			2.3 – 2.7	3.5		13.0	3.5	14.0		
			3.0 – 3.6	2.5		6.9	2.5	7.6		
			4.5 – 5.5	1.7		5.2	1.7	5.7		
t _{PLZ} , t _{PHZ}	Output Disable Time Turn-Off Time (A Port to B Port)	V _I = 2 x V _{CC} for t _{PLZ} V _I = 0V for t _{PHZ}	1.65 – 1.95	3.0		12.5	3.0	13.0	ns	Figure 12 Figure 13
			2.3 – 2.7	2.0		7.0	2.0	7.5		
			3.0 – 3.6	1.5		5.0	1.5	5.3		
			4.5 – 5.5	0.8		3.5	0.8	3.8		
t _{B-M}	Break-Before-Make Time ⁽⁹⁾		1.65 – 1.95	0.5			0.5		ns	Figure 14
			2.3 – 2.7	0.5			0.5			
			3.0 – 3.6	0.5			0.5			
			4.5 – 5.5	0.5			0.5			
Q	Charge Injection ⁽⁹⁾	C _L = 0.1nF, V _{GEN} = 0V,	5.0		7.0			pC	Figure 15	
		R _{GEN} = 0Ω	3.3		3.0					
OIRR	Off Isolation ⁽¹⁰⁾	R _L = 50Ω, f = 10MHz	1.65 – 5.5		-57.0			dB	Figure 16	
Xtalk	Crosstalk	R _L = 50Ω, f = 10MHz	1.65 – 5.5		-54.0			dB	Figure 17	
BW	-3dB Bandwidth	R _L = 50Ω	1.65 – 5.5		250			MHz	Figure 20	
THD	Total Harmonic Distortion ⁽⁹⁾	R _L = 600Ω, 0.5 V _{PP} , f = 600 Hz to 20 KHz	5.0		.011			%		

Notes:

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).
9. Guaranteed by design.
10. Off Isolation = 20 log₁₀ [V_A / V_{Bn}].

Capacitance

T_A = +25°C, f = 1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typ.	Max.	Units	Figure Number
C _{IN}	Control Pin Input Capacitance	V _{CC} = 0V	2.3		pF	
C _{IO-B}	B Port Off Capacitance	V _{CC} = 5.0V	6.5		pF	Figure 18
C _{IOA-ON}	A Port Capacitance When Switch Is Enabled	V _{CC} = 5.0V	18.5		pF	Figure 19

Typical Characteristics

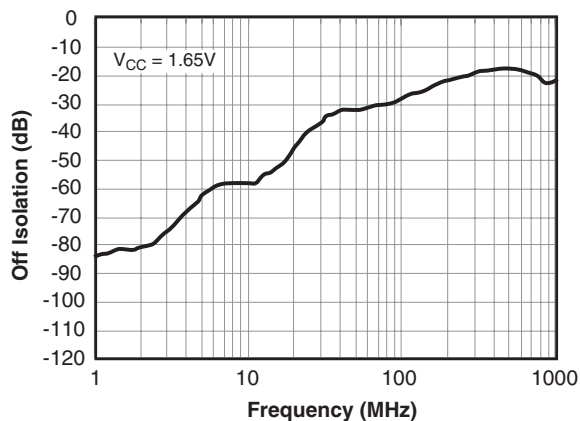


Figure 6. Off Isolation, $V_{CC} = 1.65V$

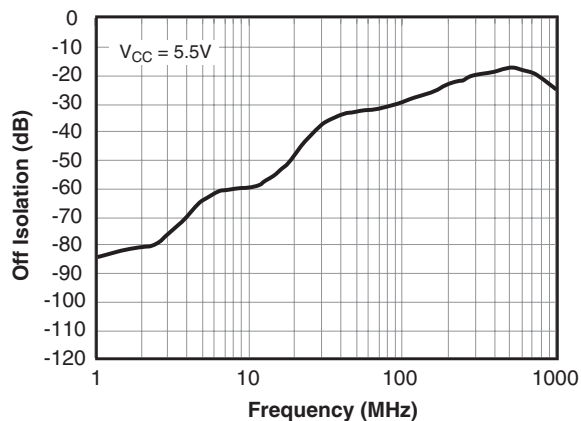


Figure 7. Off Isolation, $V_{CC} = 5.5V$

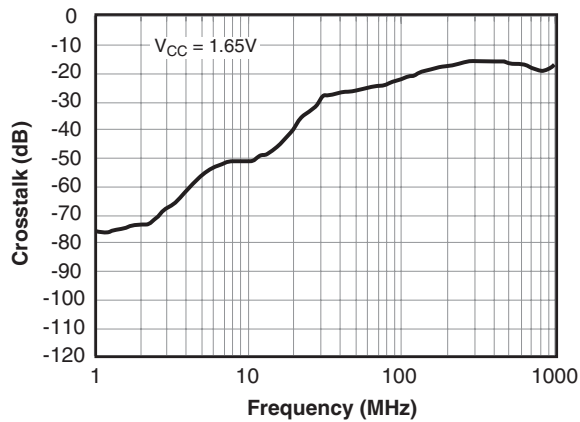


Figure 8. Crosstalk, $V_{CC} = 1.65V$

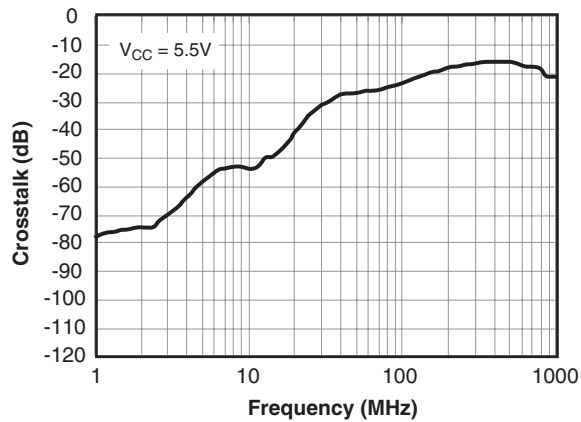


Figure 9. Crosstalk, $V_{CC} = 5.5V$

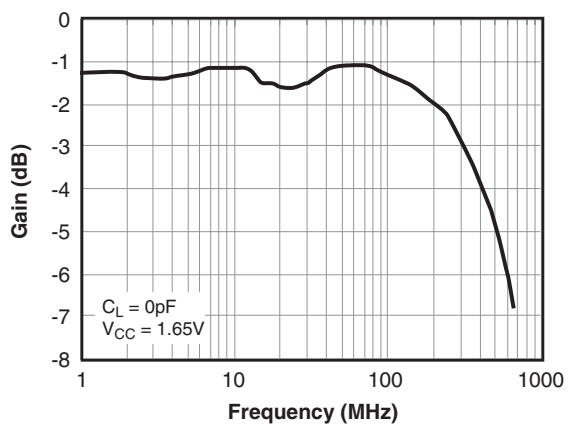


Figure 10. Bandwidth, $V_{CC} = 1.65V$

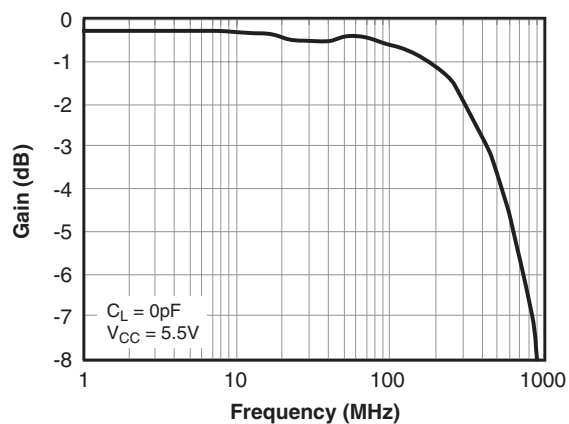
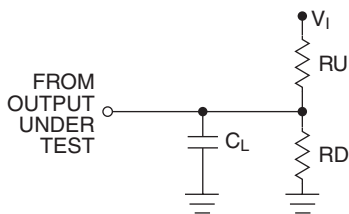


Figure 11. Bandwidth, $V_{CC} = 5.5V$

AC Loading and Waveforms



Notes:
 Input driven by 50Ω source terminated in 50Ω
 C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; t_W = 500 ns

Figure 12. AC Test Circuit

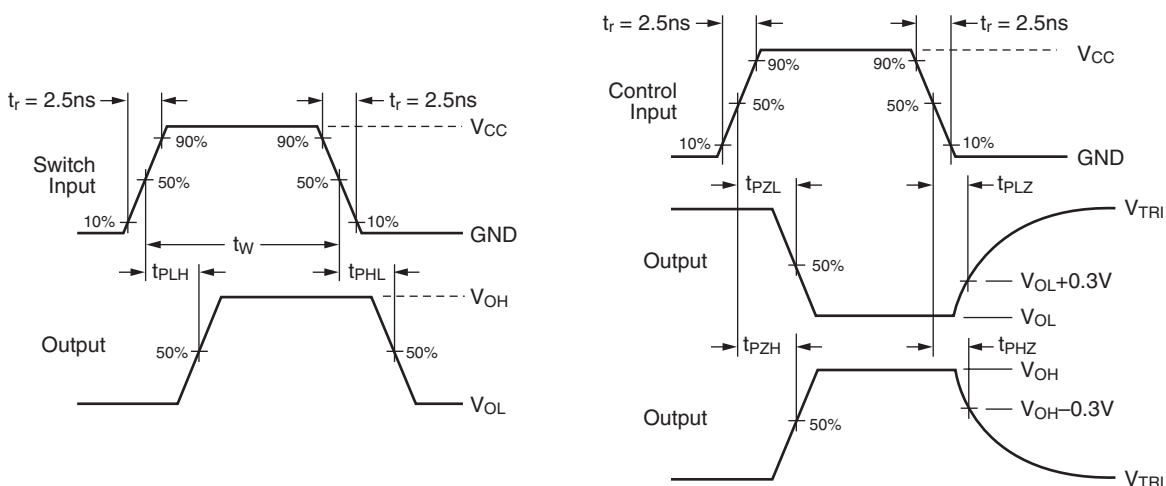


Figure 13. AC Waveforms

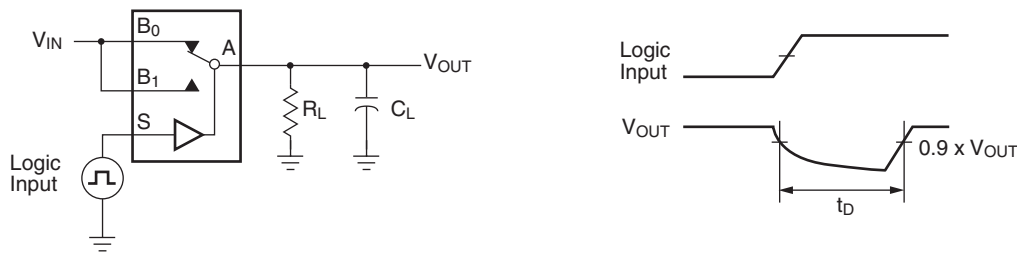


Figure 14. Break-Before-Make Interval Timing

AC Loading and Waveforms (continued)

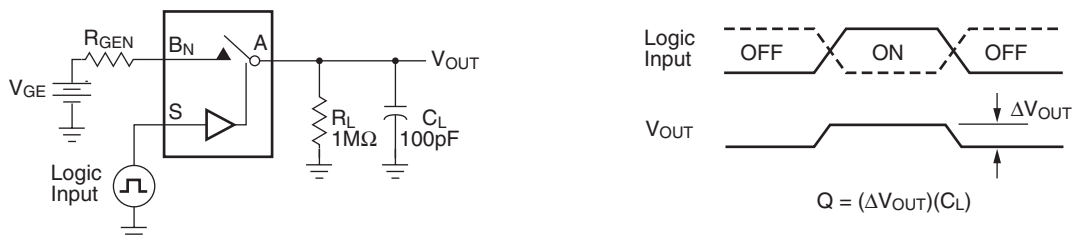


Figure 15. Charge Injection Test

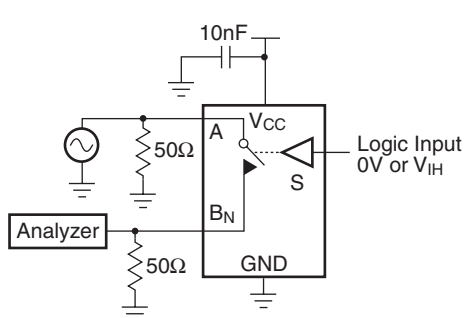


Figure 16. Off Isolation

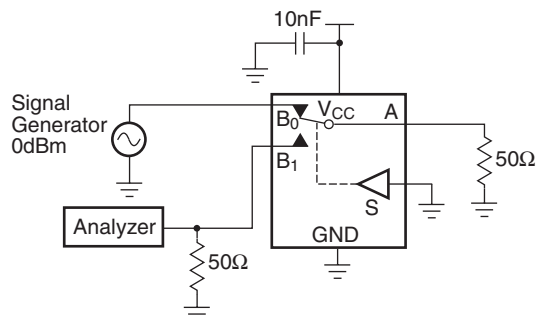


Figure 17. Crosstalk

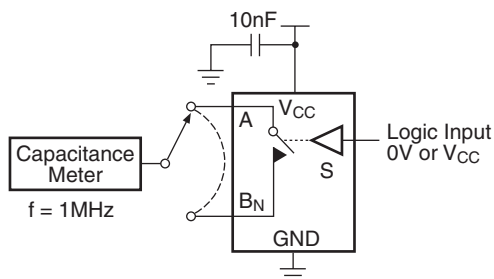


Figure 18. Channel Off Capacitance

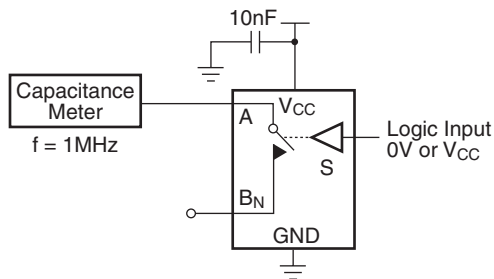


Figure 19. Channel On Capacitance

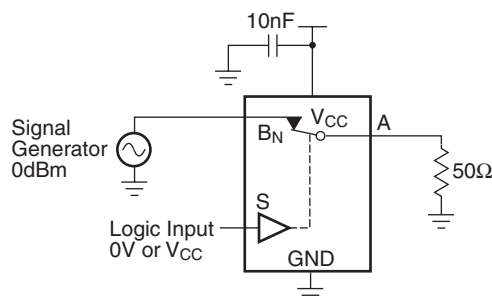


Figure 20. Bandwidth

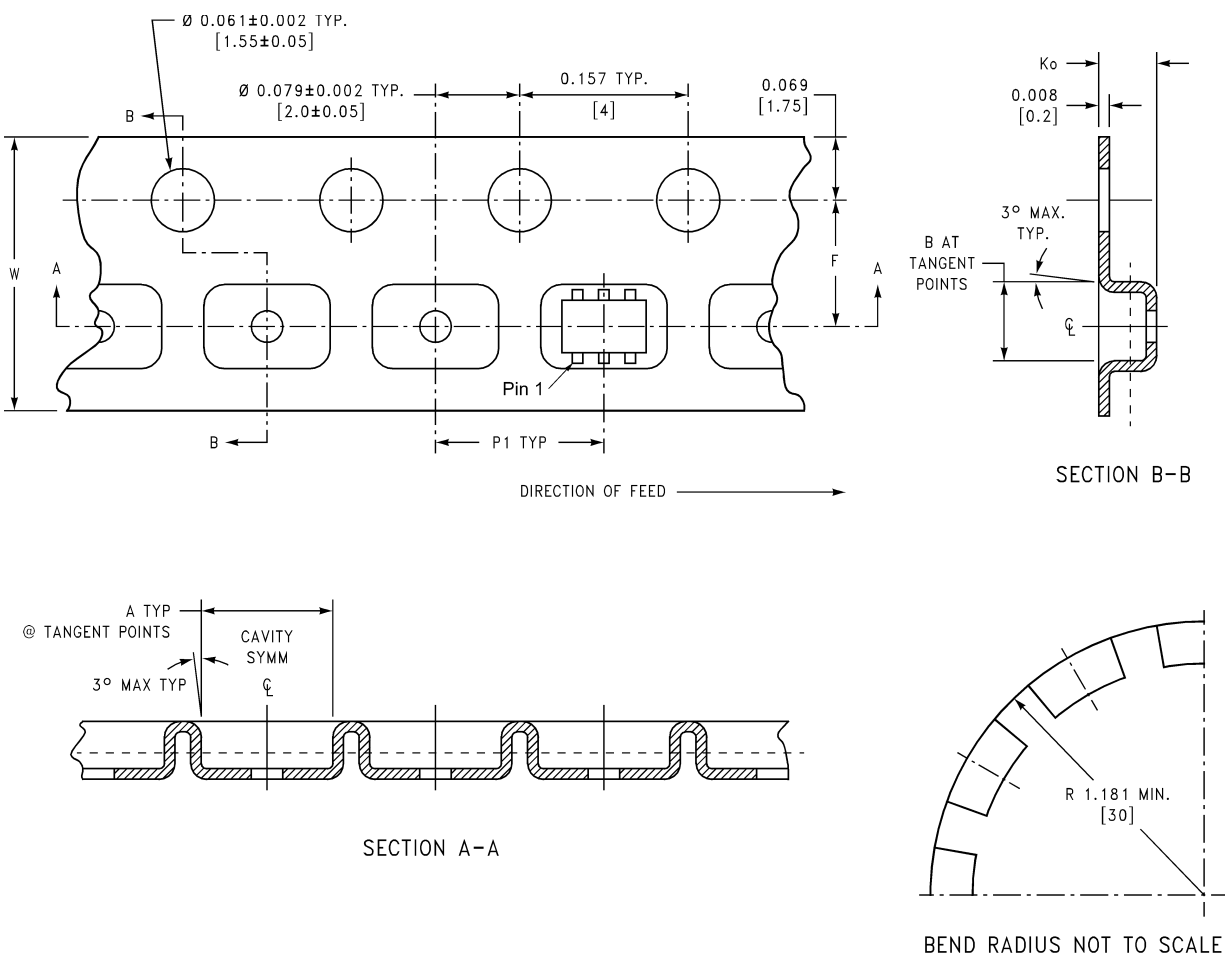
Tape and Reel Specification

Tape Format for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typical)	Empty	Sealed

Tape Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

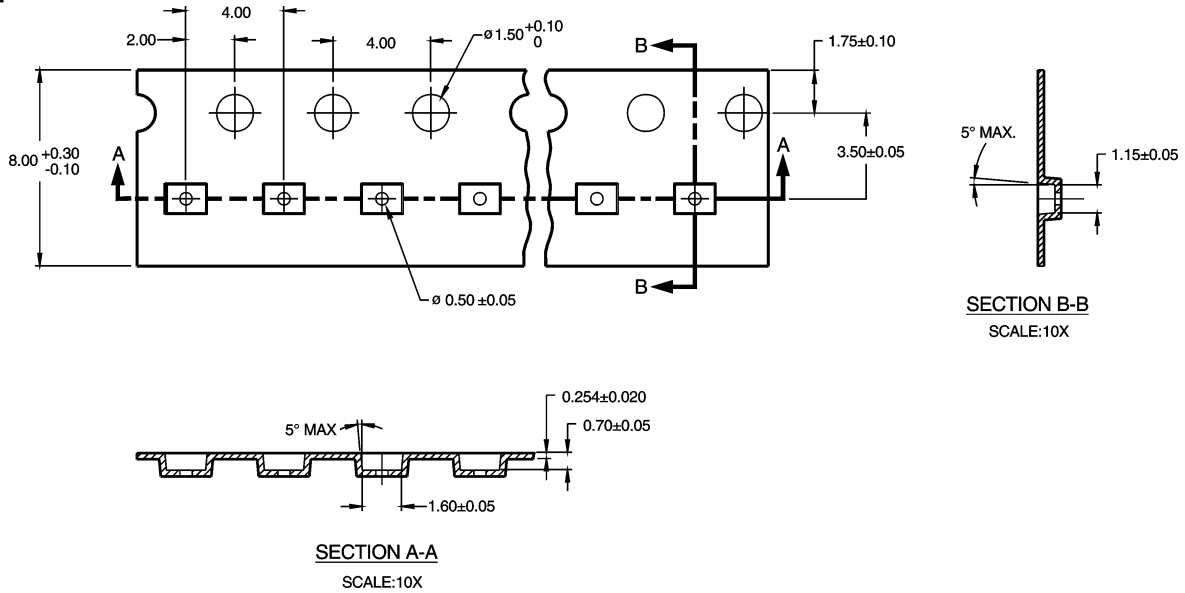


Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-6		0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004
	(8mm)	(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)

Tape Format for MicroPak™

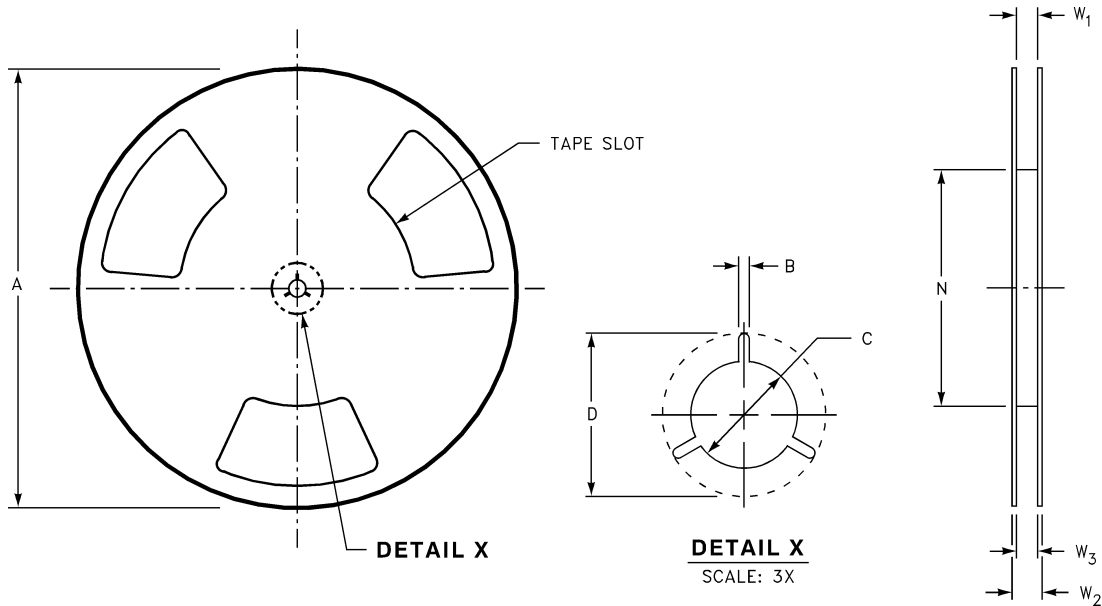
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typical)	Empty	Sealed

Tape Dimensions



Reel Dimensions

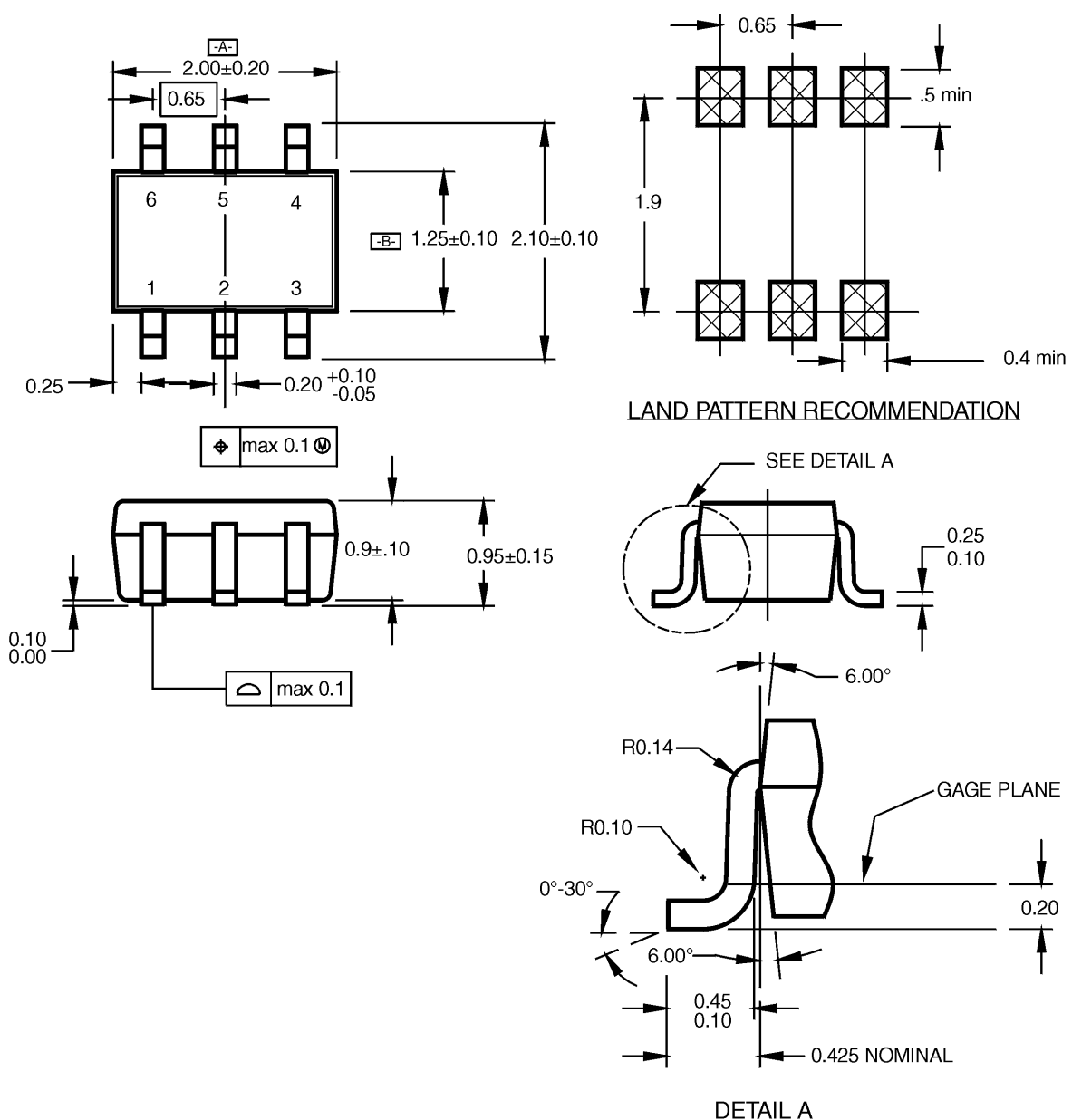
Dimensions are in inches (millimeters) unless otherwise noted.



Tape Size	A	B	C	D	N	W1	W2	W3
	7.0	0.059	0.512	0.795	2.165	$0.331 + 0.059/-0.000$	0.567	$W1 + 0.078/-0.039$
(8mm)	(177.8)	(1.50)	(13.00)	(20.20)	(55.00)	$(8.40 + 1.50/-0.00)$	(14.40)	$(W1 + 2.00/-1.00)$

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

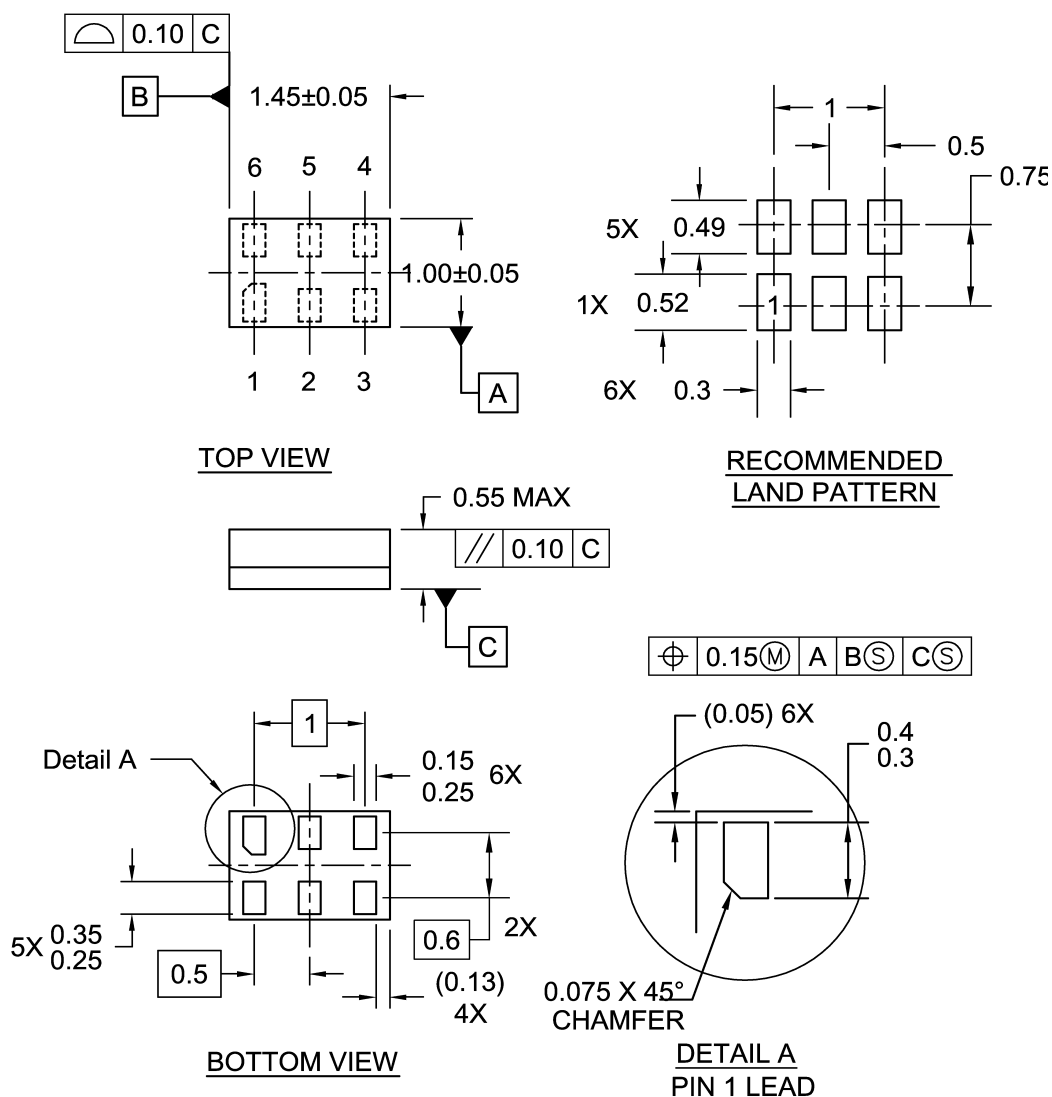
- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

Figure 21. 6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994


MAC06ARevB

Figure 22. 6-Lead, MicroPak™ 1.0mm Wide Package



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ActiveArray [™]	IntelliMAX [™]	Programmable Active Droop [™]	TinyLogic [®]
Bottomless [™]	ISOPLANAR [™]	QFET [®]	TINYOPTO [™]
Build it Now [™]	MICROCOUPLER [™]	QST [™]	TinyPower [™]
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CROSSVOLT [™]	MICROWIRE [™]	Quiet Series [™]	TruTranslation [™]
CTL [™]	Motion-SPM [™]	RapidConfigure [™]	μSerDes [™]
Current Transfer Logic [™]	MSX [™]	RapidConnect [™]	UHC [®]
DOME [™]	MSXPro [™]	ScalarPump [™]	UniFET [™]
E ² CMOST [™]	OCX [™]	SMART START [™]	VCX [™]
EcoSPARK [®]	OCXPro [™]	SPM [®]	Wire [™]
EnSigna [™]	OPTOLOGIC [®]	STEALTH [™]	
FACT Quiet Series [™]	OPTOPLANAR [®]	SuperFET [™]	
FACT [®]	PACMAN [™]	SuperSOT [™] .3	
FAST [®]	PDP-SPM [™]	SuperSOT [™] .6	
FAST _r [™]	POP [™]	SuperSOT [™] .8	
FPS [™]	Power220 [®]	SyncFET [™]	
FRFET [®]	Power247 [®]	TCM [™]	
GlobalOptoisolator [™]	PowerEdge [™]	The Power Franchise [®]	
GTO [™]	PowerSaver [™]		
HiSeC [™]			

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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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