STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME 1CH STEP-DOWN DC/DC CONVERTER

TYPE **BD9325FJ**

PACKAGE Fig.1 (SOP-J8)

BLOCK DIAGRAM Fig.2

FEATURE

1) 2A Output Current Integrated MOSFET Step-down Regulator
2) Current Mode PWM Controlled
3) Wide Operating INPUT Range
4) Feedback Voltage 0.9V
5) Low ESR Output Ceramic Capacitors are Available
6) SOP-J8 Package
7) Protection Circuit Under Voltage LockOut protection circuit
   Thermal ShutDown circuit
   Over Current Protection circuit

● ABSOLUTE MAXIMUM RATING (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	20	V
Switch Voltage	V_{SW}	20	V
EN Voltage	V_{EN}	20	V
Power Dissipation	Pd	675*	mW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	150	℃
BST Voltage	V_{BST}	V_{SW}+7	V
SS, FB, COMP Voltage	V_{LVPINS}	7	V

* Derating in done 5.4mW/℃ for operating above Ta≧25℃(On 70.0mm×70.0mm×1.6mm 1-layer board)

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

Application example
- ROHM cannot provide adequate confirmation of patents.
- The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
  Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
- ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

● **OPERATION RANGE** (Ta= -40~85℃)

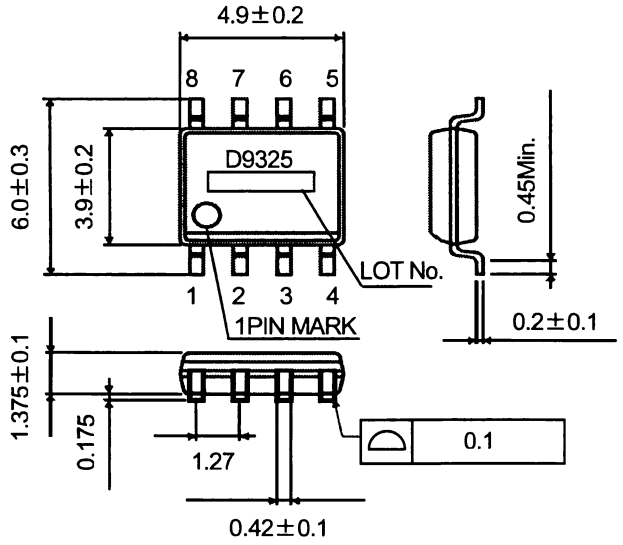
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{IN}	4.75	12	18	V
SW Voltage	V_{SW}	-0.5	-	18	V

● **Electrical characteristics** (unless otherwise specified VIN=12V Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Error amplifier block						
FB input bias current	I_{FB}	-	0.1	2	μA	
Feedback voltage 1	V_{FB}	0.886	0.900	0.914	V	Voltage follower
Feedback voltage 2	V_{FB}	0.873	0.900	0.927	V	Ta=-40~85℃
SW block – SW						
Leak current N-channel	I_{LEAKN}	-	0	10	μA	V_{IN}= 18V , V_{SW} = 0V
Hi-side FET On-resistance	R_{ONU}	-	0.16	-	Ω	I_{SW} = -0.8A
Lo-side FET On-resistance	R_{OND}	-	10	-	Ω	I_{SW} = 0.1A
Switch Current Limit	I_{LIMIT}	2.5	-	-	A	
Maximum duty cycle	M_{DUTY}	-	90	-	%	V_{FB} = 0V
General						
Enable Threshold Voltage	V_{EN}	1.0	1.18	1.4	V	
Under Voltage Lockout threshold	V_{UVLO}	4.05	4.40	4.75	V	V_{IN} rising
Under Voltage Lockout Hysteresis	V_{HYS}	-	0.1	-	V	
Soft Start Current	I_{SS}	23	41	62	μA	V_{SS}=0.1V
Soft Start Time	T_{SS}	-	1.6	-	ms	C_{SS}=0.1uF
Operating Frequency	F_{OSC}	300	380	460	kHz	
Circuit Current	I_{CC}	-	2.1	4.3	mA	V_{FB}= 1.5V, V_{EN}= 12V
Quiescent Current	I_{QUI}	-	80	170	μA	V_{EN}= OPEN

* This product is not designed for protection against radioactive rays

● PHYSICAL DIMENSION (SOP-J8)



Pin No.	Pin name
1	BST
2	VIN
3	SW
4	GND
5	FB
6	COMP
7	EN
8	SS

Fig.1 SOP-J8 Package
(Unit:mm)

● Block Diagram

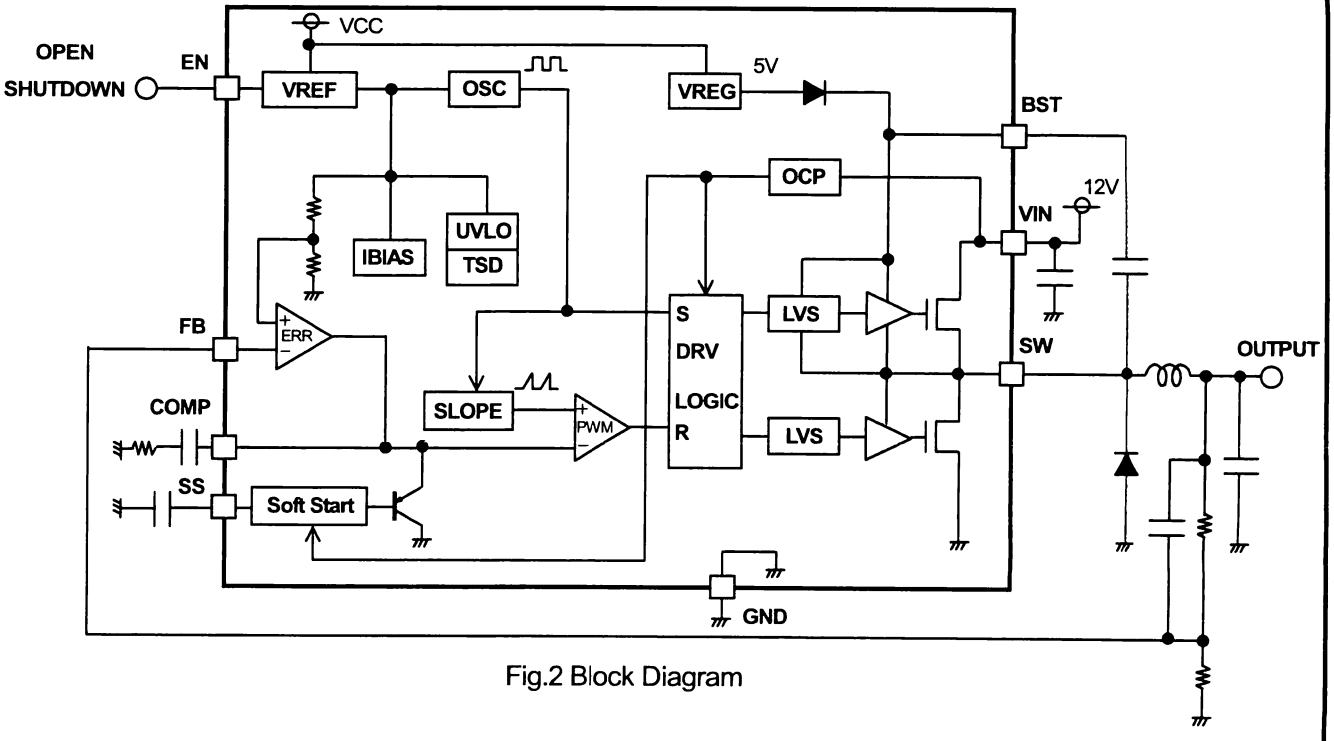


Fig.2 Block Diagram

● OPERATION NOTES

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated. When VIN voltage is near the absolute maximum ratings, there are possibilities that the VIN voltage exceed the limit and the IC is destroyed. So please consider using zener diode between VIN-GND or using large input-capacitor in order not to destroy the IC.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when the resistors and transistors are connected to the pins as shown in Fig. , a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins. The SW voltage becomes lower than GND voltage on the situation, so use the low voltage drop shotkey barrier diode between the SW and the GND.

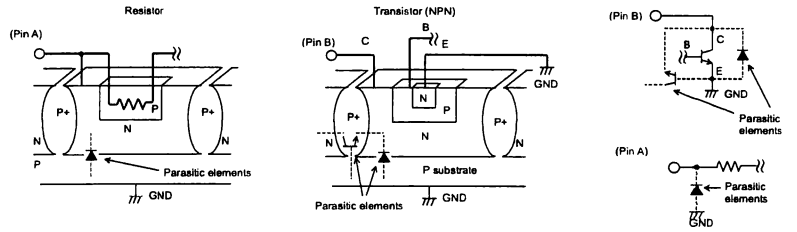


Fig. Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.