



Serial-in / Parallel-out Driver Series

Serial / Parallel 2-input Drivers





BU2098F, BU2090F, BU2090FS

Description

Serial-in-parallel-out driver is a open drain output driver. It incorporates a built-in shift register and a latch circuit to turn on a maximum of 12 LED by a 2-line interface, linked to a microcontroller.

A open drain output provides maximum of 25mA current.

Features

- 1) LED can be driven directly. (Output current 25mA)
- 2) 8/12 Bit parallel output
- 3) This product can be operated on low voltage.
- 4) Compatible with I²C BUS. (BU2098)

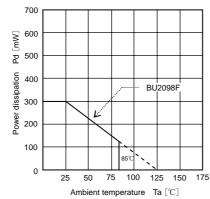
•Use

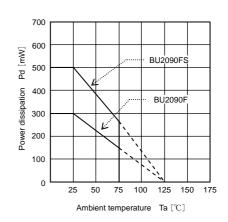
For AV equipment such as, audio stereo sets, videos and TV sets, PCs, control microcontroller mounted equipment.

Line up

Parameter	BU2098F	BU2090F	BU2090FS	Unit
Output current	25	2	5	mA
Output line	8	1	lines	
Package	SOP16	SOP16	SSOP-A16	_

Thermal derating curve





Mar. 2008

^{*} I²C BUS is a registered trademark of Phillips.

Electrical characteristics

BU2098F (unless otherwise noted, V_{DD}=5V, Vss=0V, Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Input High-level voltage	V _{IH}	$0.7 \mathrm{X} V_{DD}$	-	-	V	
Input Low-level voltage	V _{IL}	-	-	$0.3\mathrm{X}V_{DD}$	V	
Output Low-level voltage	V _{OL}	-	-	0.4	V	I _{OUT} =10mA
Input Low-level current	I _{IL}	-		2.0	μ A	V _{IN} =0
Input High-level current	I _{IH}	-	-	-2.0	μ A	V _{IN} =V _{DD}
Output leakage current	l _{OZ}	-	-	±5.0	μ Α	Output=High impedance V _{OUT} =V _{DD}
Static dissipation current	I _{DD}	-	-	2.0	μ A	

BU2090F/FS (unless otherwise noted, $V_{DD}=5V/3V$, $V_{SS}=0V$, $Ta=25^{\circ}C$)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Input High-level voltage	V _{IH}	3.5/2.5*	-	-	V	
Input Low-level voltage	V _{IL}	-	-	1.5/0.4*	V	
Output Low-level voltage	V _{OL}	-	-	2.0/1.0*	V	I _{OL} =20mA
"H" output disable current	l _{OZH}	-	-	10	μ A	V ₀ =25V
"L" output disable current	l _{OZL}	-		-5.0	μ A	V _O =0V
Static dissipation current	I _{DD}	-	-	5.0/3.0*	μ A	

(*the value at 5V /3V)

●Operating conditions (Ta=25°C, V_{SS}=0V)

Doromotor	Symbol	Lim	Unit	
Parameter	Symbol	BU2098F	BU2090F/FS	Offic
Power Supply Voltage	V_{DD}	+2.7	~5.5	V
Output Voltage	Vo	0~+15	0∼+25	V

Absolute maximum ratings

BU2098F, BU2090F/FS

Parameter	Cymhol		Unit		
Parameter	Symbol	BU2098F	BU2098F BU2090F		Offic
Power supply voltage	V_{DD}	-0.5∼ + 7.0	-0.3∼	+7.0V	V
Power dissipation1	Pd1	300 *1	300 * ¹	500 * ²	\^/
Power dissipation2	Pd2	-	- 500 * ³ 650 * ⁴		mW
Operating temperature range	Topr		$^{\circ}$		
Storage temperature range	Tstg		$^{\circ}$		
Output voltage	Vo	V _{SS} ∼+18.0 V _{SS} -0.3∼+25V		V	
Input voltage	V _{IN}	-0.5~V _{DD} +0.5 V _{SS} -0.3~V _{DD} +0.3V			V

Allowable loss of single unit
* Reduced by 3mW/°C over 25°C. (BU2098F)
* Reduced by 3mW/°C over 25°C.

^{*2} Reduced by 5mW/°C over 25°C.

^{*3} Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.(When mounted on a board 70mm×70mm×1.6mm Glass-epoxy PCB)

^{*4}Reduced by 6.5mW for each increase in Ta of 1°C over 25°C.(When mounted on a board 70mm×70mm×1.6mm Glass-epoxy PCB)

Pin descriptions

BU2098F

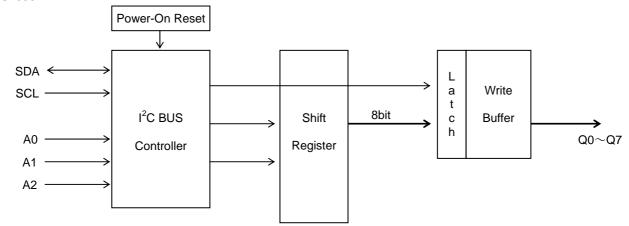
PIN No.	Pin Name	I/O	Function
1	A0	- 1	
2	A1		Address input, internally pull-up
3	A2	ı	
4	Q0		
5	Q1	0	On an Idrain autout
6	Q2	0	Open drain output
7	Q3		
8	V_{SS}	-	GND
9	Q4		
10	Q5	0	On an Idrain autout
11	Q6	0	Open drain output
12	Q7		
13	N.C.	-	Non connected
14	SCL	I	Serial clock input
15	SDA	I/O	Serial data input/output
16	V_{DD}	-	Power supply

BU2090F/FS

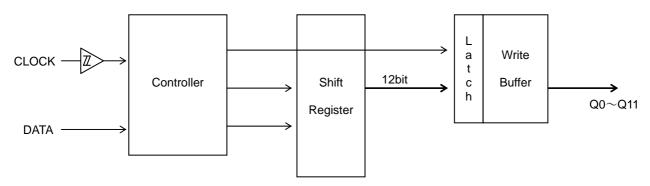
0UZU9UF/F3	•								
PIN No.	Pin Name	I/O			Function				
1	Vss	-	GND						
2	DATA	I	Serial data input						
	01 001		Data shift clock in (rising edge trigge	Data shift clock input (rising edge trigger)					
3	CLOCK	I		-	the output	when the input data logic			
			level is high durin	g the falling t	ransition of th	ne clock pulse.			
4	Q0								
5	Q1								
6	Q2								
7	Q3								
8	Q4		Parallel data outp	ut (Nch Oper	n Drain FET)				
9	Q5								
10	Q6	0	Latch data	L	Н				
11	Q7		Output FET	ON	OFF				
12	Q8								
13	Q9								
14	Q10								
15	Q11								
16	V_{DD}	-	Power supply						

Block diagram

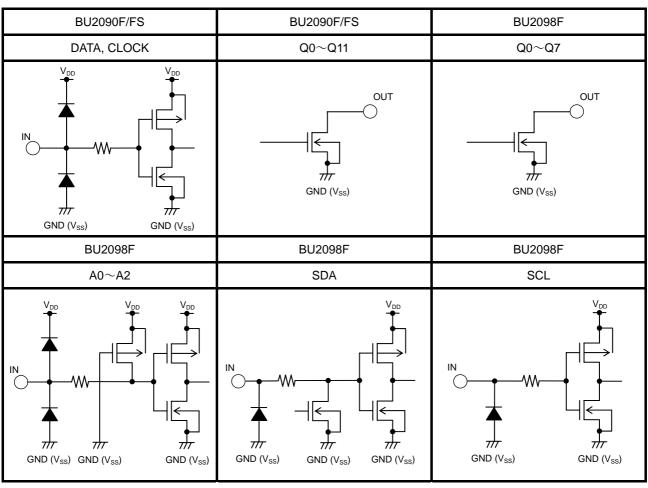
BU2098F



BU2090F/FS



Interfaces



[BU2098F]

lacktriangle AC characteristics (Unless otherwise noted, $V_{DD}\!\!=\!\!5V,\,V_{SS}\!\!=\!\!0V,\,Ta\!\!=\!\!25^{\circ}\!\!\mathrm{C})$

Doromotor	Cymphol	Symbol Fast mode I ² C BUS		Standard mo	Unit	
Parameter	Symbol	Min.	Max.	Min.	Max.	Offic
SCL clock frequency	fscL	0	400	0	100	kHz
Bus free time between start-stop condition	tBUS	1.3	-	4.7	-	μ S
Hold time start condition	thd:STA	0.6	-	4.0	-	μ S
Low period of the SCL clock	tLOW	1.3	-	4.7	-	μ S
High period of the SCL clock	tHIGH	0.6	-	4.0	-	μ S
Set up time Re-start condition	tsu:sta	0.6	-	4.7	-	μ S
Data hold time	thd:dat	0	0.9	0	-	μ S
Data set up time	tsu:dat	100	-	250	-	ns
Rise time of SDA and SCL	tR	20+0.1Cb	300	1	1000	ns
Fall time of SDA and SCL	tF	20+0.1Cb	300	-	300	ns
Set up time stop condition	tsu:sto	0.6	-	4.0	-	μ S
Capacitive load for SDA line and SCL line	Cb	-	400	-	400	pF

●Timing chart

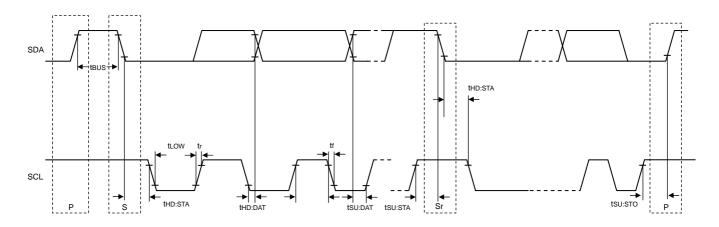


Fig.1 SDA, SCL timing chart

Function

OStart condition

The start condition is a "HIGH" to "LOW" transition of the SDA line while SCL is "HIGH".

OStop condition

The stop condition is a "LOW" to "HIGH" transition of the SDA line while SCL is "HIGH".

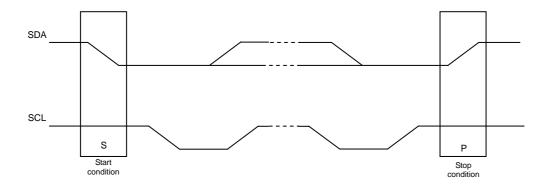


Fig.2 Start / Stop condition

OAcknowledge

The master (μ p) puts a resistive "HIGH" level on the SDA line during the acknowledge clock pulse. The peripheral (audio processor) that acknowledge has to pull-down ("LOW") the SDA line during the acknowledge clock pulse, so that the SDA line is stable "LOW" during this clock pulse.

The slave which has been addressed has to generate an acknowledgement after the reception of each byte, otherwise the SDA line remains at the "HIGH" level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

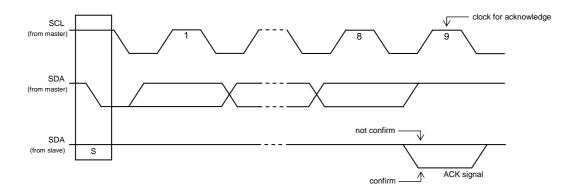


Fig.3 Acknowledge

○Write DATA

Send the stave address from master following the start condition (S). This address consists of 7 bits. The left 1 bit (the foot bit) is fixed "0". The stop condition (P) is needed to finish the data transferred. But the re-send starting condition (Sr) enables to transfer the data without STOP (P).

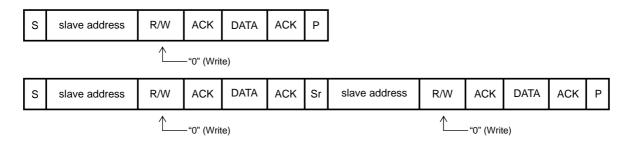


Fig.4 DATA transmit

OData format

The format is following.

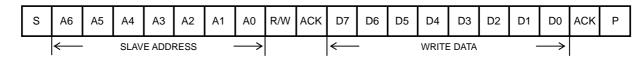


Table 1 for WRITE format

Slave address	A0∼A2	Each bit can be defined by the input levels of pins A0~A3.
Slave address	A3~A6	These 4 bits are fixed.
	R/W	"0"
Write Data	D0 - D7	Write "1" to D0 makes Q0 pin High-impedance. And write "0" makes Q0
white Data	D0∼D7	pin LOW. D[1:7] and Q[1:7] are same as D0 and Q0.

Table 2 for (A2, A1, A0) to SLAVE ADDRESS

A6	A5	A4	A3	A2	A1	A0	Slave address
0	1	1	1	0	0	0	38H
0	1	1	1	0	0	1	39H
0	1	1	1	0	1	0	ЗАН
0	1	1	1	0	1	1	3ВН
0	1	1	1	1	0	0	3CH
0	1	1	1	1	0	1	3DH
0	1	1	1	1	1	0	3EH
0	1	1	1	1	1	1	3FH
	Fixed for BU2098F						

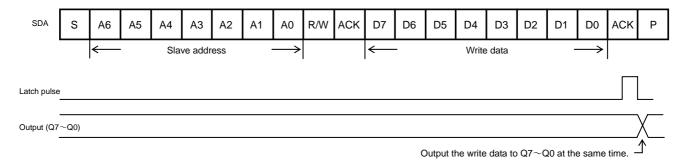
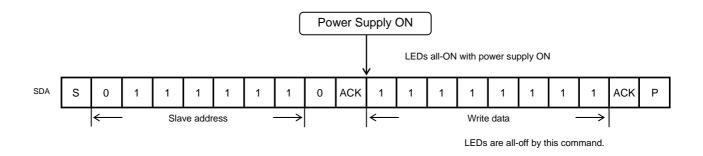


Fig.5 Timing chart for WRITE

Command sample for driving LEDs. These are all off. (terminal A0~A2 is open)



 \cdot RESET CONDITION $\text{After reset, Q0}{\sim}\text{Q7 pins are ON. (LEDs are all ON.)}$

· RISING TIME OF POWER SUPPLY

 V_{DD} must rise within 10ms. If the rise time would exceed 10ms, it is afraid not to reset the BU2098F.

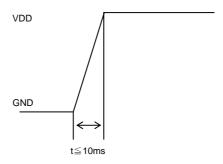


Fig.6 Rising time of power supply

[BU2090F/FS]

ullet AC characteristics (unless otherwise noted, V_{DD}=5V, V_{SS}=0V, Ta=25 $^{\circ}$ C)

Parameter	Symbol	Limit			Unit	Condition	
Farameter	Symbol	Min.	Тур.	Max.	Offic	Condition	
Minimum alaak fraguanay	tw	500	-	-	ns	V _{DD} =5V	
Minimum clock frequency	tvv	1000	-	-	ns	V _{DD} =3V	
Data shift set up time	tsu	200	-	-	ns	V _{DD} =5V	
Data shift set up time	เอ	300	-	•	ns	V _{DD} =3V	
Data shift hold time	tH	200	•	•	ns	V _{DD} =5V	
Data Shiit Hold time		400	-	-	ns	V _{DD} =3V	
Data latch set up time	tlsuh	50	•	•	ns	V _{DD} =5V	
Data lateri set up time		100	-	•	ns	V _{DD} =3V	
Data latch hold time	t∟нн	250	-	-	ns	V _{DD} =5V	
	ILHH	500	-	-	ns	V _{DD} =3V	
Data latch "L"	t i (CI II	200	-	•	ns	V _{DD} =5V	
set up time	tLSUL	400	-	-	ns	V _{DD} =3V	
Data latch "L"	tlhl	250	•	•	ns	V _{DD} =5V	
hold time	ILML	500	-	-	ns	V _{DD} =3V	

Switching time test circuit

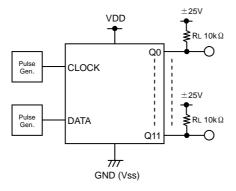


Fig.7

Switching time test waveforms

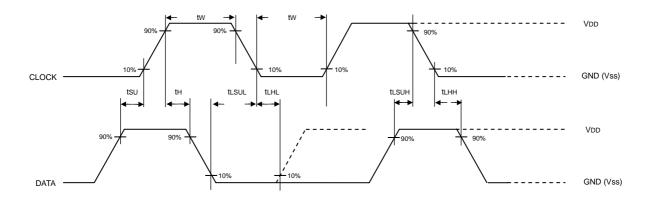
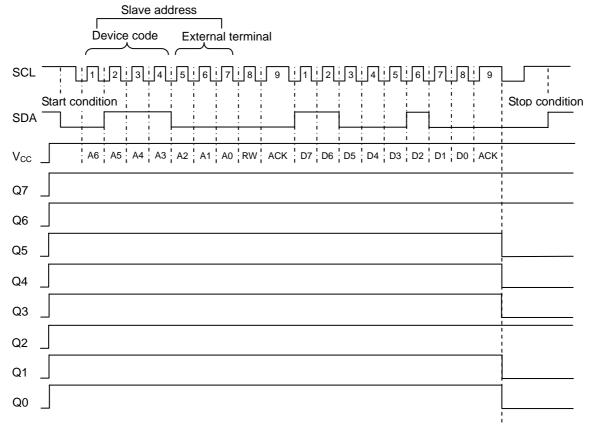


Fig.8

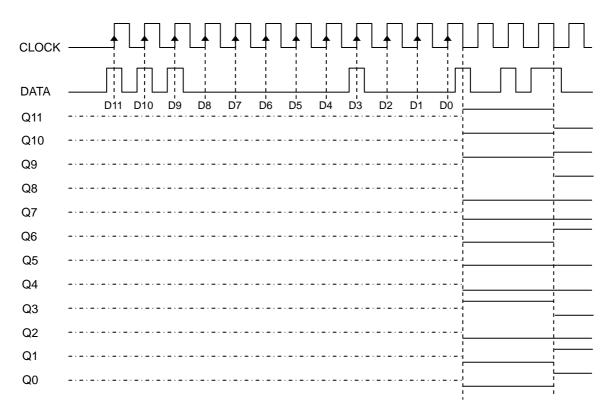
Timing chart

[BU2098F]



Note) Diagram shows a status where a pull-up resistor is connected to output.

[BU2090F/FS]



Note1) ----- Indicates undefined output.

Note2) Output terminal is provided with a pull-up resistor.

Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

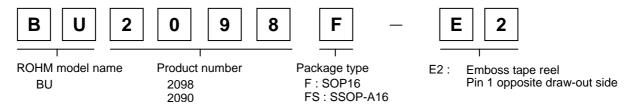
9. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

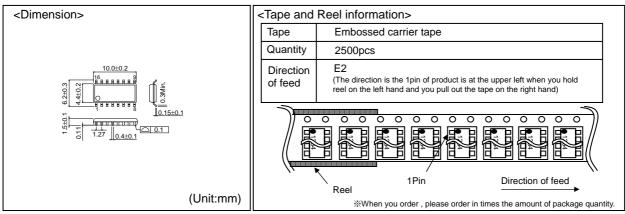
10. Unused input terminals

Connect all unused input terminals to VDD or VSS in order to prevent excessive current or oscillation. Insertion of a resistor ($100k\Omega$ approx.) is also recommended.

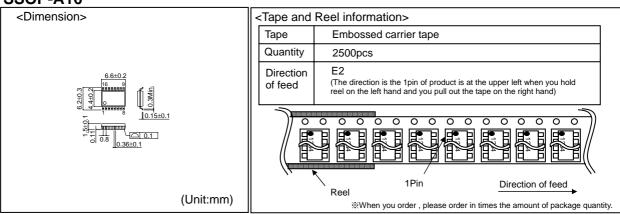
Type Designations (Selections) for Ordering



SOP16



SSOP-A16



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It is our top priority to supply products with the utmost quality and reliability. However, there is always a chance of failure due to unexpected factors. Therefore, please take into account the derating characteristics and allow for sufficient safety features, such as extra margin, anti-flammability, and fail-safe measures when designing in order to prevent possible accidents that may result in bodily harm or fire caused by component failure. ROHM cannot be held responsible for any damages arising from the use of the products under conditions out of the range of the specifications or due to non-compliance with the NOTES specified in this catalog.

Thank you for your accessing to ROHM product informations.

More detail product informations and catalogs are available, please contact your nearest sales office.

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