DATA SHEET

74LVC02A
Quad 2-input NOR gate

Product specification
Supersedes data of 2003 May 01

2004 Mar 12

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Quad 2-input NOR gate 74LVC02A

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from
  –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC02A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVC02A provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 50 pF; V_{CC} = 3.3 V	2.3	ns
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V; notes 1 and 2	10	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC02AD	–40 °C to +125 °C	14	SO14	plastic	SOT108-1
74LVC02ADB	–40 °C to +125 °C	14	SSOP14	plastic	SOT337-1
74LVC02APW	–40 °C to +125 °C	14	TSSOP14	plastic	SOT402-1
74LVC02ABQ	–40 °C to +125 °C	14	DHVQFN14	plastic	SOT762-1

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	**nB**	**nY**
L	L	H
L	H	L
H	L	L
H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

PINNING

PIN	SYMBOL	DESCRIPTION
1	1Y	data output
2	1A	data input
3	1B	data input
4	2Y	data output
5	2A	data input
6	2B	data input
7	GND	ground (0 V)
8	3A	data input
9	3B	data input
10	3Y	data output
11	4A	data input
12	4B	data input
13	4Y	data output
14	V_{CC}	supply voltage

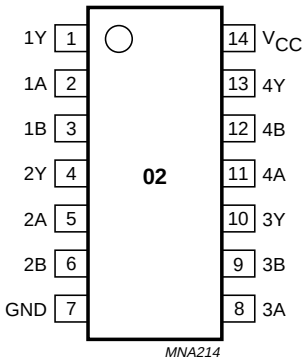
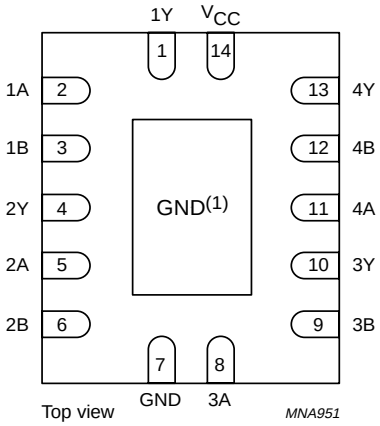


Fig.1 Pin configuration SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

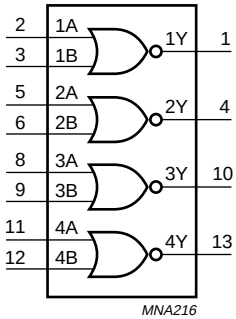


Fig.3 Logic symbol.

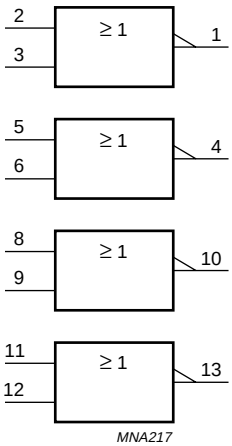


Fig.4 Logic symbol (IEEE/IEC).

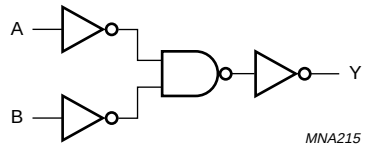


Fig.5 Logic diagram (one gate).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	–	±50	mA
V_O	output voltage	note 1	–0.5	V_{CC} + 0.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO14 packages: above 70 °C derate linearly with 8 mW/K.
   For SSOP and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
   For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.2	–	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.5	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.6	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	–	0.2	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	±0.1	±5	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.3	–	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.65	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.75	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 1	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.6	V
		I_O = 24 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	–	–	5000	μA

Note

1. Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

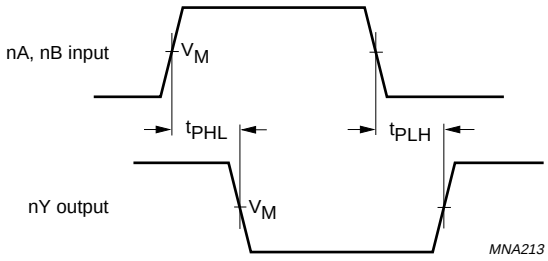
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	14	–	ns
			2.7	1.0	2.7	5.1	ns
			3.0 to 3.6	1.0	2.3(2)	4.4	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.0	ns
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.0	–	6.5	ns
			3.0 to 3.6	1.0	–	5.5	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.5	ns

Notes

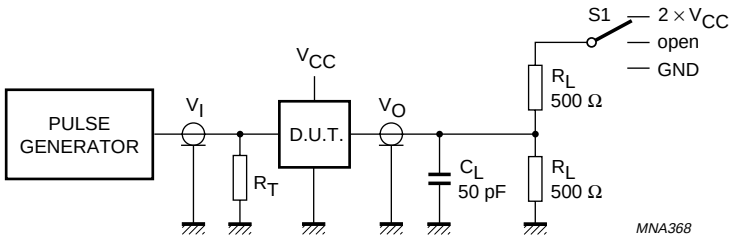
1. All typical values are measured at $T_{amb} = 25$ °C.
2. This typical value are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 The input nA, nB to output nY propagation delays.



V_{CC}	V_I	C_L	R_L	SWITCH S1		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω[1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

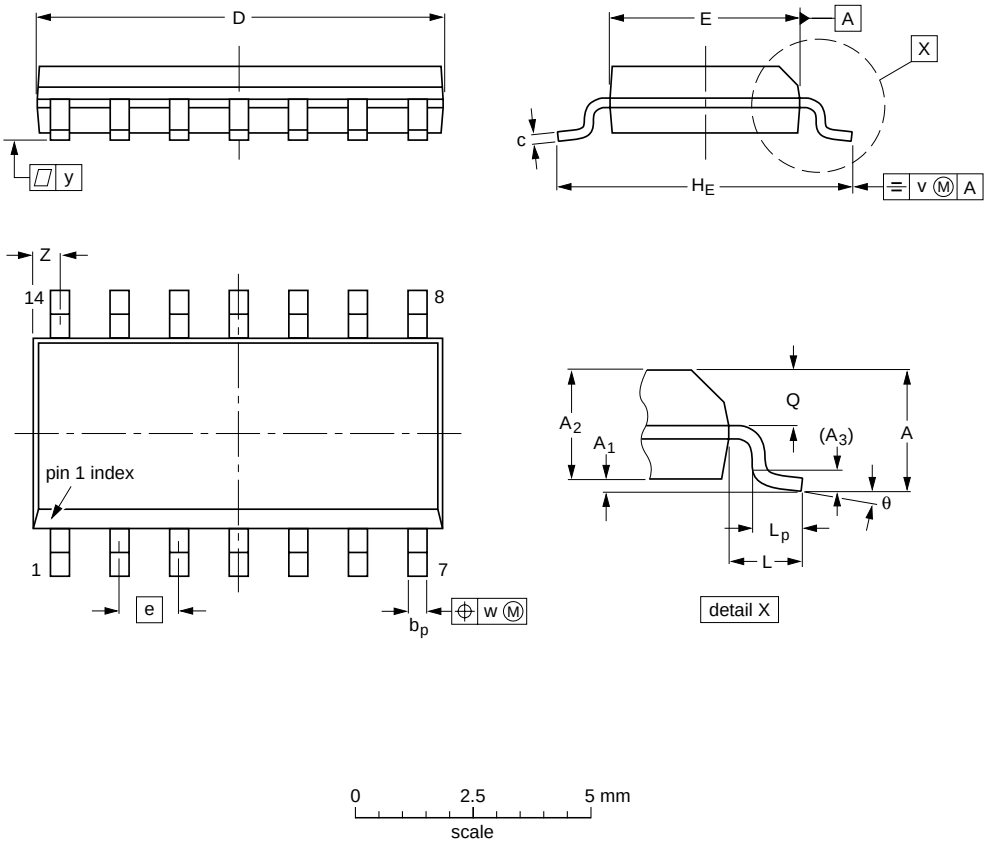
1. The circuit performs better when RL = 1000 Ω.

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

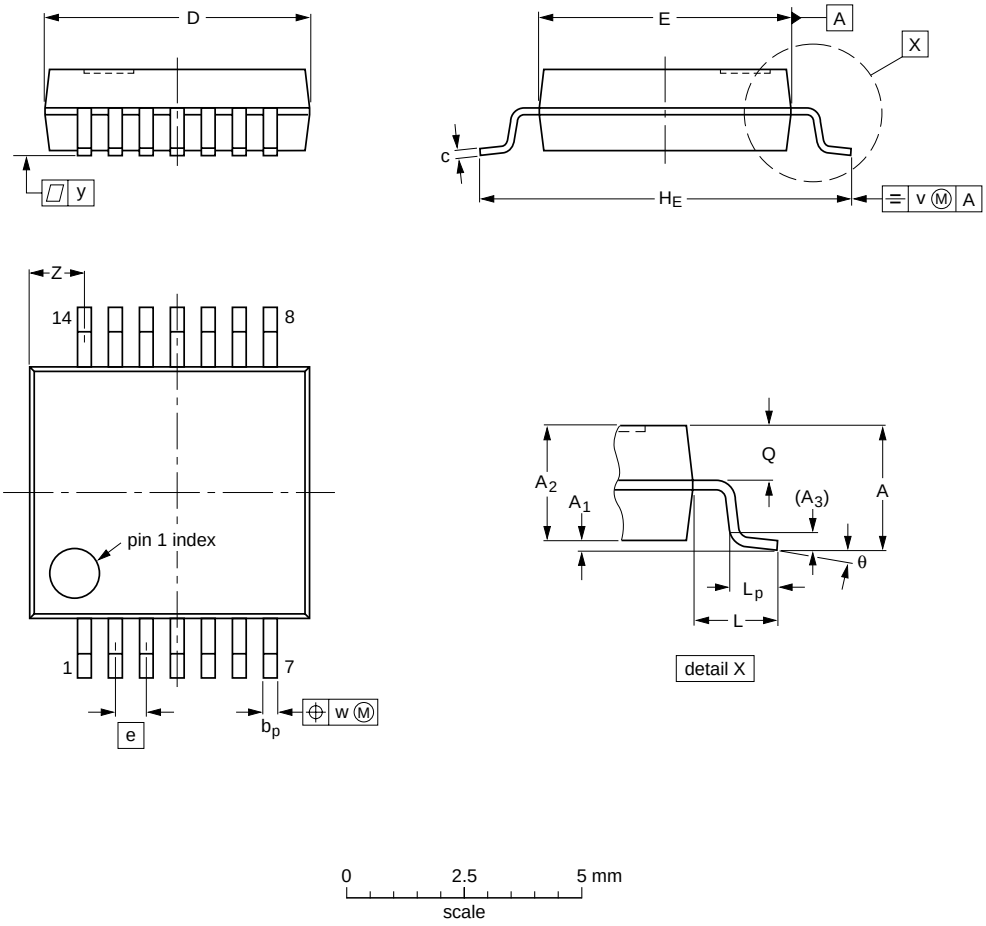
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

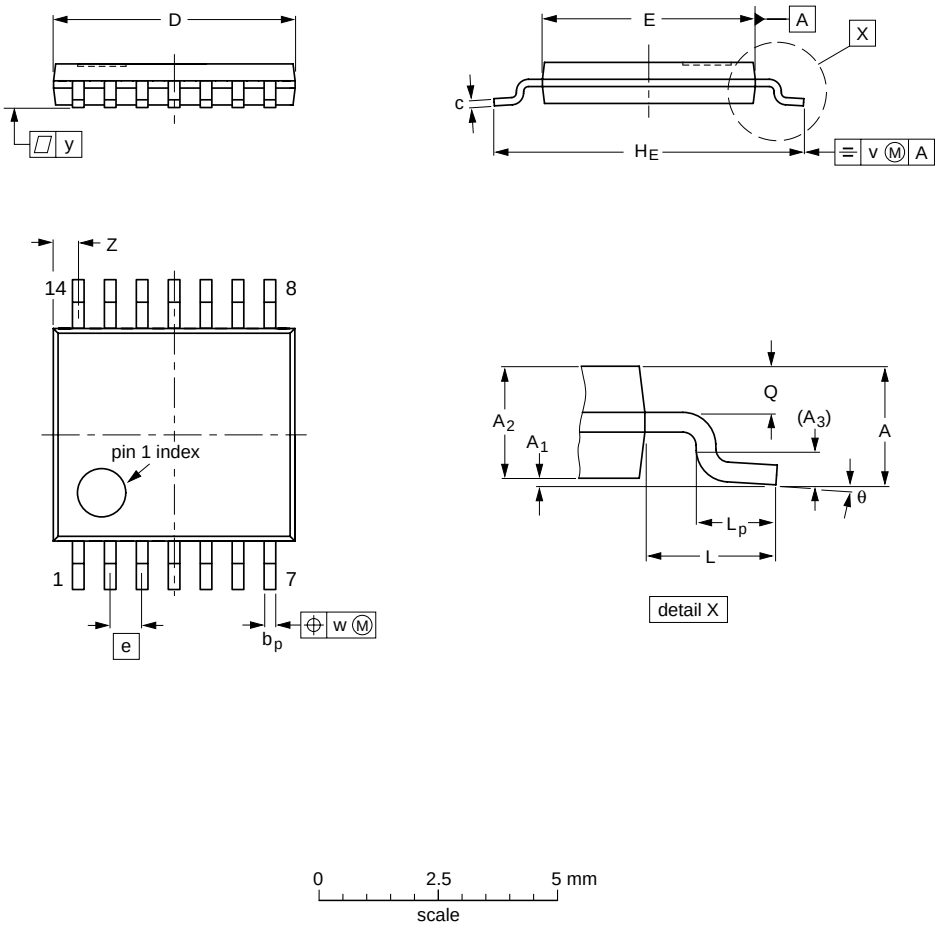
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

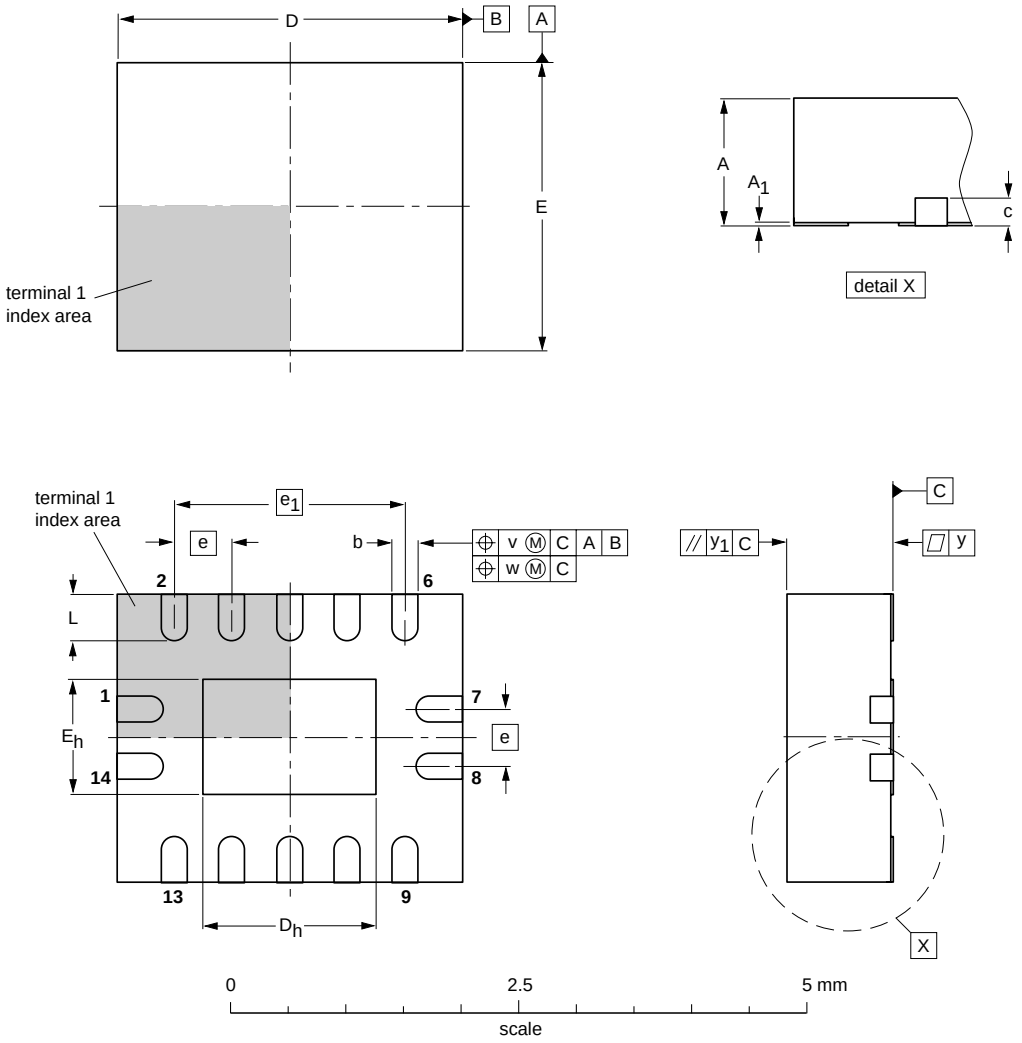
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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