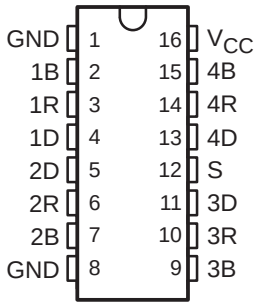
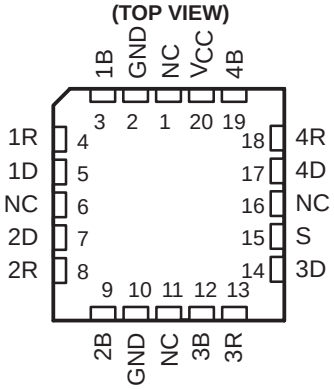
- **Single 5-V Supply**
- **High-Input-Impedance, High-Threshold Receivers**
- **Common Driver Strobe**
- **TTL-Compatible Driver and Strobe Inputs With Clamp Diodes**
- **High-Speed Operation**
- **100-mA Open-Collector Driver Outputs**
- **Four Independent Channels**
- **TTL-Compatible Receiver Output**

SN55138 . . . J OR W PACKAGE
SN75138 . . . D OR N PACKAGE
(TOP VIEW)



SN55138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55138 and SN75138 quadruple bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver open-collector output is designed to handle loads up to 100-mA open collector. The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

The receiver design also features a threshold of 2.3 V (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single 5-V supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero.

The SN55138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75138 is characterized for operation from 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Function Tables

TRANSMITTING

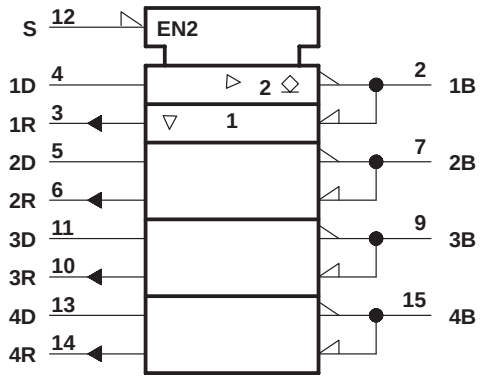
INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

RECEIVING

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

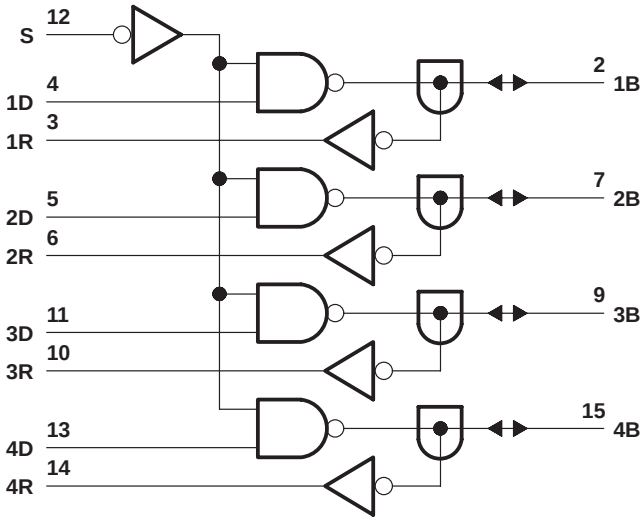
H = high level, L = low level, X = irrelevant

logic symbol†

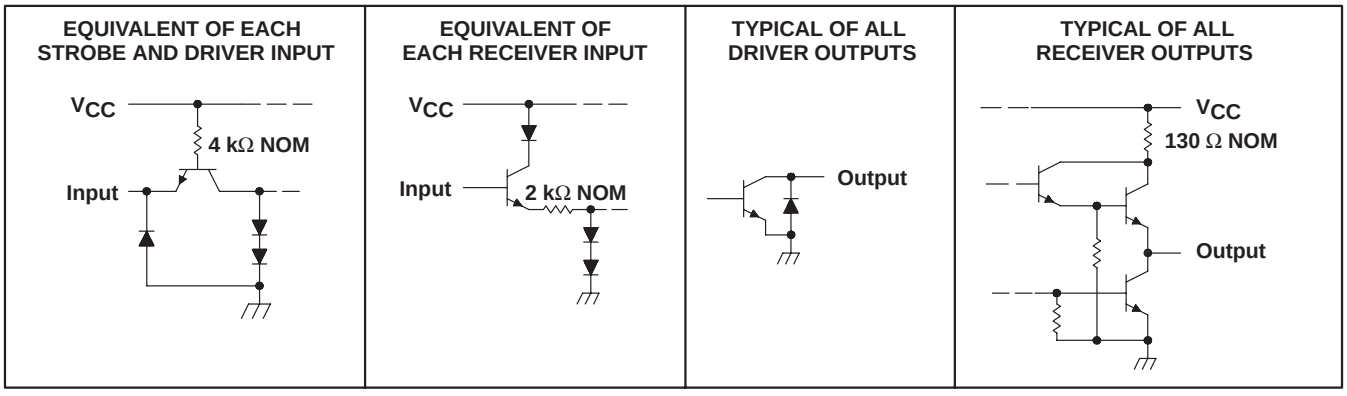


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Driver off-state output voltage . . . . . 7 V
Low-level output current into the driver output . . . . . 150 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55138 . . . . . –55°C to 125°C
SN75138 . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package . . . . . 260°C
Case temperature for 60 seconds, T_C: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to both ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK and J packages, the SN55138 chip is alloy mounted.

recommended operating conditions

		SN55138			SN75138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5		5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver or strobe	2			2			V
	Receiver	3.2			2.9			
Low-level input voltage, V_{IL}	Driver or strobe			0.8			0.8	V
	Receiver			1.5			1.8	
High-level output current, I_{OH}	Receiver output			–400			–400	μA
Low-level output current, I_{OL}	Driver output			100			100	mA
	Receiver output			16			16	
Operating free-air temperature, T_A		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55138			SN75138			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	Driver or strobe	V_{CC} = MIN,	I_I = –12 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage	Receiver	V_{CC} = MIN, $V_{IL(R)}$ = V_{IL} max,	$V_{IH(S)}$ = 2 V, I_{OH} = –400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	Driver	V_{CC} = MIN, $V_{IL(S)}$ = 0.8 V,	$V_{IH(D)}$ = 2 V, I_{OL} = 100 mA			0.45			0.45	V
		Receiver	V_{CC} = MIN, $V_{IH(S)}$ = 2 V,	$V_{IH(R)}$ = V_{IH} min, I_{OL} = 16 mA			0.4			0.4	
I_I(max)	Input current at maximum input voltage	Driver or strobe	V_{CC} = MAX,	V_I = V_{CC}			1			1	mA
I_{IH}	High-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
		Receiver	V_{CC} = 5 V, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 4.5 V,		25	300		25	300	
I_{IL}	Low-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 0.4 V		–1	–1.6		–1	–1.6	mA
		Receiver	V_{CC} = MAX, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 0.45 V,			–50			–50	μA
$I_{I(off)}$	Input current with power off	Receiver	V_{CC} = 0,	V_I = 4.5 V		1.1	1.5		1.1	1.5	mA
I_{OS}	Short-circuit output current§	Receiver	V_{CC} = MAX		–20		–55	–18		–55	mA
I_{CC}	Supply current	All driver outputs low	V_{CC} = MAX, $V_{I(S)}$ = 0.8 V	$V_{I(D)}$ = 2 V,		50	65		50	65	mA
		All driver outputs high	V_{CC} = MAX, $V_{I(S)}$ = 2 V, Receiver outputs open	$V_{I(R)}$ = 3.5 V,		42	55		42	55	

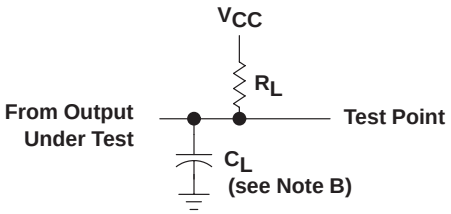
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

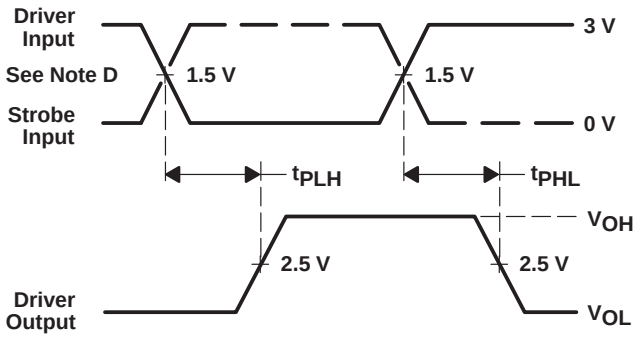
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Driver	Driver	C_L = 50 pF, R_L = 50 Ω,	See Figure 1		15	24	ns
t_{PHL}						14	24	
t_{PLH}	Strobe	Driver				18	28	ns
t_{PHL}						22	32	
t_{PLH}	Receiver	Receiver	C_L = 15 pF R_L = 400 Ω,	See Figure 2		7	15	ns
t_{PHL}						8	15	

¶ t_{PLH} = propagation delay time, low- to high-level output
t_{PHL} = propagation delay time, high- to low-level output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

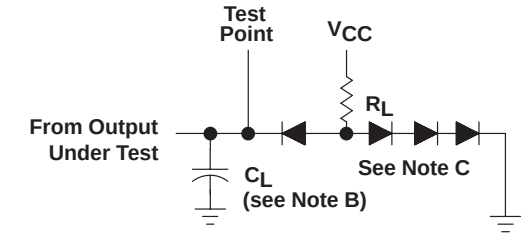


VOLTAGE WAVEFORMS

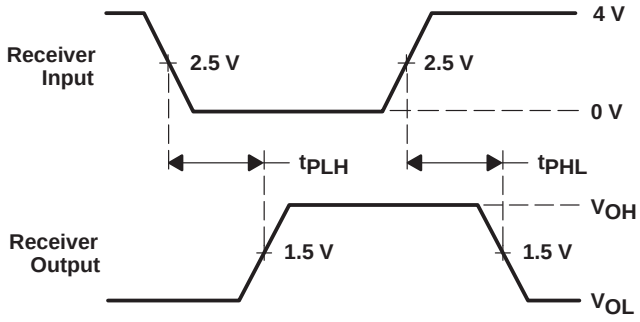
NOTES: A. Input pulses are supplied by generators having the following characteristics: t_W = 100 ns, PRR ≤ 1 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

Figure 1. Propagation Delay Times From Data and Strobe Inputs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: t_W = 100 ns, PRR ≤ 1 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

Figure 2. Propagation Delay Times From Receiver Input

TYPICAL CHARACTERISTICS†

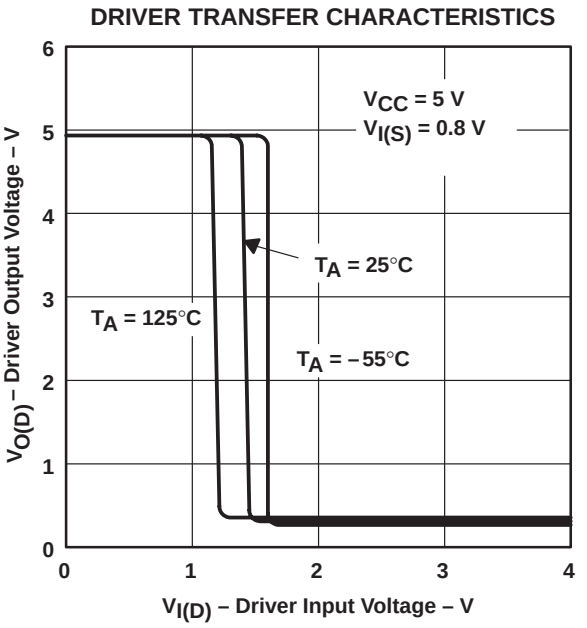


Figure 3

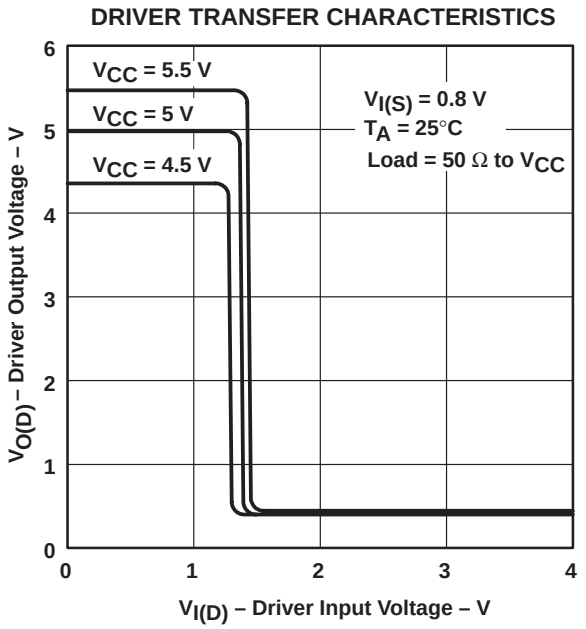


Figure 4

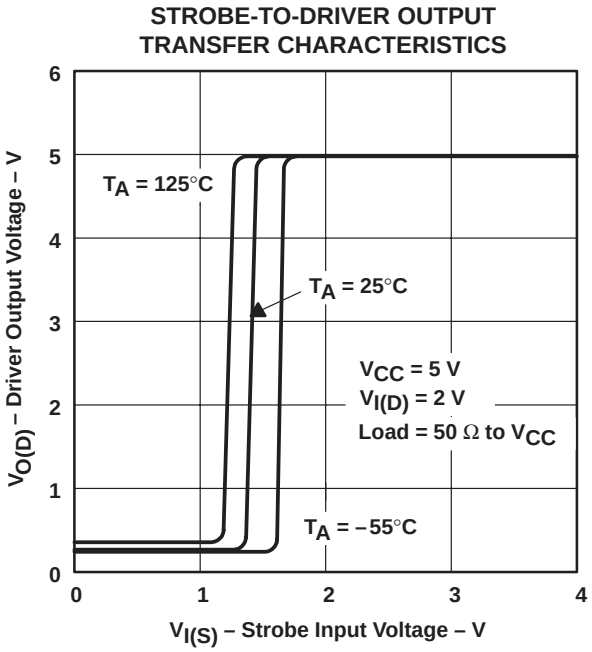


Figure 5

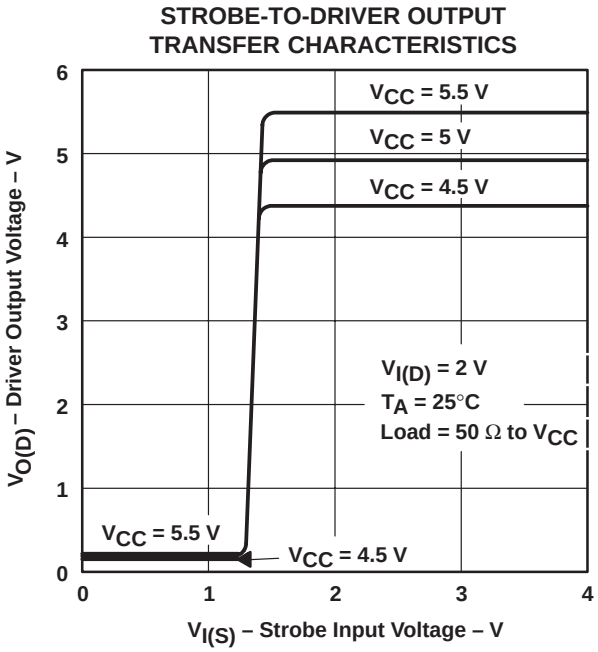


Figure 6

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

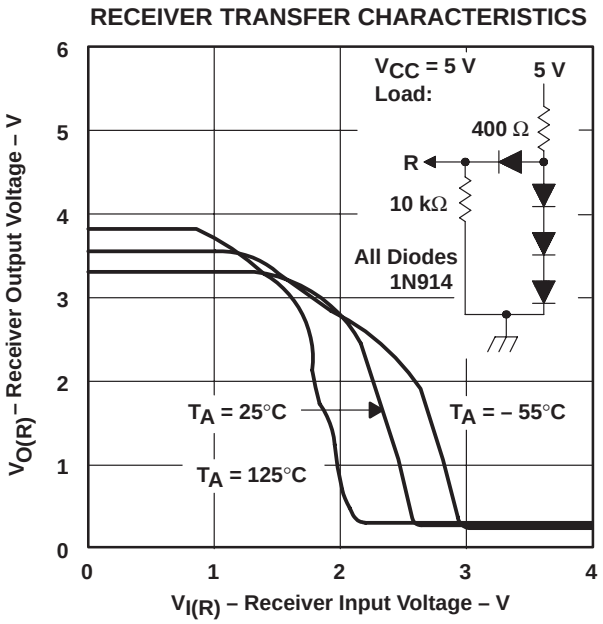


Figure 7

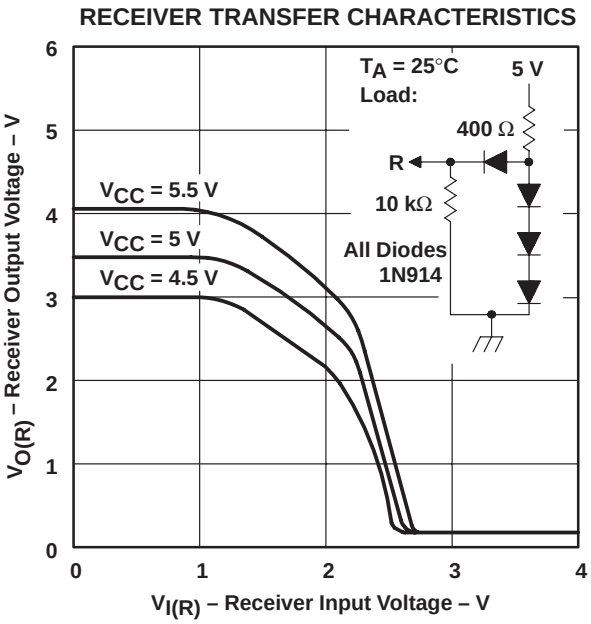


Figure 8

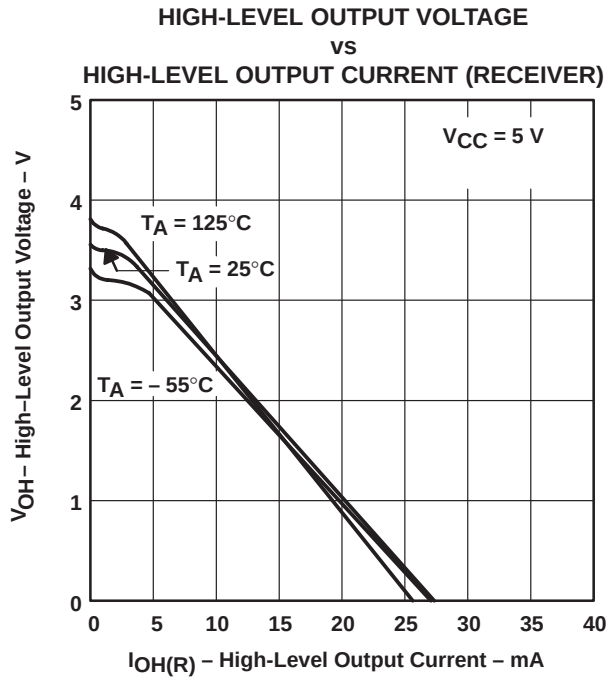


Figure 9

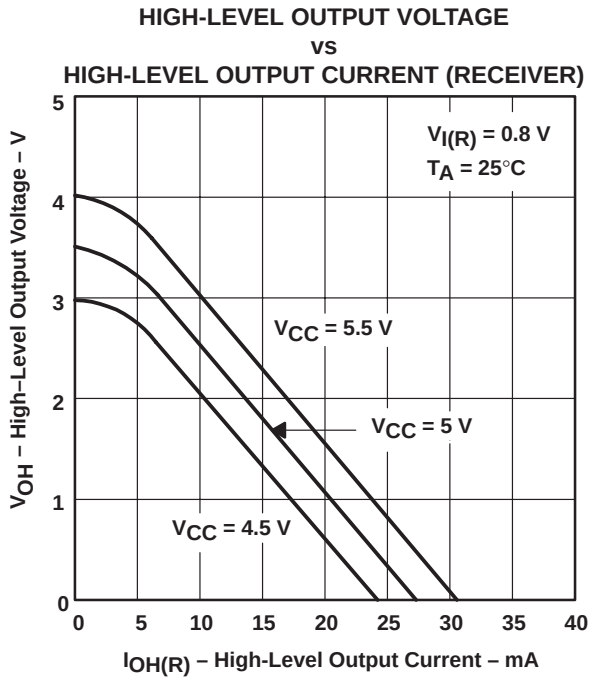


Figure 10

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT (RECEIVER)

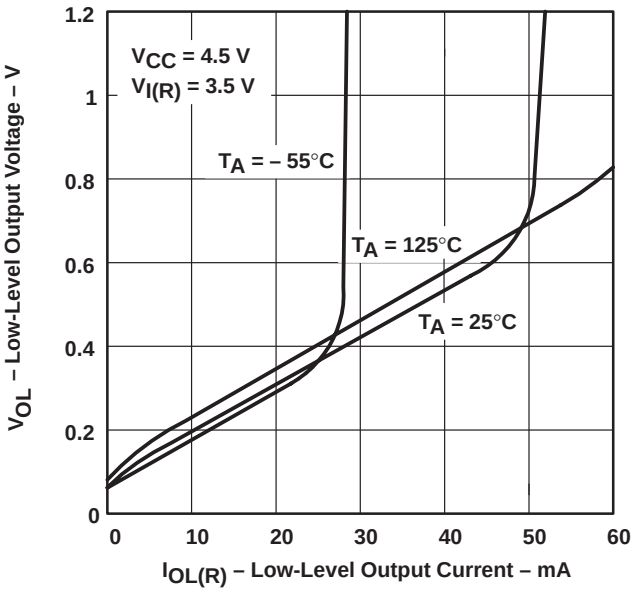


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT (DRIVER)

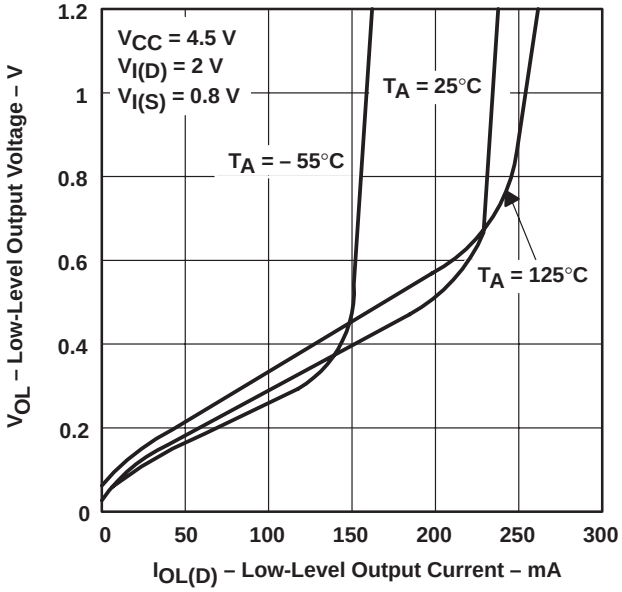


Figure 12

RECEIVER INPUT CURRENT vs RECEIVER INPUT VOLTAGE

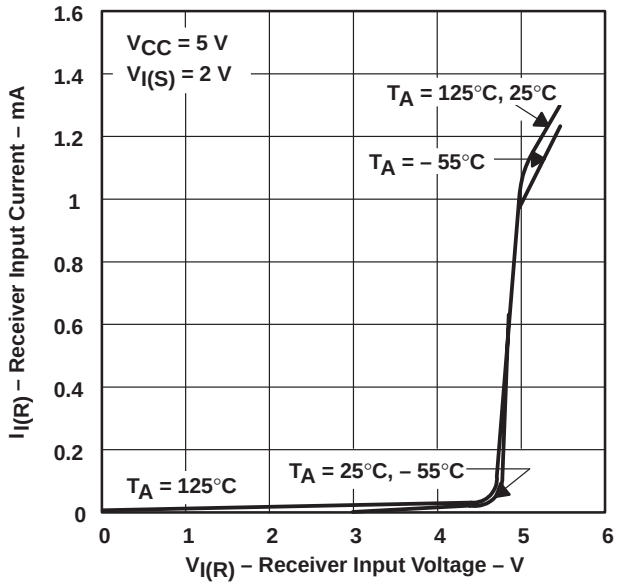


Figure 13

RECEIVER INPUT CURRENT vs RECEIVER INPUT VOLTAGE

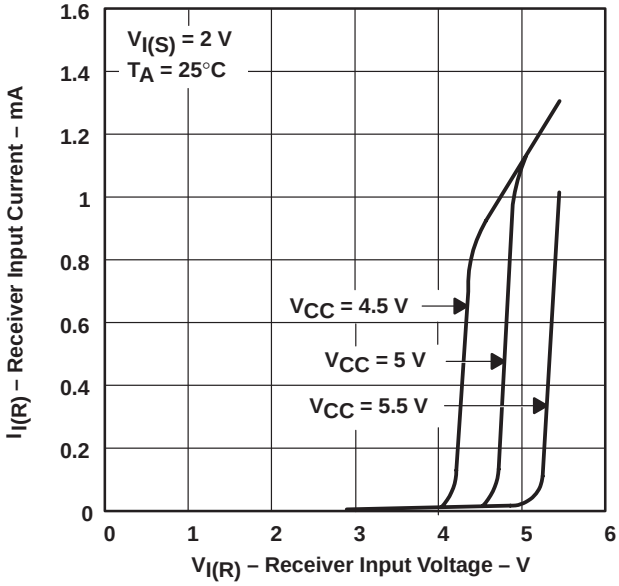


Figure 14

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE (ALL DRIVER OUTPUTS LOW)

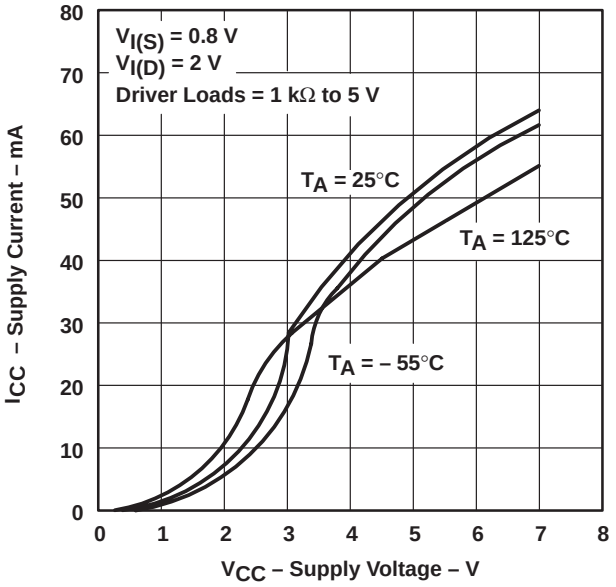


Figure 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

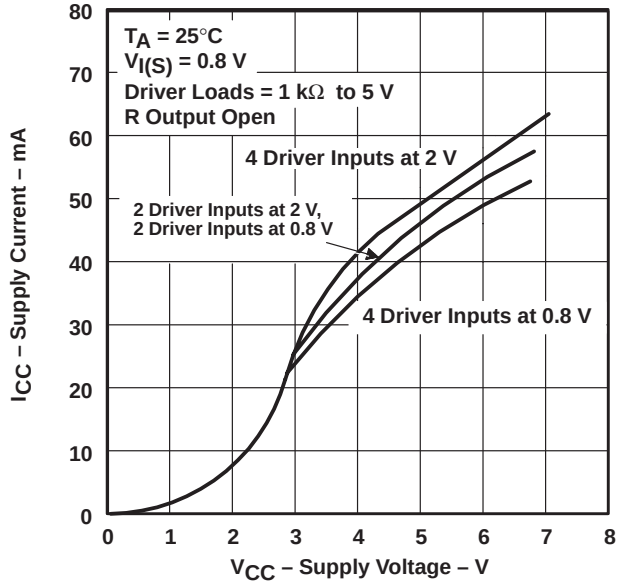


Figure 16

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

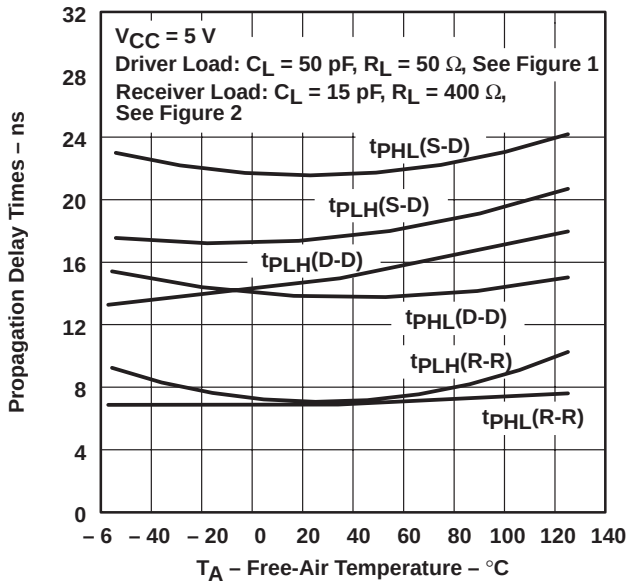


Figure 17

PROPAGATION DELAY TIMES vs SUPPLY VOLTAGE

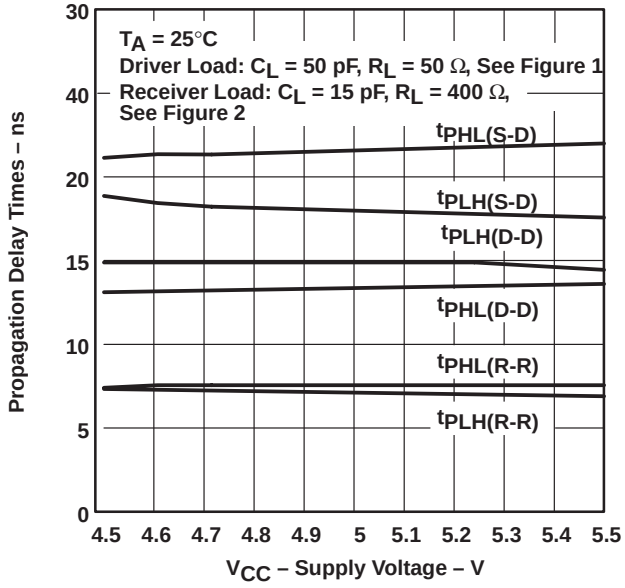


Figure 18

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS

DRIVER
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

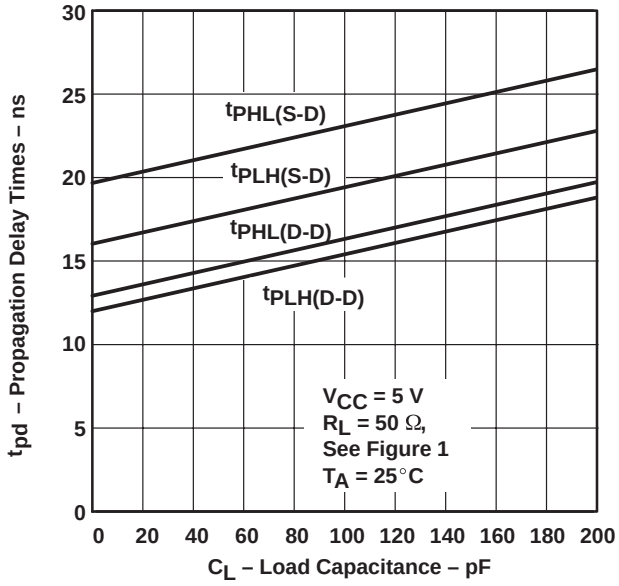


Figure 19

RECEIVER
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

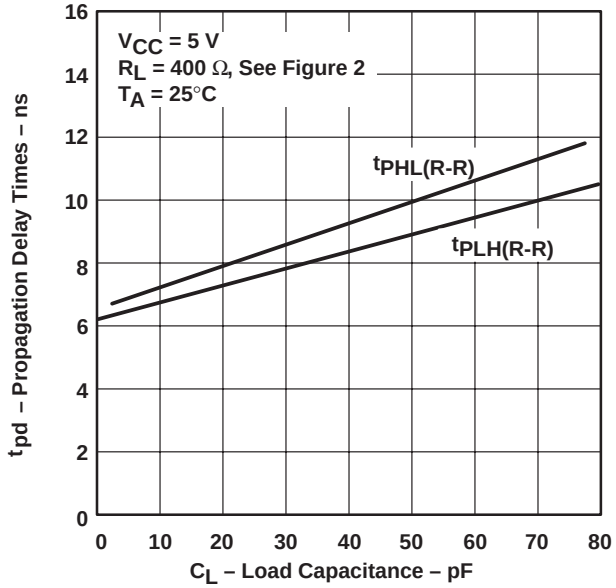
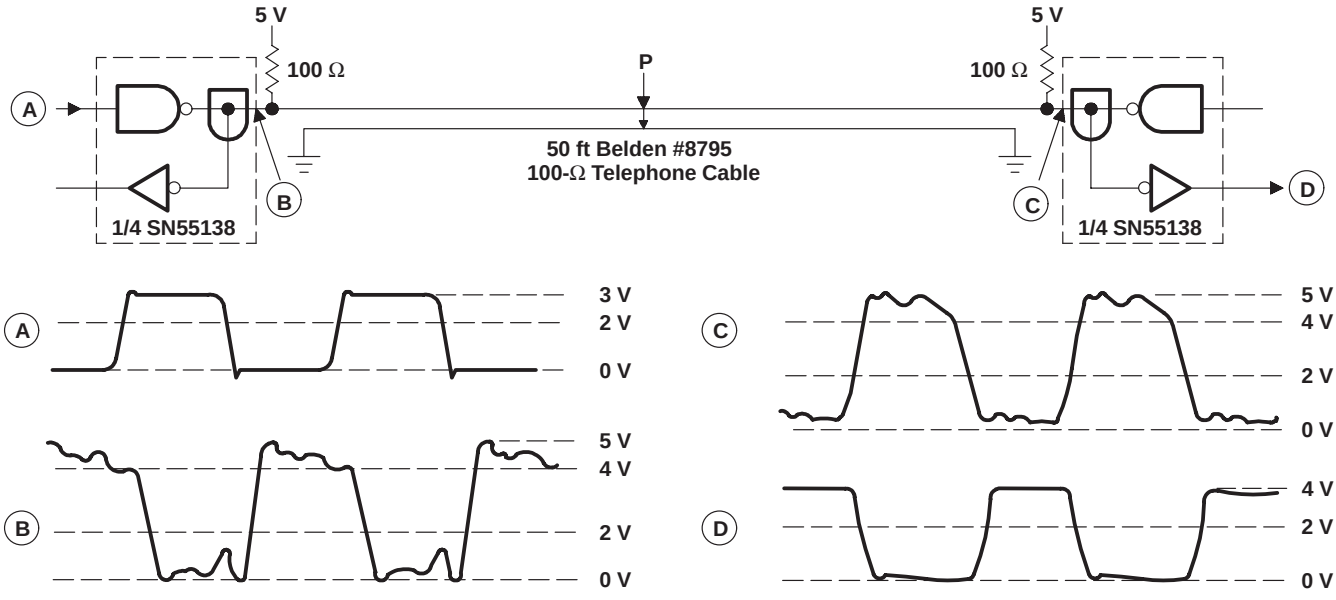


Figure 20

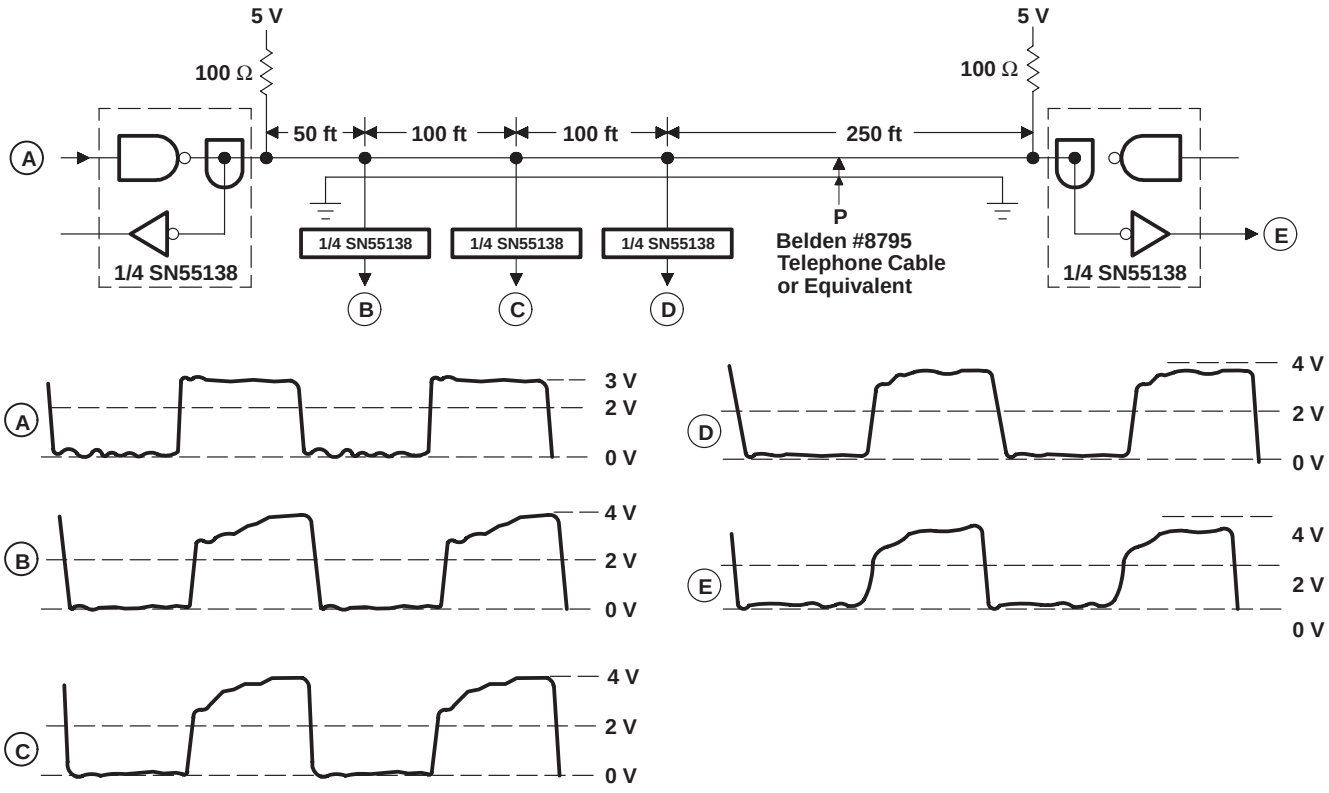
APPLICATION INFORMATION



TYPICAL VOLTAGE WAVEFORMS

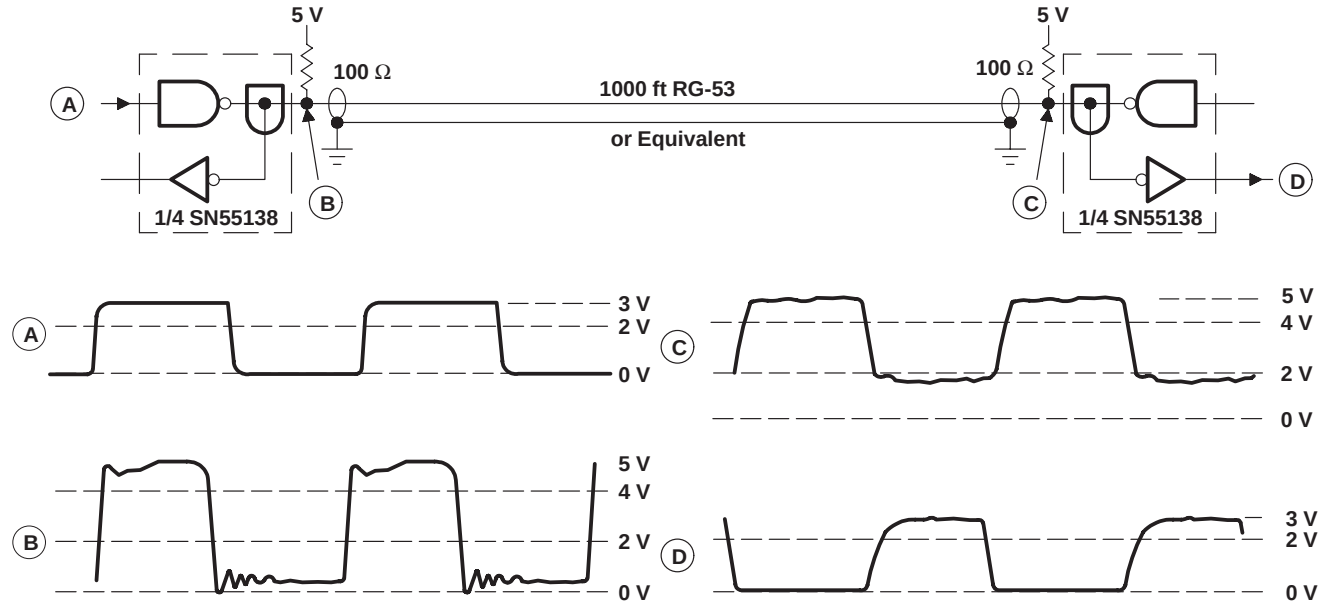
Figure 21. Point-to-Point Communication Over 50 Feet of Twisted Pair at 5 MHz

APPLICATION INFORMATION



TYPICAL VOLTAGE WAVEFORMS

Figure 22. Party-Line Communication on 500 Feet of Twisted Pair at 1 MHz



TYPICAL VOLTAGE WAVEFORMS

Figure 23. Point-to-Point Communication Over 1000 Feet of Coaxial Cable at 1 MHz

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN55138J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75138D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75138NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75138NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75138NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ55138FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ55138J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ55138W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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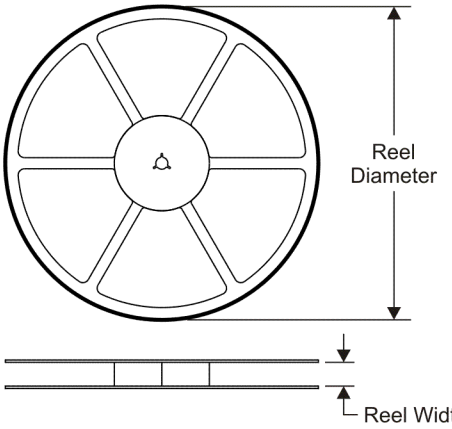
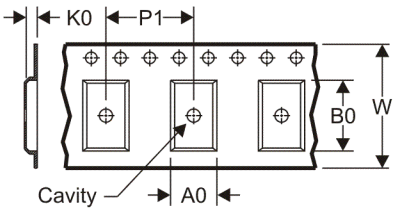
TAPE AND REEL INFORMATION

REEL DIMENSIONS

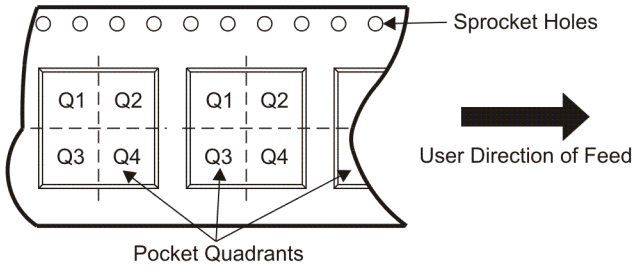


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

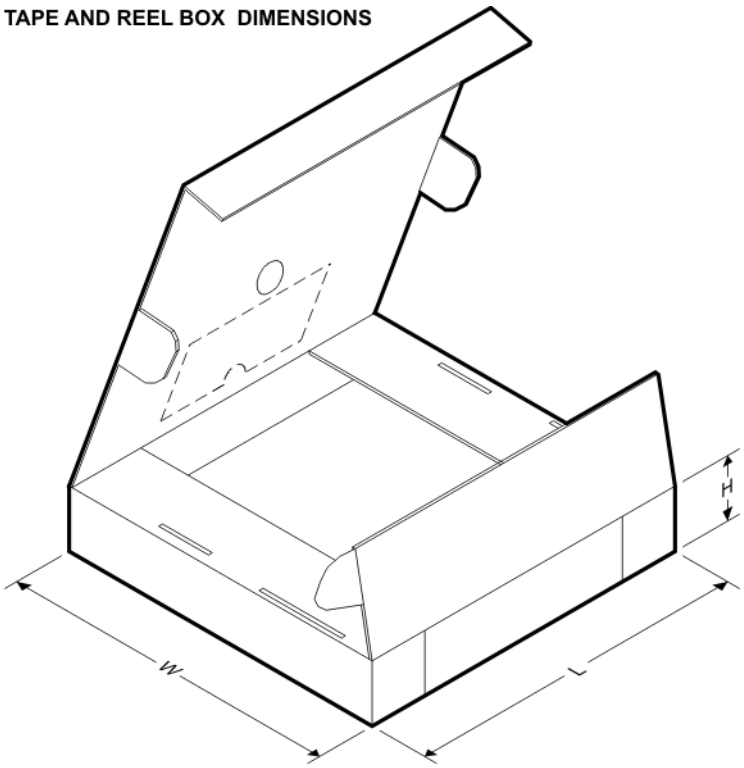
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75138DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75138NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



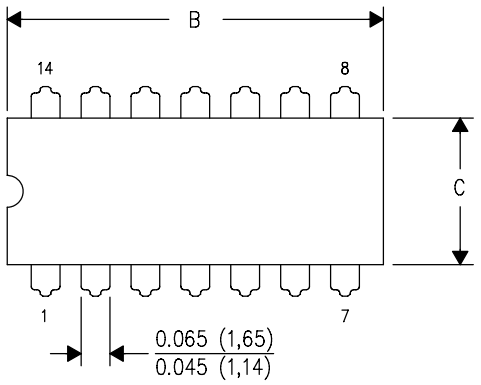
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75138DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75138NSR	SO	NS	16	2000	346.0	346.0	33.0

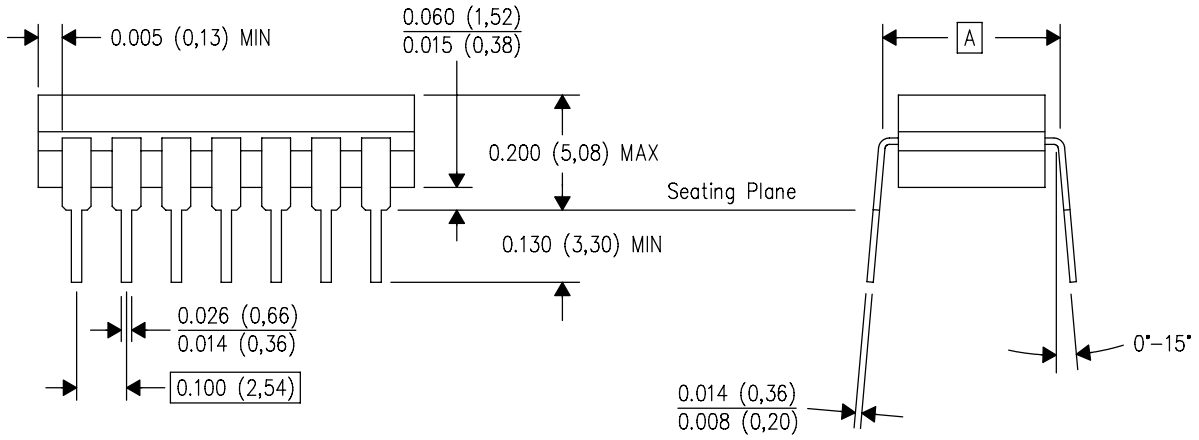
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



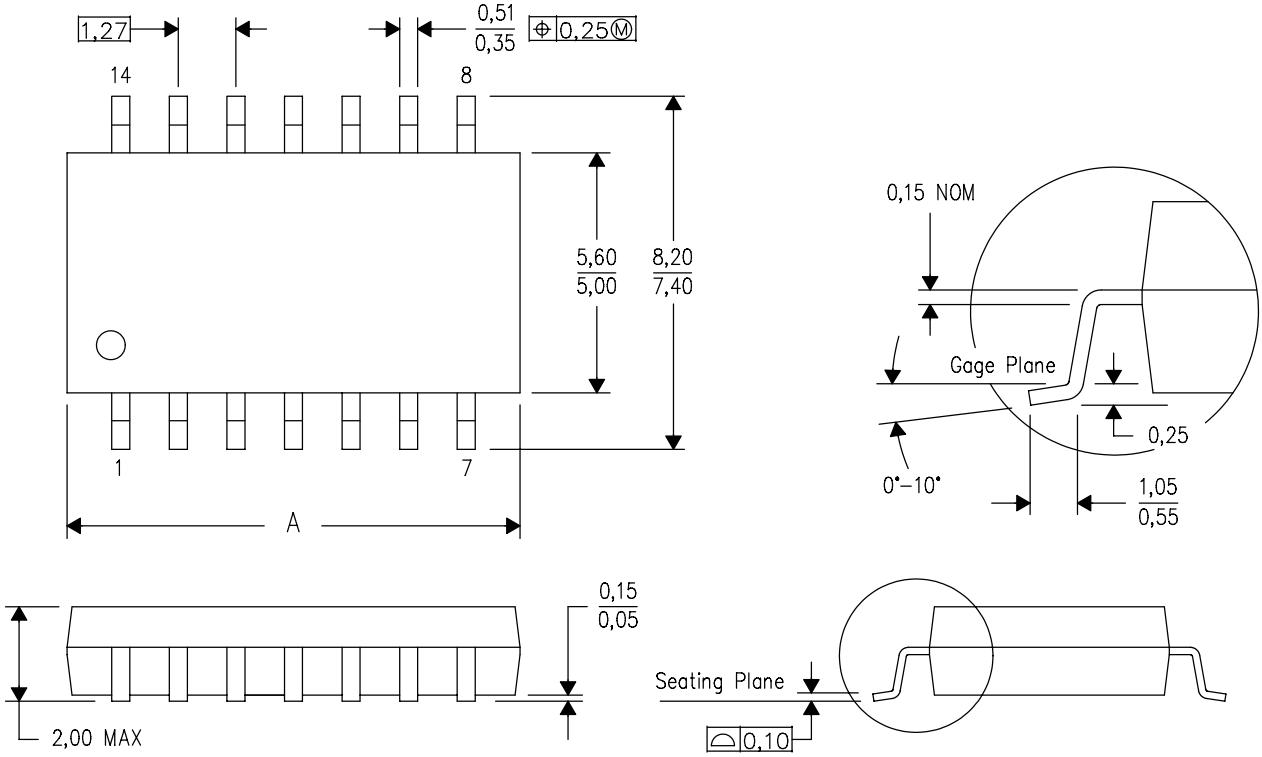
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



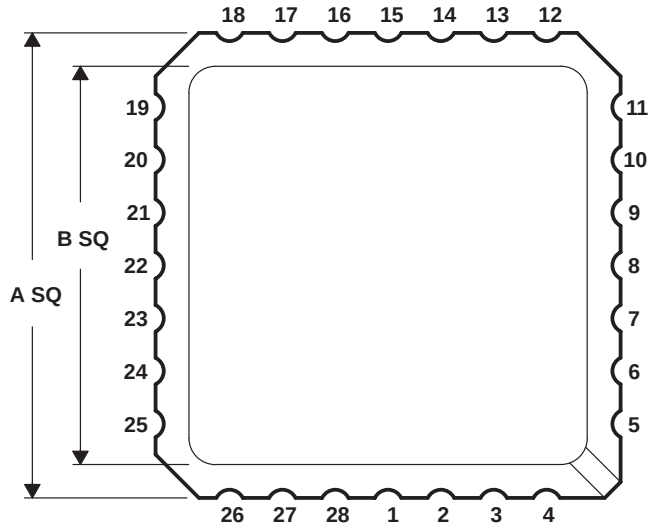
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

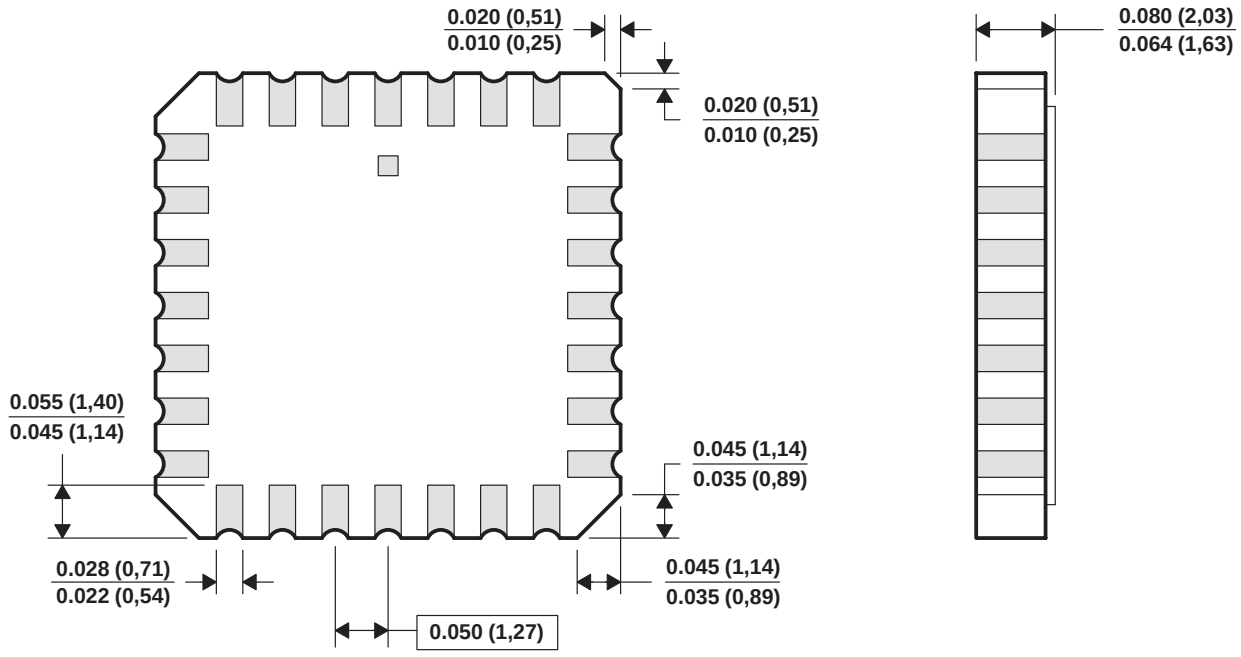
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



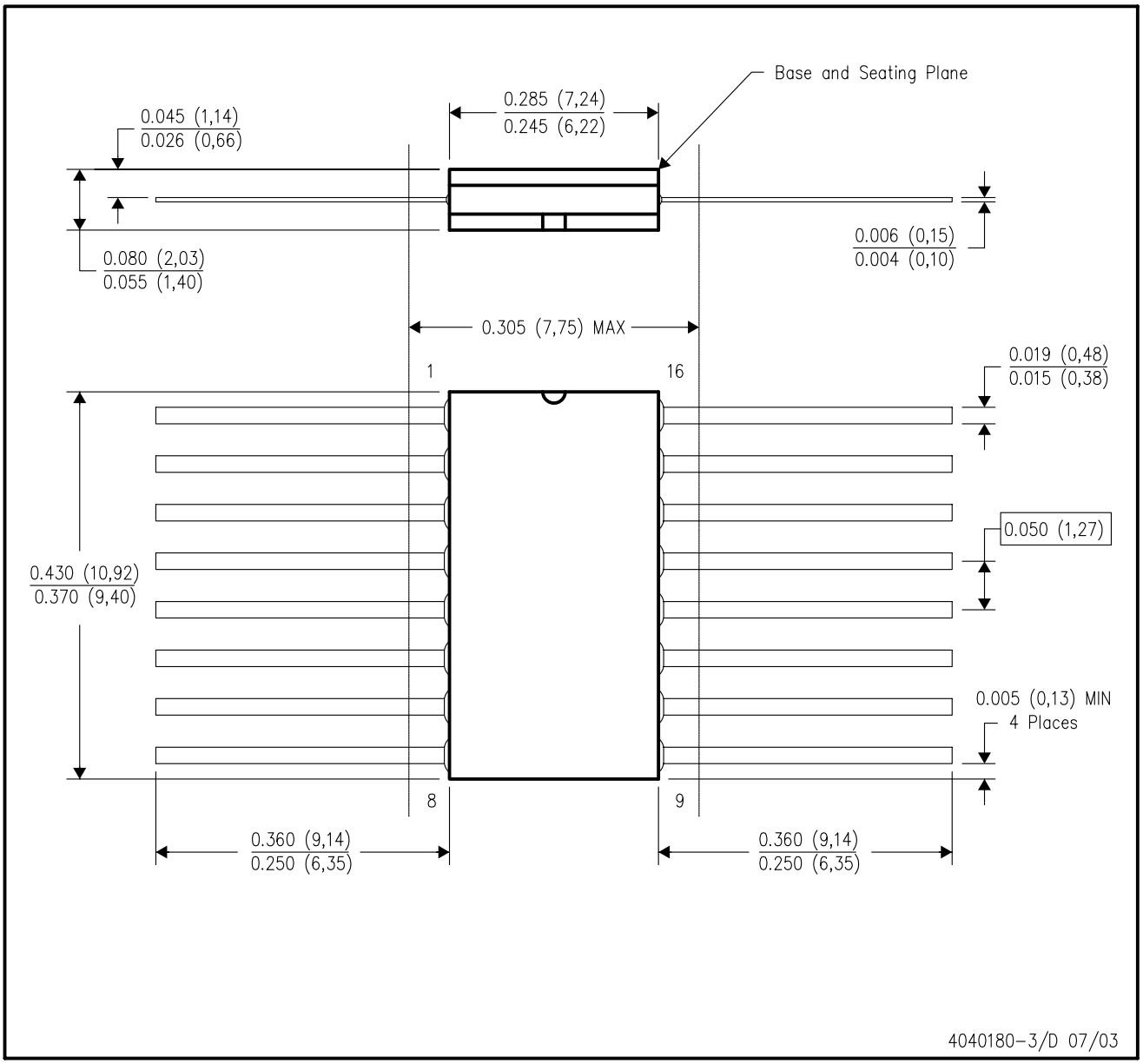
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

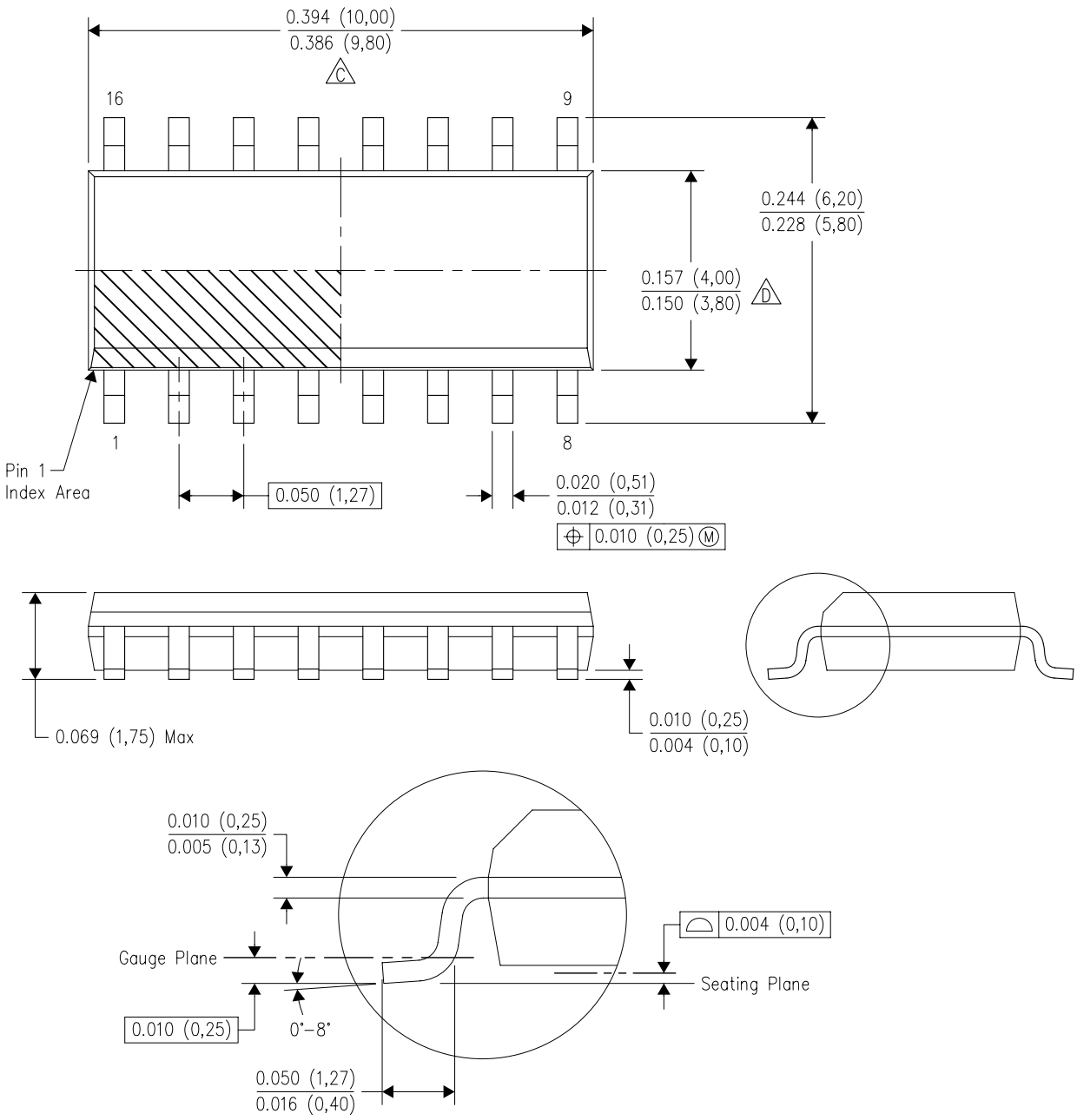
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



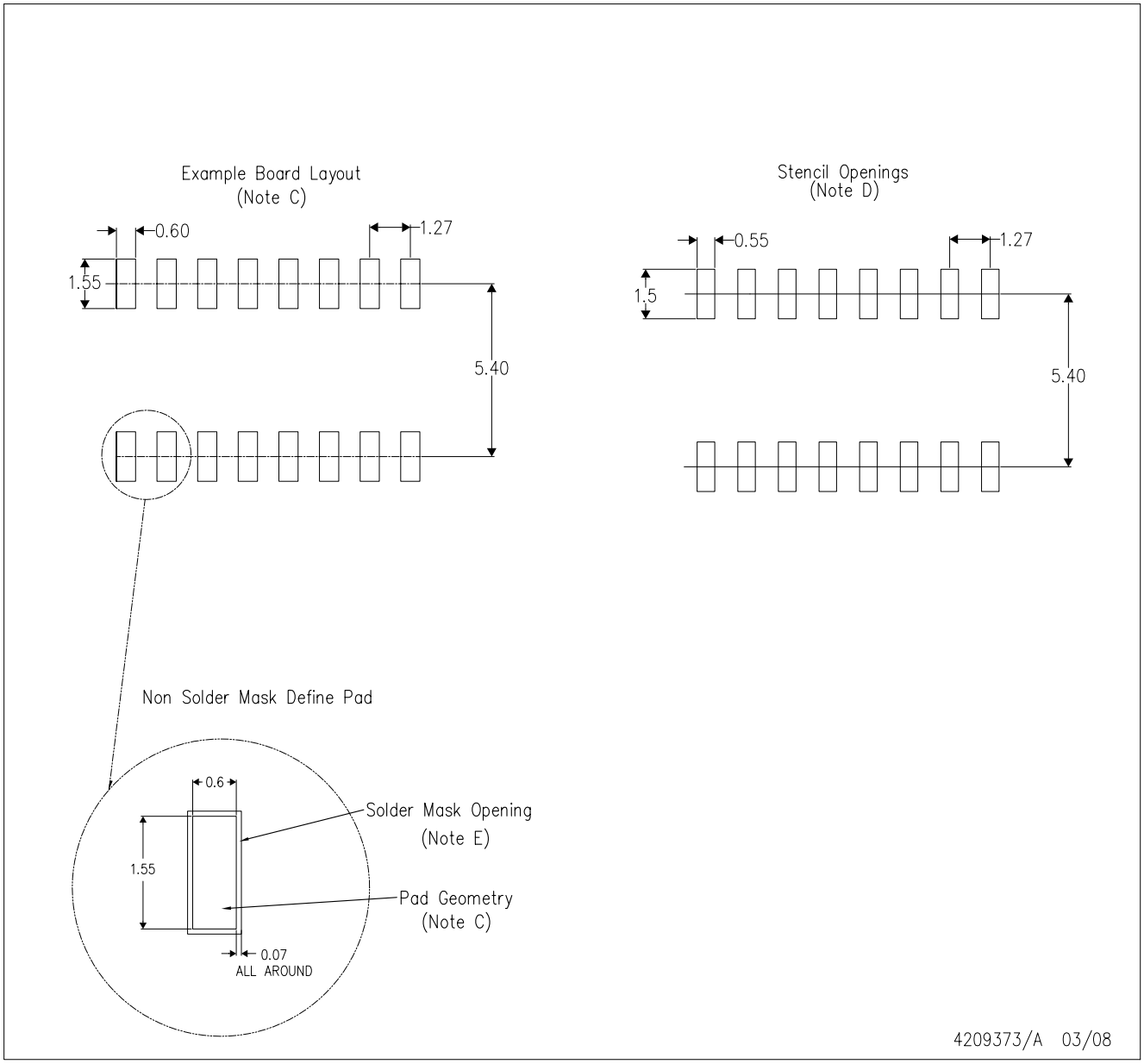
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)

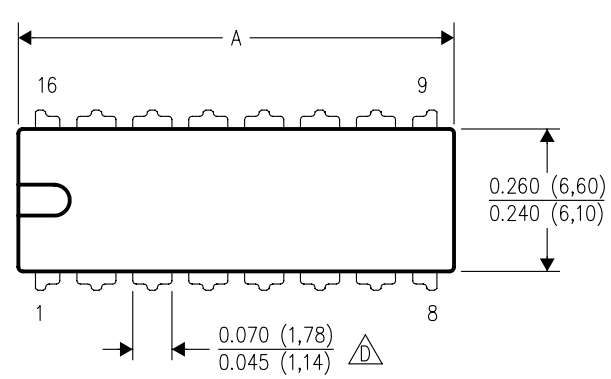


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

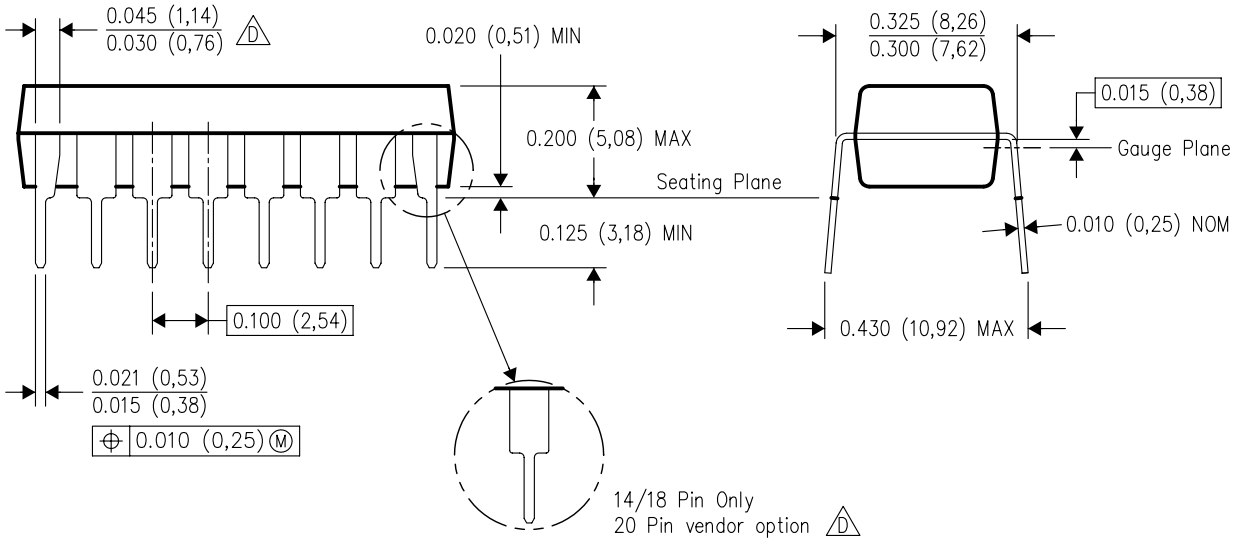
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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