TECHNICAL NOTE

High-performance Regulator IC Series for PCs

Ultra Low Dropout Linear Regulators for PC Chipsets with Power Good

BD3512MUV (3A)

● Description

The BD3512MUV ultra low-dropout linear chipset regulator operates from a very low input supply, and offers ideal performance in low input voltage to low output voltage applications. It incorporates a built-in N-MOSFET power transistor to minimize the input-to-output voltage differential to the ON resistance (R_{ON}=100mΩ) level. By lowering the dropout voltage in this way, the regulator realizes high current output (Iomax=3.0A) with reduced conversion loss, and thereby obviates the switching regulator and its power transistor, choke coil, and rectifier diode. Thus, the BD3512MUV is designed to enable significant package profile downsizing and cost reduction. An external resistor allows the entire range of output voltage configurations between 0.65 and 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to whatever power supply sequence is required.

● Features

1) Internal high-precision reference voltage circuit (0.65V±1%)
2) Built-in VCC undervoltage lockout circuit (VCC=3.80V)
3) NRCS (soft start) function reduces the magnitude of in-rush current
4) Internal Nch MOSFET driver offers low ON resistance (65mΩ typ)
5) Built-in current limit circuit (3.0A min)
6) Built-in thermal shutdown (TSD) circuit (Timer latch)
7) Variable output (0.65～2.7V)
8) High-power package VQFN020V4040 : 4.0×4.0×1.0(mm)
9) Tracking function

● Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

Oct. 2008

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Input Voltage 1	VCC	6.0 *1	V
Input Voltage 2	VIN	6.0 *1	V
Input Voltage 3	VCC	6.0 *1	V
Input Voltage 4	VD	1	V
Maximum Output Current	IO	3 *1	A
Enable Input Voltage	Ven	6.0	V
PGOOD Input Voltage	V_{PGOOD}	6.0	V
Power Dissipation 1	Pd1	0.34 *2	W
Power Dissipation 2	Pd2	0.70 *3	W
Power Dissipation 3	Pd3	1.21 *4	W
Power Dissipation 4	Pd4	3.56 *5	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+125	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.
*2 Reduced by 2.7mW/℃ for each increase in Ta≧25℃(no heat sink)
*3 Reduced by 5.6mW for each increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB.)
:No substrate surface copper foil area.
*4 Reduced by 9.7mW for each increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB.)
:4 layers, substrate surface copper foil area 10.29mm^2.
*5 Reduced by 28.5mW for each increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB.)
:4 layers, substrate surface copper foil area 5505mm^2.

●Operating Voltage (Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit
Input Voltage 1	VCC	4.3	5.5	V
Input Voltage 2	VIN	0.7	VCC-1 *6	V
Input Voltage 3	VCC	4.5	5.5	V
Output Voltage Setting Range	Vo	VFB	2.7	V
Enable Input Voltage	Ven	-0.3	5.5	V

*6 VCC and VIN do not have to be implemented in the order listed.
★This product is not designed for use in radioactive environments.

● Electrical Characteristics (Unless otherwise specified, Ta=25℃, Vcc=5V, Ven=3V, VIN=1.7V, R1=3.9KΩ, R2=3.3KΩ)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Bias Current	Icc	-	1.4	2.2	mA	
VCC Shutdown Mode Current	IST	-	0	10	uA	Ven=0V
Maximum Output Current	Io	3.0	-	-	A	
Output Voltage Temperature Coefficient	Tcvo	-	0.01	-	%/℃	
Feedback Voltage 1	VFB1	0.643	0.650	0.657	V	
Feedback Voltage 2	VFB2	0.637	0.650	0.663	V	Io=0 to 3A Tj=-10 to 100℃
Line Regulation 1	Reg.l1	-	0.1	0.5	%/V	Vcc=4.3V to 5.5V
Line Regulation 2	Reg.l2	-	0.1	0.5	%/V	VIN=1.5V to 3.3V
Load Regulation	Reg.L	-	0.5	10	mV	Io=0 to 3A
Minimum dropout voltage	dVo	-	65	100	mV	Io=1A,VIN=1.2V
Standby Discharge Current	Iden	1	-	-	mA	Ven=0V, Vo=1V
[ENABLE]						
Enable Pin Input Voltage High	Enhi	2	-	-	V	
Enable Pin Input Voltage Low	Enlow	-0.2	-	0.8	V	
Enable Input Bias Current	Ien	-	6	10	uA	Ven=3V
[FEEDBACK]						
Feedback Pin Bias Current	IFB	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	Inrcs	14	20	26	uA	Vnrcs=0.5V
NRCS Standby Voltage	VSTB	-	0	50	mV	Ven=0V
[UVLO]						
VCC Undervoltage Lockout Threshold Voltage	VccUVLO	3.5	3.8	4.1	V	Vcc:Sweep-up
VCC Undervoltage Lockout Hysteresis Voltage	Vcchys	100	160	220	mV	Vcc:Sweep-down
VD Undervoltage Lockout Threshold Voltage	V_DUVLO	V_{REF} × 0.6	V_{REF} × 0.7	V_{REF} × 0.8	V	V_D:Sweep-up
[SCP]						
SCP Startup Voltage	V_{OSCP}	V_O × 0.3	V_O × 0.4	V_O × 0.5	V	
SCP Threshold Voltage	V_{SCPTH}	1.05	1.15	1.25	V	
SCP Charge Current	I_{SCP}	1.4	2	2.6	μA	
SCP Standby Voltage	$V_{SCPSTBY}$	-	-	50	mV	
[PGOOD]						
Low-side Threshold Voltage	V_{THPGL}	V_O × 0.87	V_O × 0.9	V_O × 0.93	V	
High-side Threshold Voltage	V_{THPGH}	V_O × 1.07	V_O × 1.1	V_O × 1.13	V	
PGDLY Charge Current	Ipgdly	1.4	2.0	2.6	μA	※
Ron	R_{PG}	-	0.1	-	kΩ	

※PGOOD delay time is determined as in formula below.

$$t_{pgdly} = \frac{C(pF) \times 1.23}{I_{pgdly}(\mu A)} \quad (\mu sec)$$

●Reference Data

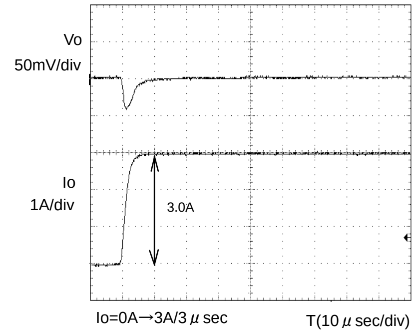


Fig.1 Transient Response
(0→3A)
Co=22μF, Cfb=1000pF

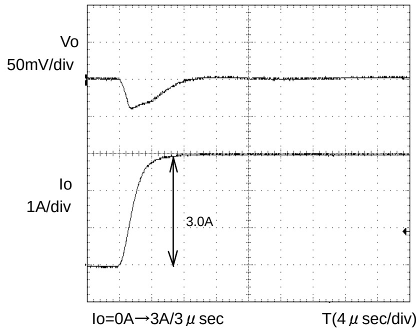


Fig.2 Transient Response
(0→3A)
Co=100μF

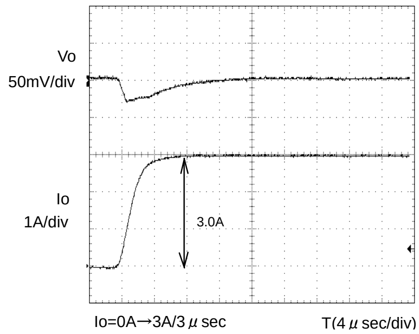


Fig.3 Transient Response
(0→3A)
Co=100μF, Cfb=1000pF

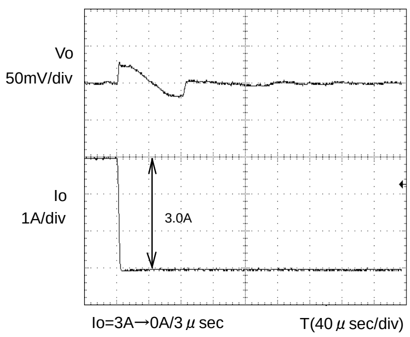


Fig.4 Transient Response
(3→0A)
Co=22μF, Cfb=1000pF

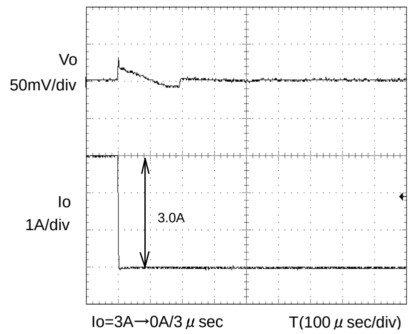


Fig.5 Transient Response
(3→0A)
Co=100μF

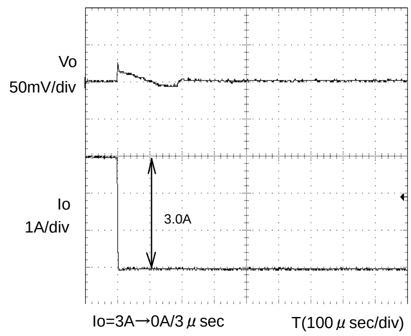


Fig.6 Transient Response
(3→0A)
Co=100μF, Cfb=1000pF

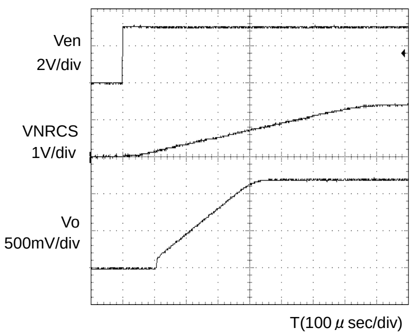


Fig.7 Waveform at output start

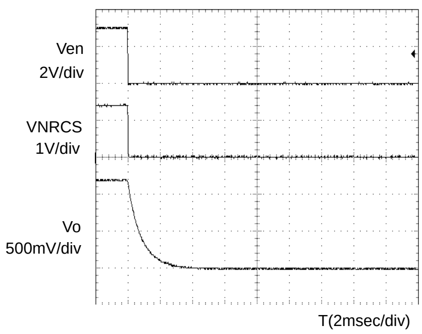


Fig.8 Waveform at output OFF

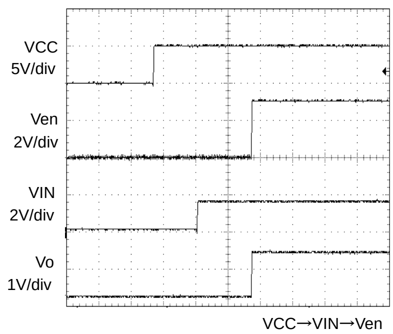


Fig.9 Input sequence

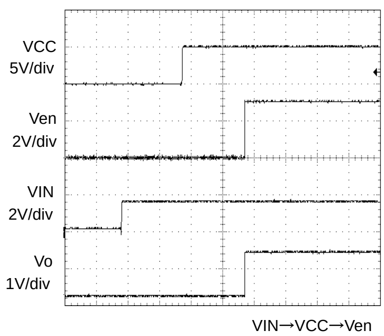


Fig.10 Input sequence

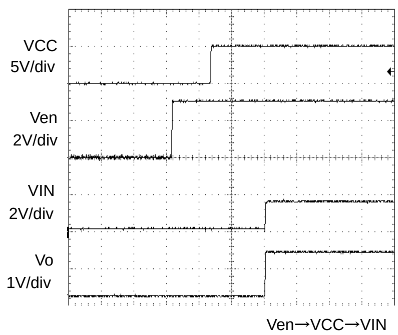


Fig.11 Input sequence

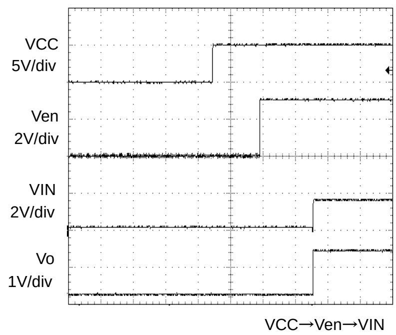


Fig.12 Input sequence

●Reference Data

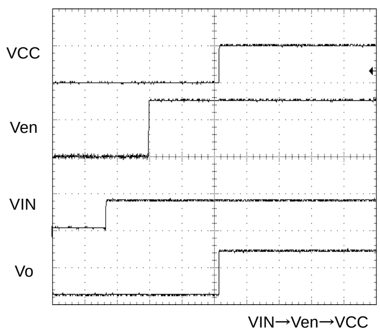


Fig.13 Input sequence

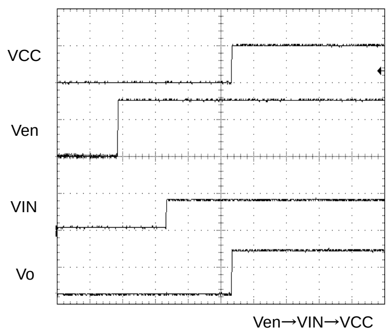


Fig.14 Input sequence

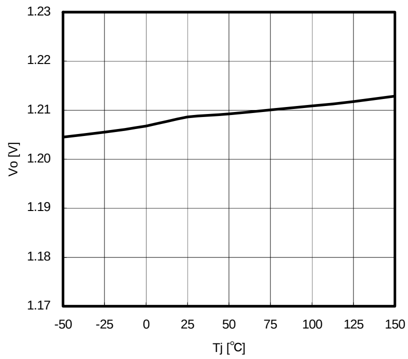


Fig.15 Tj-Vo

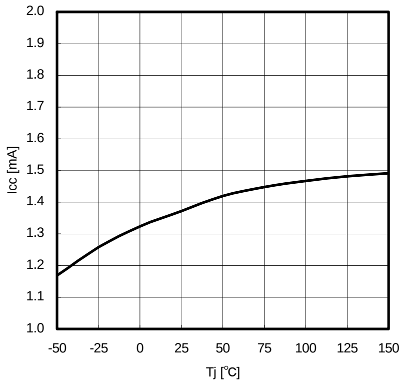


Fig.16 Tj-ICC

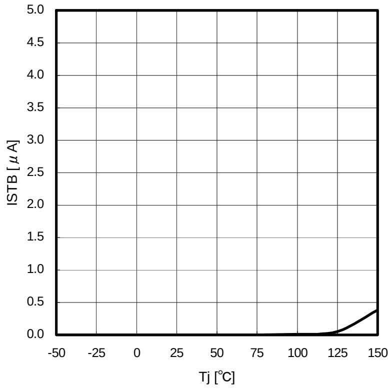


Fig.17 Tj-ISTB

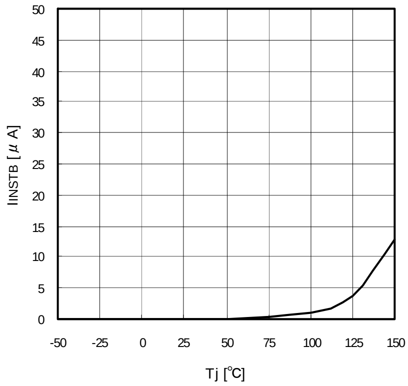


Fig.18 Tj-IINSTB

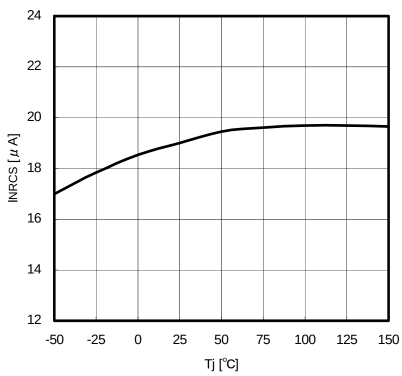


Fig.19 Tj-INRCS

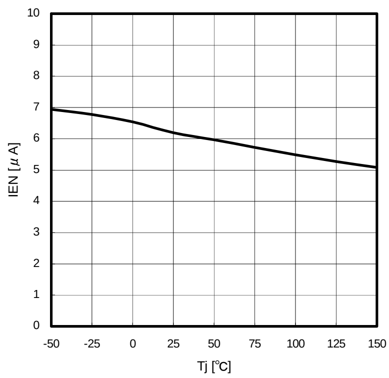


Fig.20 Tj-IEN

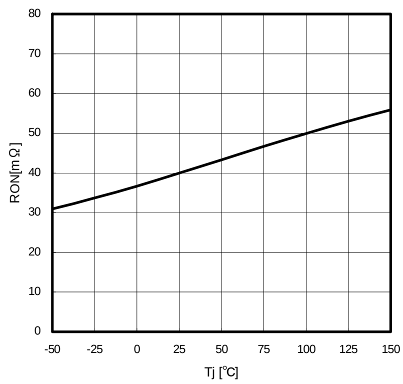


Fig.21 Tj-RON
(VCC=5V/VO=1.2V)

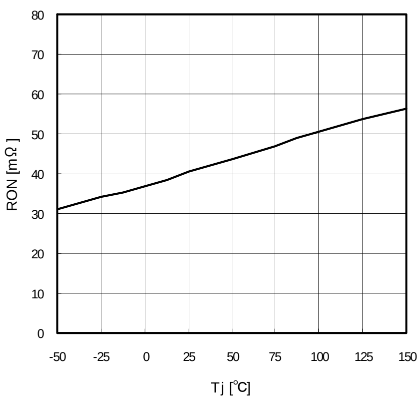


Fig.22 Tj-RON
(VCC=5V/VO=1.5V)

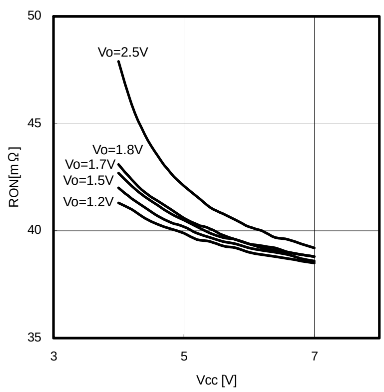
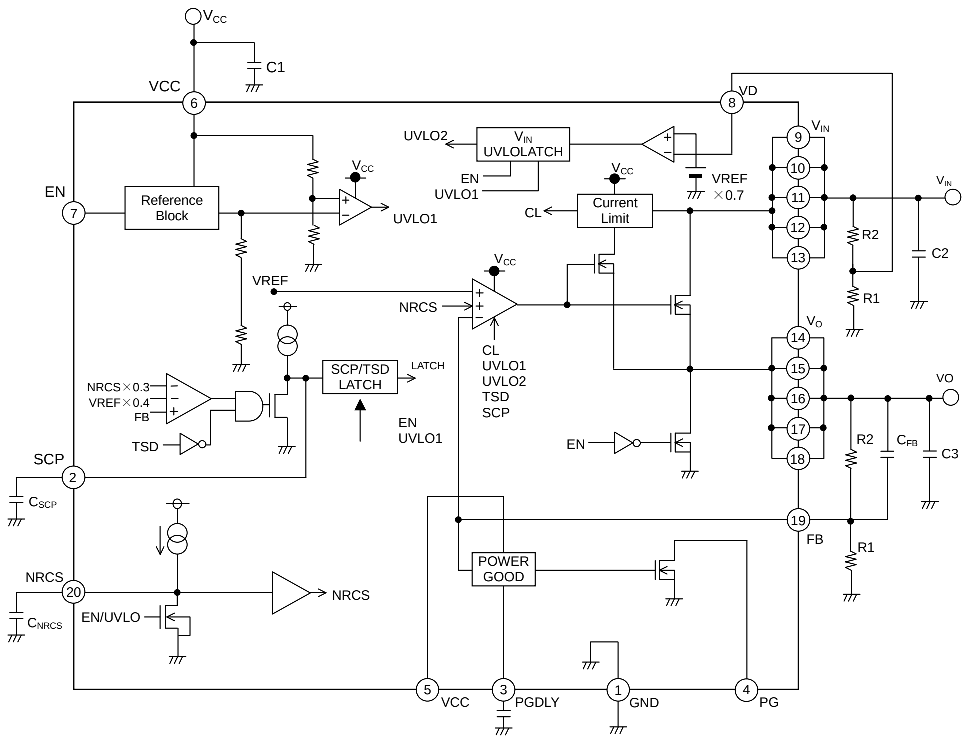
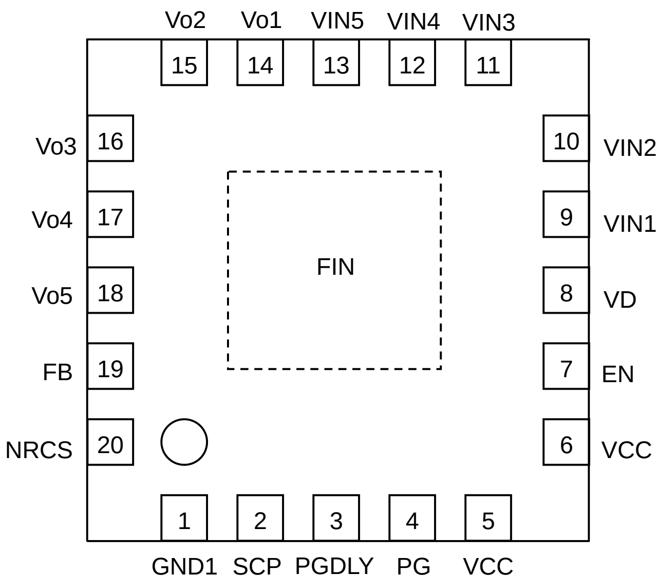


Fig.23 VCC-RON

●Block Diagram



●Pin Layout



●Pin Function Table

PIN No.	PIN name	PIN Function
1	GND1	Ground Pin 1
2	SCP	SCP Delay Time Setting Capacitor Connection Pin
3	PGDLY	PGOOD Delay Setting Capacitor Connection Pin
4	PG	Power Good Pin
5	VCC	Power Supply Pin
6	VCC	Power Supply Pin
7	EN	Enable Input Pin
8	VD	VIN Input Voltage Detect Pin
9	VIN1	Input Voltage Pin 1
10	VIN2	Input Voltage Pin 2
11	VIN3	Input Voltage Pin 3
12	VIN4	Input Voltage Pin 4
13	VIN5	Input Voltage Pin 5
14	Vo1	Output Voltage Pin 1
15	Vo2	Output Voltage Pin 2
16	Vo3	Output Voltage Pin 3
17	Vo4	Output Voltage Pin 4
18	Vo5	Output Voltage Pin 5
19	FB	Reference Voltage Feedback Pin
20	NRCS	In-rush Current Protection (NRCS) Capacitor Connection Pin
bottom	FIN	Connected to heatsink and GND

* Please short N.C to the GND line.

●Operation of Each Block

・AMP

This is an error amp compares the reference voltage (0.65V) with V_O to drive the output Nch FET (Ron=50mΩ). Frequency optimization helps to realize rapid transient response, and to support the use of ceramic capacitors on the output. AMP input voltage ranges from GND to 2.7V, while the AMP output ranges from GND to V_{CC}. When EN is OFF, or when UVLO is active, output goes LOW and the output of the NchFET switches OFF.

・EN

The EN block controls the regulator's ON/OFF state via the EN logic input pin. In the OFF position, circuit voltage is maintained at 0μA, thus minimizing current consumption at standby. The FET is switched ON to enable discharge of the NRCS pin V_O, thereby draining the excess charge and preventing the IC on the load side from malfunctioning. Since no electrical connection is required (e.g. between the V_{CC} pin and the ESD prevention diode), module operation is independent of the input sequence.

・UVLO

To prevent malfunctions that can occur during a momentary decrease in V_{CC}, the UVLO circuit switches the output OFF, and (like the EN block) discharges NRCS and V_O. Once the UVLO threshold voltage (TYP3.80V) is reached, the power-on reset is triggered and output continues.

・CURRENT LIMIT

When output is ON, the current limit function monitors the internal IC output current against the parameter value. When current exceeds this level, the current limit module lowers the output current to protect the load IC. When the overcurrent state is eliminated, output voltage is restored to the parameter value.

・NRCS (Non Rush Current on Start-up)

The soft start function enabled by connecting an external capacitor between the NRCS pin and ground. Output ramp-up can be set for any period up to the time the NRCS pin reaches V_{FB} (0.65V). During startup, the NRCS pin serves as a 20μA (TYP) constant current source to charge the external capacitor. Capacitors with low susceptibility (0.001μF～1μF) to temperature are recommended, in order to assure a stable soft-start time.

・TSD (Thermal Shut down)

The shutdown (TSD) circuit automatically is latched OFF when the chip temperature exceeds the threshold temperature after the programmed time period elapses, thus serving to protect the IC against "thermal runaway" and heat damage. Because the TSD circuit is intended to shut down the IC only in the presence of extreme heat, it is crucial that the Tj (max) parameter not be exceeded in the thermal design, in order to avoid potential problems with the TSD.

・VIN

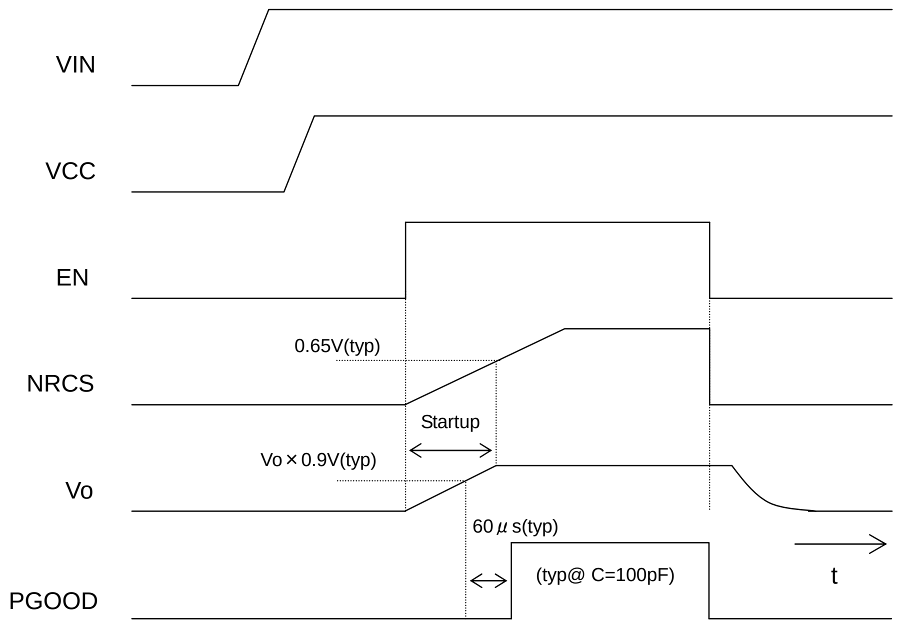
The V_{IN} line acts as the major current supply line, and is connected to the output NchFET drain. Since no electrical connection (such as between the V_{CC} pin and the ESD protection diode) is necessary, V_{IN} operates independent of the input sequence. However, since an output NchFET body diode exists between V_{IN} and V_O, a V_{IN}-V_O electric (diode) connection is present. Note, therefore, that when output is switched ON or OFF, reverse current may flow to V_{IN} from V_O.

・PGOOD

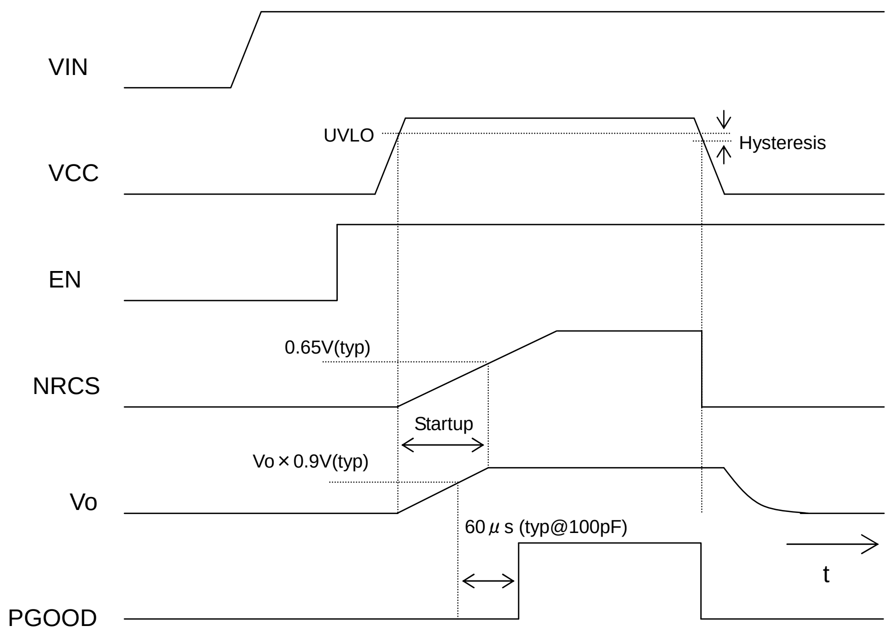
It outputs the status of the output voltage. This is open drain pin and connects to V_{CC} pin through the pull-up resistance (100kΩ or so). When the output voltage range is $V_O \times 0.9$ to $V_O \times 1.1$(TYP), the status is high.

●Timing Chart

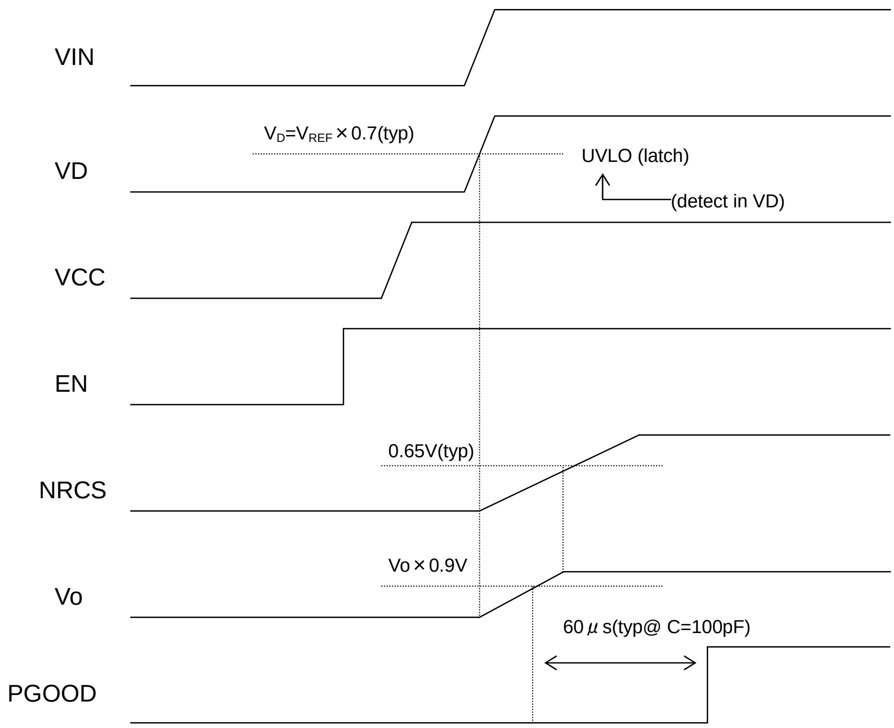
EN ON/OFF



VCC ON/OFF

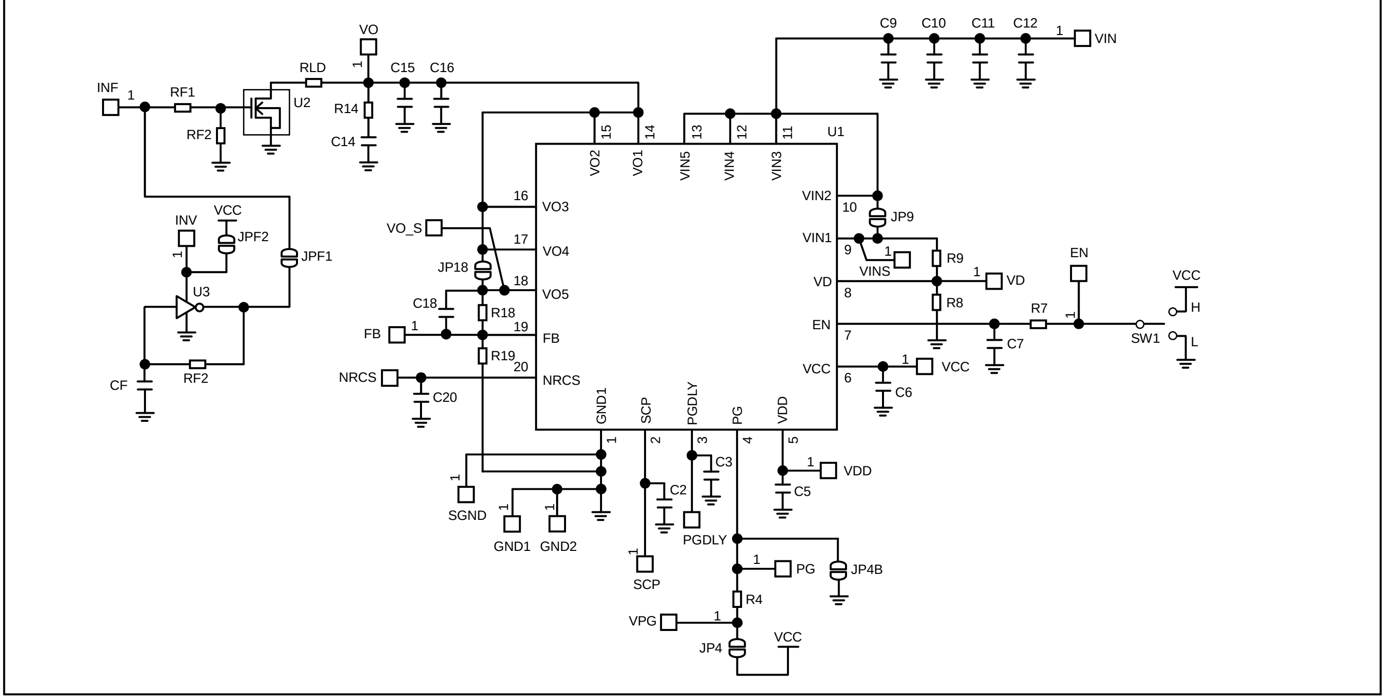


VIN ON/OFF


VIN
VD
VCC
EN
NRCS
Vo
PGOOD
VD=VREF×0.7(typ)
UVLO (latch)
(detect in VD)
0.65V(typ)
Vo×0.9V
60μs(typ@ C=100pF)

●Evaluation Board

■ BD3512MUV Evaluation Board Schematic



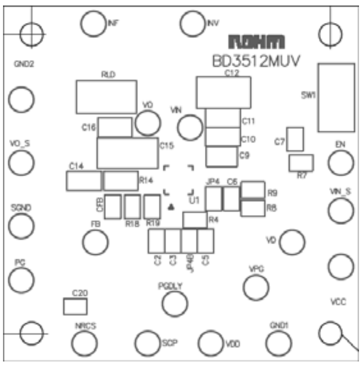
■ BD3512MUV Evaluation Board Standard Component List

Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD3512MUV
C2	100pF	MURATA	CRM1882C1H101JA01
C3	100pF	MURATA	CRM1882C1H101JA01
R4	100kΩ	ROHM	MCR03EZPF1003
C5	0.1uF	KYOCERA	CM05104K10A
C6	1uF	KYOCERA	CM105B105K06A
R7	0Ω	-	jumper

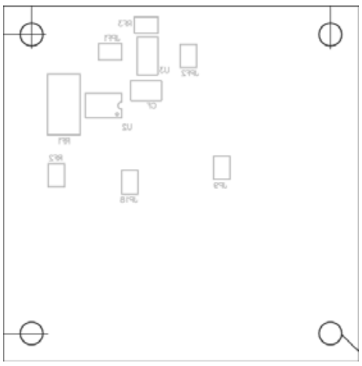
Component	Rating	Manufacturer	Product Name
R8	3.9kΩ	ROHM	MCR03EZPF3901
R9	3.3kΩ	ROHM	MCR03EZPF3301
C9	10uF	KYOCERA	CM21B106M06A
C16	22uF	KYOCERA	CM316B226M06A
R18	3.3kΩ	ROHM	MCR03EZPF3301
R19	3.9kΩ	ROHM	MCR03EZPF3901
V20	0.01uF	MURATA	GRM188B11H102KA01

■ BD3512MUV Evaluation Board Layout

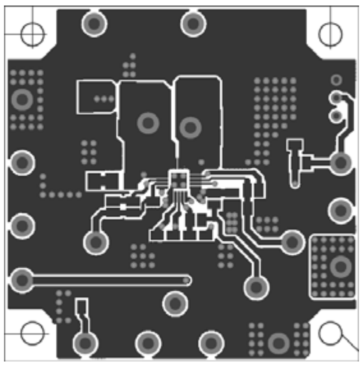
Silk Screen (Top)



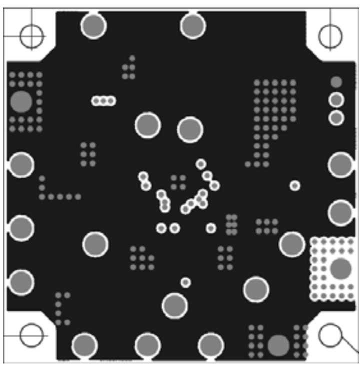
Silk Screen (Bottom)



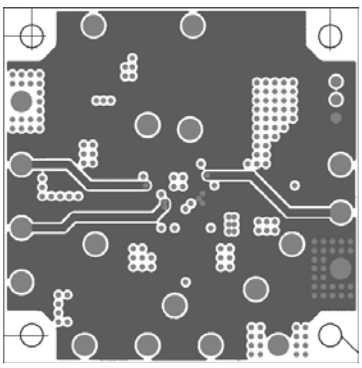
TOP Layer



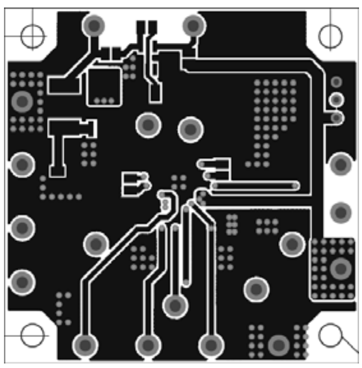
Middle Layer_1



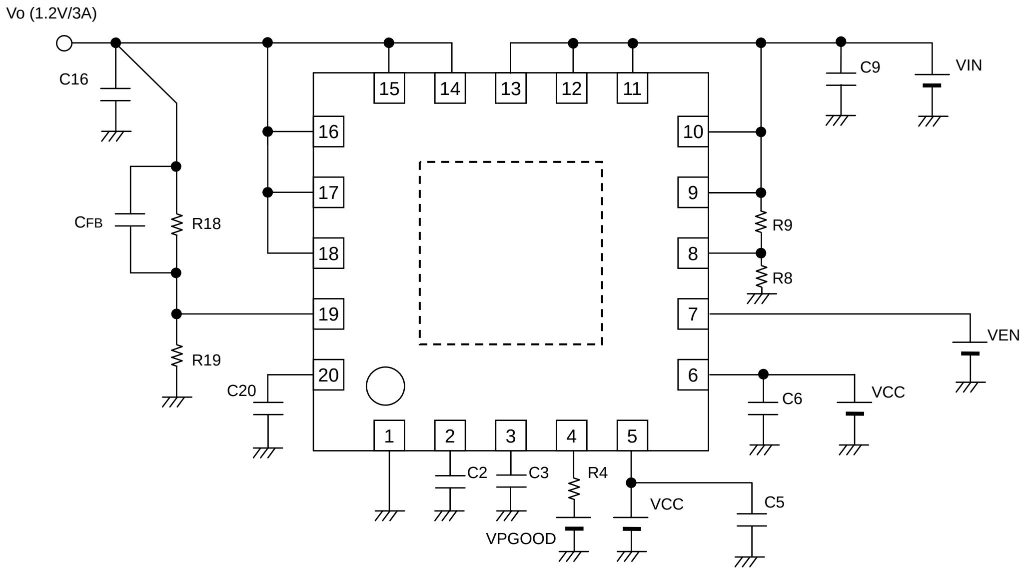
Middle Layer_2



Bottom Layer



●Recommended Circuit Example



Component	Recommended Value	Programming Notes and Precautions
R18/R19	3.3k/3.9k	IC output voltage can be set with a configuration formula V_{FB} × (R18+R19)/R19 using the values for the internal reference output voltage (V_{FB}) and the output voltage resistors (R18, R19). Select resistance values that will avoid the impact of the FB bias current (±100nA). The recommended total resistance value is 10KΩ.
R4	100k	This is the pull-up resistance for open drain pin. It is recommended to set the value about 100kΩ.
C16	22μF	To assure output voltage stability, please be certain the Vo1～Vo5 pins and the GND pins are connected. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22μF ceramic capacitor is recomended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.
C6/C5	1μF/0.1μF	Input capacitors reduce the output impedance of the voltage supply source connected to the (VCC) input pins. If the impedance of this power supply were to increase, input voltage (VCC) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 1μF / 0.1μF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C9	10μF	Input capacitors reduce the output impedance of the voltage supply source connected to the (VIN) input pins. If the impedance of this power supply were to increase, input voltage (VIN) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 10μF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C20	0.01μF	The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (VIN to VO) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.
C_{FB}	1000pF	This component is employed when the C16 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.

●Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature Ta can be no higher than 100 ℃.
2. Chip junction temperature (Tj) can be no higher than 150℃.

Chip junction temperature can be determined as follows:

① Calculation based on ambient temperature (Ta)

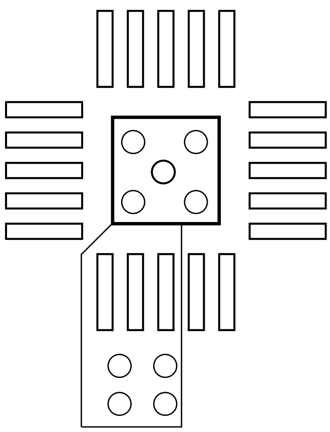
$Tj=Ta+\theta j\text{-}a \times W$

＜Reference values＞

θj-a:VQFN020V4040	249.5℃/W	IC only
	160.1℃/W	1-layer substrate (copper foil area : $0mm^2$)
	82.6℃/W	4-layer substrate (copper foil area : $10.29mm^2$)
	31.2℃/W	4-layer substrate (copper foil area : $5505mm^2$)

Substrate size: $74.2 \times 74.2 \times 1.6mm^3$ (substrate with thermal via)

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). This package is so small (size: 2.9mm×3.0mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA like the figure below enable to get the superior heat radiation characteristic. (This figure is the image. It is recommended that the VIA size and the number is designed suitable for the actual situation.).



Most of the heat loss that occurs in the BD3512MUV is generated from the output Nch FET. Power loss is determined by the total V_{IN}-Vo voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the V_{IN} and Vo in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD3512MUV) make certain to factor conditions such as substrate size into the thermal design.

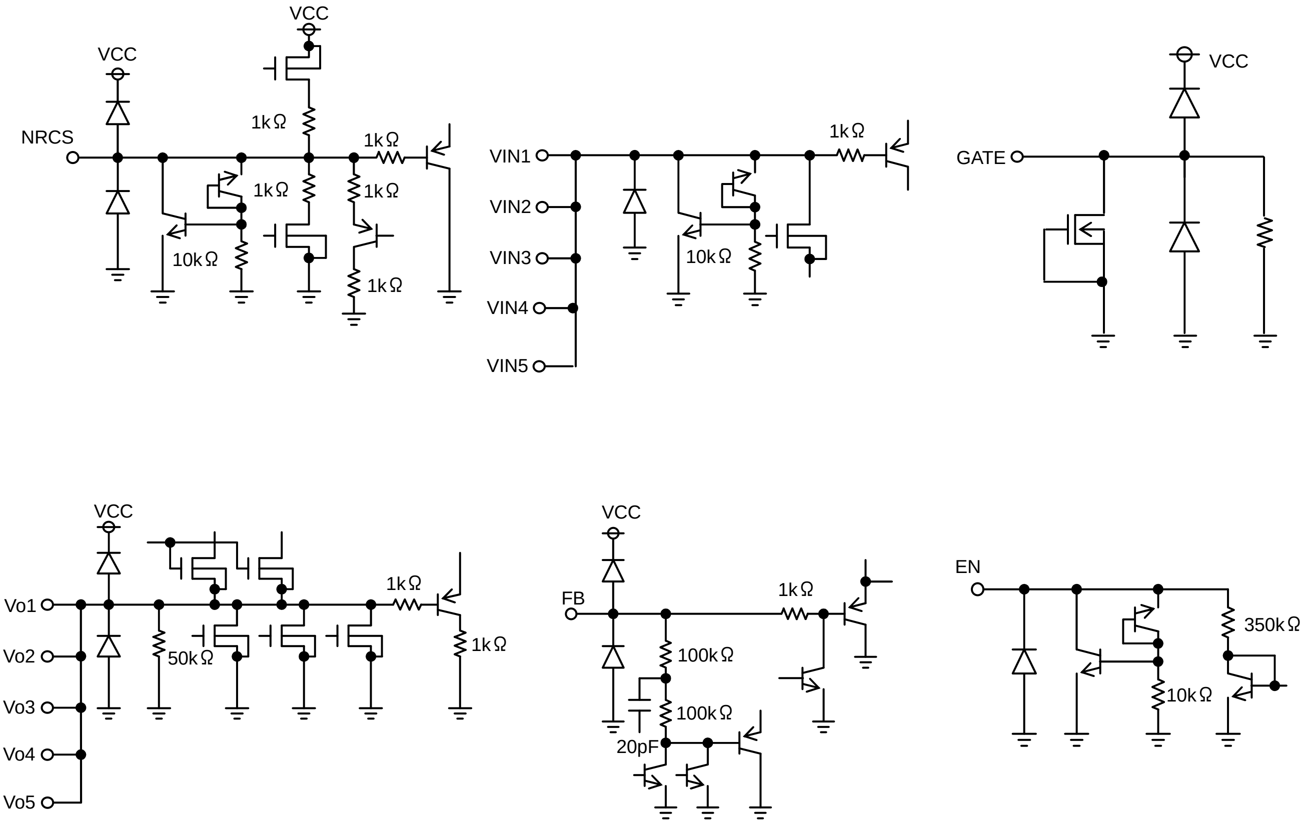
Power consumption (W) = {Input voltage (VIN)- Output voltage (Vo) (Vo≒VREF)} ×Io(Ave)

Example) Where VIN=1.5V, VO=1.25V, Io(Ave) = 4A,

Power consumption (W) = {1.5(V)-1.2(V)} ×4.0(A)

= 1.0(W)

●Input-Output Equivalent Circuit Diagram



●Operation Notes

1. Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward
Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines
Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage
The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
BD3512MUV	175	15

10. Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

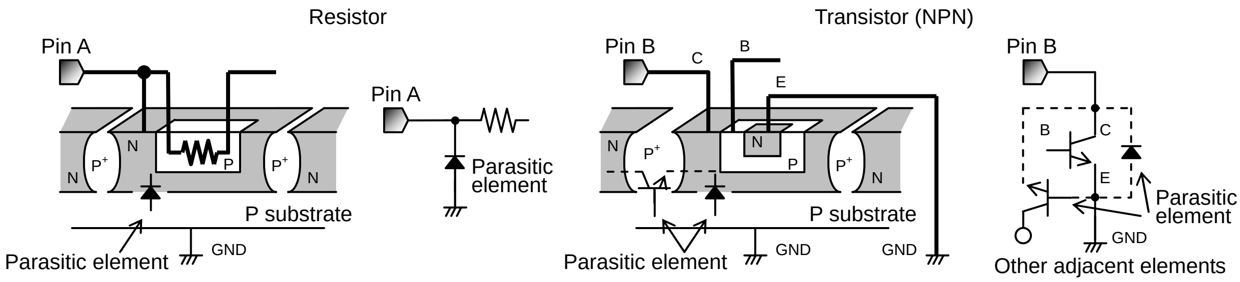
11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



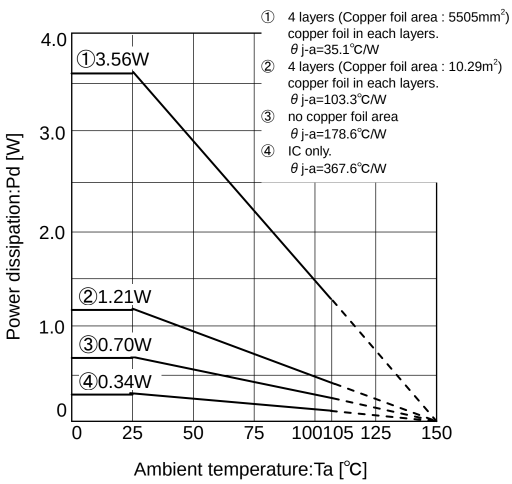
Example of IC structure

12. Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Heat Dissipation Characteristics

◎VQFN020V4040



●Type Designations (Ordering Information)

B	D	3	5	1	2	M	U	V	—	E	2

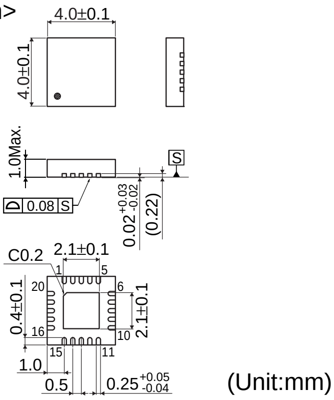
Product Name
・**BD3512**

Package Type
・**MUV : VQFN020V4040**

E2 Emboss tape reel opposite draw-out side: 1 pin

VQFN020V4040

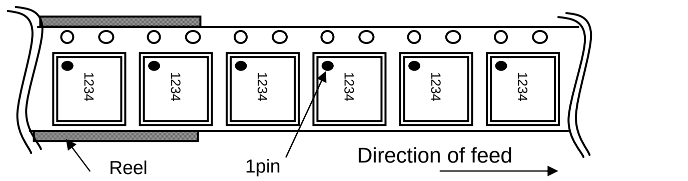
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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